



VALUE-LINE TWO-CHANNEL AC'97 CODECS

STAC9750/9751

OVERVIEW

Value-Line Stereo AC'97 CODECs with headphone drive and SPDIF outputs.

FEATURES

- 10 Full Duplex Stereo 18-bit ADCs and 20-bit DACs
- 10 AC'97 Rev 2.2 Compliant
- 10 High Performance $\Sigma\Delta$ Technology
- 10 SPDIF Output
- 10 Crystal Elimination Circuit
- 10 Headphone amplifier
- 10 Independent Sample Rates for ADCs & DACs (hardware SRCs)
- 10 20dB or 30dB Microphone Boost Capability
- 10 90dB SNR LINE-LINE
- 10 5-Wire AC-Link Protocol Compliance
- 10 Digital-Ready Architecture
- 10 General Purpose I/O
- 10 +3.3 V (STAC9751) and +5 V (STAC9750) Analog Power Supply Options
- 10 Pin Compatible With STAC9700/21/56/66
- 10 TSI Surround (SS3D) Stereo Enhancement
- 10 Energy Saving Dynamic Power Modes

KEY SPECIFICATIONS

- 10 Analog LINE_OUT SNR: 90dB
- 10 Digital DAC SNR: 89dB
- 10 Digital ADC SNR: 85dB
- 10 Full-scale Total Harmonic Distortion: 0.005%
- 10 Crosstalk between Input Channels: -70dB
- 10 Spurious Tone Rejection: 100dB

RELATED MATERIALS

- 10 Data Sheet
- 10 Reference Designs for MB, CNR, ACR and PCI applications
- 10 Audio Precision Performance Plots

DESCRIPTION

TSI's STAC9750/9751 are general purpose, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio CODEC 97 Component Specification Rev. 2.2). They have 18-bit ADCs and 20-bit DACs. The STAC9750/9751 incorporate TSI's proprietary $\Sigma\Delta$ technology to achieve a DAC SNR in excess of 89dB.

The DACs, ADCs and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel.

The STAC9750/9751 include digital input/output capability for support of modern PC systems and also an output that supports the SPDIF format.

The STAC9750/9751 is a standard 2-channel stereo CODEC. With TSI's headphone drive capability, headphones can be driven with no external amplifier.

The STAC9750/9751 may be used as a secondary CODEC, with the STAC9700/21/44/56/08/84/66 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.2 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications.

The STAC9750/9751 communicates via the five-wire AC-Link to any digital component of AC'97, providing flexibility in the audio system design.

The STAC9750/9751 supports General Purpose Input/Output (GPIO), as well as SPDIF output. These digital I/O options provide for a number of advanced architectural implementations, with volume controls and digital mixing capabilities built directly into the CODEC.

Packaged in an AC'97 compliant 48-pin TQFP, the

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1. PRODUCT BRIEF

1.1. Features

- Full duplex stereo 18-bit ADC and 20-bit DAC
- AC'97 Rev 2.2-compliant
- High performance $\Sigma\Delta$ technology
- SPDIF output
- Crystal elimination circuit
- Headphone amplifier
- Independent sample rates for ADCs & DACs (hardware SRCs)
- 20dB or 30dB microphone boost capability
- 90dB SNR LINE-LINE
- 5-Wire AC-Link protocol compliance
- Digital-Ready architecture
- General Purpose I/O
- +3.3 V (STAC9751) and +5 V (STAC9750) analog power supply options
- Pin compatible with the STAC9700/21/44/08/56/66/52
- TSI Surround (SS3D) Stereo Enhancement
- Energy saving dynamic power modes

1.2. Description

TSI's STAC9750/9751 are general purpose 18-bit ADC, 20-bit DAC, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio Codec '97 Component Specification Rev. 2.2). The STAC9750/9751 incorporate TSI's proprietary $\Sigma\Delta$ technology to achieve a DAC SNR in excess of 90 dB. The DACs, ADCs, and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9750/9751 include digital input/output capability for support of modern PC systems with an output that supports the SPDIF format. The STAC9750/9751 is a standard 2-channel stereo CODEC. With TSI's headphone drive capability, headphones can be driven with no external amplifier. The STAC9750/9751 may be used as a secondary CODEC, with the STAC9700/21/44/56/08/84/66 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.2 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications. The STAC9750/9751 communicates via the five-wire AC-Link to any digital component of AC'97, providing flexibility in the audio system design. Packaged in an AC'97 compliant 48-pin LQFP, the STAC9750/9751 can be placed on a motherboard, daughter boards, PCI, AMR, CNR, or ACR cards.

The STAC9750/9751 block diagram is illustrated in Figure 1. It provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing, and analog processing. Supported audio sample rates include 48 KHz, 44.1 KHz, 32 KHz, 22.05 KHz, 16 KHz, 11.025 KHz, and 8 KHz; additional rates are supported in the STAC9750/9751 soft audio drivers. The digital interface communicates with the AC'97 controller via the five-wire AC-Link and contains the 64-word by 16-bit registers. The two DACs convert the digital stereo PCM-out content to audio. The MIXER block combines the PCM_OUT with any analog sources, to drive the LINE_OUT and HP_OUT outputs. The MONO_OUT delivers either microphone only, or a mono mix of sources from the MIXER. The stereo variable sample rate ADCs provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM_IN signal back to the AC-Link. The microphone input and mono input can be recorded simultaneously, thus allowing for an all digital output in support of the digital

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ready initiative. All ADCs operate at 18-bit resolution and DACs at 20-bit resolution. For a digital ready record path, the microphone is connected to the left channel ADC while the mono output of the stereo mixer is connected to right channel ADC. Make sure the microphone input is not connected to the stereo mixer when in this mode.

The STAC9750/9751 supports General Purpose Input/Output (GPIO), as well as SPDIF output. These digital I/O options provide for a number of advanced architectural implementations, with volume controls and digital mixing capabilities built directly into the CODEC.

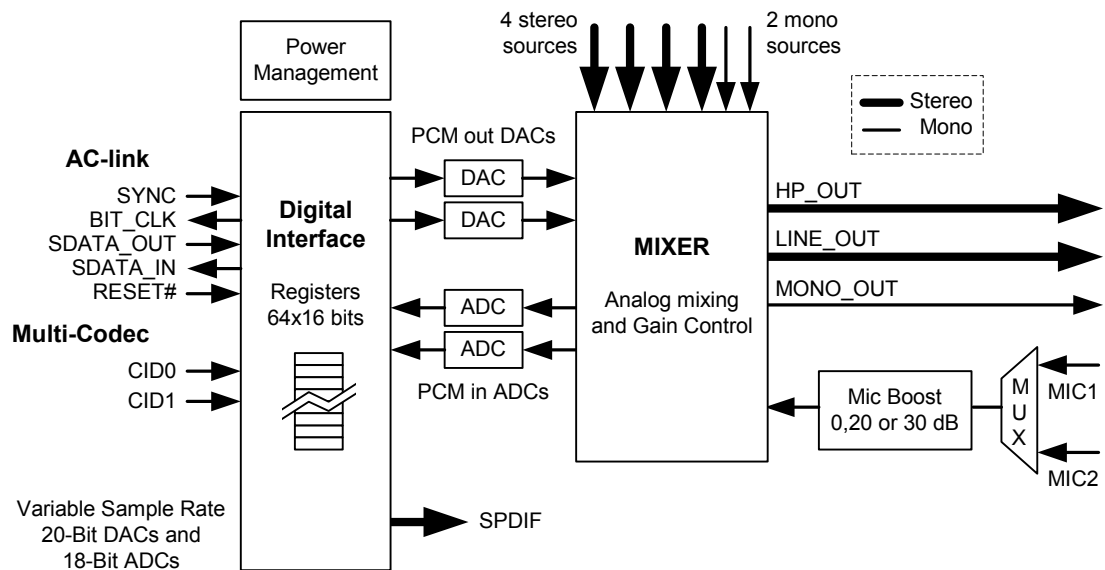
The STAC9750/9751 is designed primarily to support stereo (2-speaker) audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-CODEC option available in the STAC9750/9751 to support multiple CODECs in an AC'97 architecture. Additionally, the STAC9750/9751 provides for a stereo enhancement feature, TSI Surround 3D (SS3D). SS3D provides the listener with several options for improved speaker separation beyond the normal 2/4-speaker arrangements.

Together with the logic component (controller or advanced core logic chip-set) of AC'97, STAC9750/9751 can be SoundBlaster® and Windows Sound System® compatible with TSI's WDM driver for WIN 98/2K/ME/XP.

SoundBlaster is a registered trademark of Creative Labs.
Windows is a registered trademark of Microsoft Corporation.

1.3. STAC9750/9751 Block Diagram

Figure 1. STAC9750/9751 Block Diagram



1.4. Key Specifications

- Analog LINE_OUT SNR: 90 dB
- Digital DAC SNR: 89 dB
- Digital ADC SNR: 85 dB
- Full-scale Total Harmonic Distortion: 0.005%
- Crosstalk between Input Channels: -70 dB
- Spurious Tone Rejection: 100 dB

1.5. Related Materials

- Product Brief
- Reference Designs for MB, AMR, CNR, and ACR applications
- Audio Precision Performance Plots

1.6. Additional Support

Additional product and company information can be obtained by going to the TSI website at: www.TSI.com

2. CHARACTERISTICS/SPECIFICATIONS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings:

Stresses above the ratings listed below can cause permanent damage to the STAC9750/9751. These ratings, which are standard values for TSI commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Pin | Maximum Rating |
|---------------------------------------|-----|--|
| Maximum supply voltage | Vdd | 5.5 Volts |
| Output current per pin | | ± 4 mA, except VREF_OUT = ± 5mA |
| Voltage on any pin relative to ground | | Vss - 0.3 V to Vdd + 0.3 V |
| Operating temperature | | 0°C to +70°C |
| Storage temperature | | -55 °C to +125 °C |
| Soldering temperature | | 260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 64. |

2.1.2. Recommended Operation Conditions

| Parameter | | Min. | Typ. | Max. | Units |
|-------------------------------|-----------------------------|-------|------|-------|-------|
| Power Supply Voltage | Digital - 3.3 V | 3.135 | 3.3 | 3.465 | V |
| | Analog - 5 V | 4.75 | 5 | 5.25 | V |
| | Analog - 3.3 V | 3.135 | 3.3 | 3.465 | V |
| Ambient Operating Temperature | | 0 | | +70 | °C |
| Case Temperature | T _{case} (48-LQFP) | | | +90 | °C |

ESD: The **STAC9750/9751** is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the **STAC9750/9751** implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.1.3. Power Consumption

| Parameter | | Min | Typ | Max | Unit |
|---|--|-----|-----|-----|------|
| Digital Supply Current | | | | | |
| + 3.3 V Digital | | - | 30 | - | mA |
| Analog Supply Current (at Reset state) | | | | | |
| + 5 V Analog | | - | 35 | - | mA |
| + 3.3 V Analog | | - | 35 | - | mA |

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| Parameter | | Min | Typ | Max | Unit |
|--|-------------------------------|-----|-----|-----|------|
| Power Down Status (individually asserted) | | | | | |
| All PR measurements taken while unmuted. | | | | | |
| All paths unmuted | +5 V Analog Supply Current | - | 50 | - | mA |
| | +3.3 V Analog Supply Current | | 44 | | |
| | +3.3 V Digital Supply Current | | 33 | | |
| PR0 | +5 V Analog Supply Current | - | 42 | - | mA |
| | +3.3 V Analog Supply Current | | 39 | | |
| | +3.3 V Digital Supply Current | | 22 | | |
| PR1 | +5 V Analog Supply Current | - | 41 | - | mA |
| | +3.3 V Analog Supply Current | | 38 | | |
| | +3.3 V Digital Supply Current | | 28 | | |
| PR2 | +5 V Analog Supply Current | - | 32 | - | mA |
| | +3.3 V Analog Supply Current | | 29 | | |
| | +3.3 V Digital Supply Current | | 12 | | |
| PR3 | +5 V Analog Supply Current | - | 23 | - | mA |
| | +3.3 V Analog Supply Current | | 19 | | |
| | +3.3 V Digital Supply Current | | 12 | | |
| PR4 | +5 V Analog Supply Current | - | 50 | - | mA |
| | +3.3 V Analog Supply Current | | 44 | | |
| | +3.3 V Digital Supply Current | | 0.2 | | |
| PR5 | +5 V Analog Supply Current | - | 50 | - | mA |
| | +3.3 V Analog Supply Current | | 44 | | |
| | +3.3 V Digital Supply Current | | 12 | | |
| PR6 | +5 V Analog Supply Current | - | 38 | - | mA |
| | +3.3 V Analog Supply Current | | 36 | | |
| | +3.3 V Digital Supply Current | | 33 | | |
| PR0 & PR1 | +5 V Analog Supply Current | - | 35 | - | mA |
| | +3.3 V Analog Supply Current | | 35 | | |
| | +3.3 V Digital Supply Current | | 12 | | |
| PR0, PR1, PR2, PR6 | +5 V Analog Supply Current | - | 5 | - | mA |
| | +3.3 V Analog Supply Current | | 5 | | |
| | +3.3 V Digital Supply Current | | 12 | | |
| PR0, PR1, PR2, PR3, PR6 | +5 V Analog Supply Current | - | 0.6 | - | mA |
| | +3.3 V Analog Supply Current | | 0.6 | | |
| | +3.3 V Digital Supply Current | | 12 | | |

2.1.4. Revision Comparison

| | CA3 | | | CC1 | | | % Of Savings | | |
|-------|--------|-------|---------|--------|-------|---------|--------------|-------|---------|
| | Analog | | Digital | Analog | | Digital | Analog | | Digital |
| | 5 V | 3.3 V | 3.3 V | 5 V | 3.3 V | 3.3 V | 5 V | 3.3 V | 3.3 V |
| No PR | 78 | 69 | 27 | 50 | 44 | 33 | 36% | 36% | -22% |
| PR0 | 62 | 56 | 23 | 42 | 39 | 22 | 32% | 30% | 4% |
| PR1 | 63 | 52 | 24 | 41 | 38 | 28 | 35% | 27% | -17% |
| PR2 | 48 | 42 | 27 | 32 | 29 | 12 | 33% | 31% | 56% |
| PR3 | 40 | 35 | 21 | 23 | 19 | 12 | 43% | 46% | 43% |
| PR4 | 76 | 68 | 1 | 50 | 44 | 0.2 | 34% | 35% | 80% |
| PR5 | 75 | 68 | 7.5 | 50 | 44 | 12 | 33% | 35% | -60% |
| PR6 | 97 | 61 | 27 | 38 | 36 | 33 | 61% | 41% | -22% |

PR bit individually asserted. All PR measurements taken while unmuted.

2.1.5. AC-Link Static Digital Specifications(T_{ambient} = 25 °C, DVdd = 3.3 V ± 5%, AVss=DVss=0 V; 50 pF external load)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|-----------------|-----------|-----|-------------|------|
| Input Voltage Range | V _{in} | -0.30 | - | DVdd + 0.30 | V |
| Low level input range | V _{il} | - | - | 0.35xDVdd | V |
| High level input voltage | V _{ih} | 0.65xDVdd | - | - | V |
| High level output voltage | V _{oh} | 0.90xDVdd | - | - | V |
| Low level output voltage | V _{ol} | - | - | 0.1xDVdd | V |
| Input Leakage Current (AC-Link inputs) | - | -10 | - | 10 | μA |
| Output Leakage Current (AC-Link outputs - Hi-Z) | - | -10 | - | 10 | μA |
| Output buffer drive current | - | - | 4 | - | mA |

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2.1.6. STAC9750 Analog Performance Characteristics

($T_{\text{ambient}} = 25^{\circ}\text{C}$, $AV_{\text{dd}} = 5.0\text{ V} \pm 5\%$, $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$, $AV_{\text{ss}}=DV_{\text{ss}}=0\text{ V}$; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 Vrms, 10 K Ω / 50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0dB settings on all gain stages)

| Parameter | Min | Typ | Max | Unit |
|--|--------|------------|--------|------------|
| Full Scale Input Voltage: | | | | |
| All Analog Inputs except Microphone | - | 1.0 | - | Vrms |
| Microphone Inputs (Note 1) | - | 0.03 | - | Vrms |
| Full Scale Output: | | | | |
| Line Output | - | 1.0 | - | Vrms |
| PCM (DAC) to LINE_OUT | - | 1.0 | | Vrms |
| MONO_OUT | - | 1.0 | - | Vrms |
| HEADPHONE_OUT (32 Ω load) (peak) | - | 50 | - | mW |
| Analog S/N: (Note 2) | | | | |
| CD to LINE_OUT | - | 90 | - | dB |
| Other to LINE_OUT | - | 90 | - | dB |
| D/A to LINE_OUT | - | 89 | - | dB |
| LINE_IN to A/D with High pass filter enabled | - | 85 | - | dB |
| Analog Frequency Response (Note 3) | 20 | - | 20,000 | Hz |
| Total Harmonic Distortion: (Note 4) | | | | |
| CD to LINE_OUT | - | 89 | - | dB |
| Other to LINE_OUT | - | 89 | - | dB |
| D/A to LINE_OUT (full scale) | - | 89 | - | dB |
| LINE_IN to A/D with High pass filter enabled | 84 | - | - | dB |
| HEADPHONE_OUT | 74 | 80 | - | dB |
| A/D & D/A Digital Filter Pass Band (Note 5) | 20 | - | 19,200 | Hz |
| A/D & D/A Digital Filter Transition Band | 19,200 | - | 28,800 | Hz |
| A/D & D/A Digital Filter Stop Band | 28,800 | - | - | Hz |
| A/D & D/A Digital Filter Stop Band Rejection (Note 6) | 100 | - | - | dB |
| DAC Out-of-Band Rejection (Note 7) | 55 | - | - | dB |
| Group Delay (48KHz sample rate) | - | | 1 | ms |
| Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency) | - | 70 | - | dB |
| Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency) | - | 100 | - | dB |
| Spurious Tone Rejection | - | 100 | - | dB |
| Attenuation, Gain Step Size | - | 1.5 | - | dB |
| Input Impedance (Note 8) | - | 50 | - | K Ω |
| Input Capacitance | - | 15 | - | pF |
| VREF_OUT | - | 0.5 X AVdd | - | V |
| Interchannel Gain Mismatch ADC | - | - | 0.5 | dB |
| Interchannel Gain Mismatch DAC | - | - | 0.5 | dB |

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- Note:**
1. With +30 dB Boost on, 1.0 Vrms with Boost off.
 2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
 3. ± 1 dB limits for Line Output & 0 dB gain.
 4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a 20 KHz BW, 48 KHz Sample Frequency.
 5. ± 0.25 dB limits
 6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
 7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
 8. For all inputs except PC BEEP.

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2.1.7. STAC9751 Analog Performance Characteristics

(T_{ambient} = 25 °C, AVdd = DVdd = 3.3 V ± 5%, AVss=DVss=0 V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 Vrms, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0dB settings on all gain stages)

| Parameter | Min | Typ | Max | Unit |
|--|--------|------------|--------|--------|
| Full Scale Input Voltage: | | | | |
| All Analog Inputs except Microphone | - | 1.0 | - | Vrms |
| Microphone Inputs (Note 1) | - | 0.03 | - | Vrms |
| Full Scale Output: | | | | |
| Line Output | - | 0.5 | - | Vrms |
| PCM (DAC) to LINE_OUT | | 0.5 | | Vrms |
| MONO_OUT | - | 0.5 | - | Vrms |
| HEADPHONE_OUT (32 Ω load) (peak) | - | 12.5 | - | mW |
| Analog S/N: (Note 2) | | | | |
| CD to LINE_OUT | - | 90 | - | dB |
| Other to LINE_OUT | - | 90 | - | dB |
| D/A to LINE_OUT | - | 89 | - | dB |
| LINE_IN to A/D with High pass filter enabled | - | 85 | - | dB |
| Analog Frequency Response (Note 3) | 20 | - | 20,000 | Hz |
| Total Harmonic Distortion: (Note 4) | | | | |
| CD to LINE_OUT | - | 89 | - | dB |
| Other to LINE_OUT | - | 89 | - | dB |
| D/A to LINE_OUT (full scale) | - | 89 | - | dB |
| LINE_IN to A/D with High pass filter enabled | - | 84 | - | dB |
| HEADPHONE_OUT | 74 | 80 | - | dB |
| A/D & D/A Digital Filter Pass Band (Note 5) | 20 | - | 19,200 | Hz |
| A/D & D/A Digital Filter Transition Band | 19,200 | - | 28,800 | Hz |
| A/D & D/A Digital Filter Stop Band | 28,800 | - | - | Hz |
| A/D & D/A Digital Filter Stop Band Rejection (Note 6) | 100 | - | - | dB |
| DAC Out-of-Band Rejection (Note 7) | 55 | - | - | dB |
| Group Delay (48 KHz sample rate) | - | - | 1 | ms |
| Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency) | - | 70 | - | dB |
| Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency) | - | 100 | - | dB |
| Spurious Tone Rejection | - | 100 | - | dB |
| Attenuation, Gain Step Size | - | 1.5 | - | dB |
| Input Impedance (Note 8) | - | 50 | - | KΩ |
| Input Capacitance | - | 15 | - | pF |
| VREF_OUT | - | 0.5 X AVdd | - | V |
| Interchannel Gain Mismatch ADC | - | - | 0.5 | dB |
| Interchannel Gain Mismatch DAC | - | - | 0.5 | dB |
| Gain Drift | - | 100 | - | ppm/°C |

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- Note:**
1. With +30 dB Boost on, 1.0 Vrms with Boost off.
 2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio). 0 dB gain, 20 KHz BW, 48 KHz Sample Frequency ± 1 dB limits.
 3. ± 1 dB limits for Line Output & 0 dB gain.
 4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a 20 KHz BW, 48 KHz Sample Frequency.
 5. ± 0.25 dB limits
 6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
 7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
 8. For all inputs except PC BEEP.

2.2. AC Timing Characteristics

($T_{\text{ambient}} = 25^{\circ}\text{C}$, $\text{AVdd} = 3.3\text{ V or }5\text{ V} \pm 5\%$, $\text{DVdd} = 3.3\text{ V} \pm 5\%$, $\text{AVss} = \text{DVss} = 0\text{ V}$; 50 pF external load)

2.2.1. Cold Reset

Figure 2. Cold Reset Timing

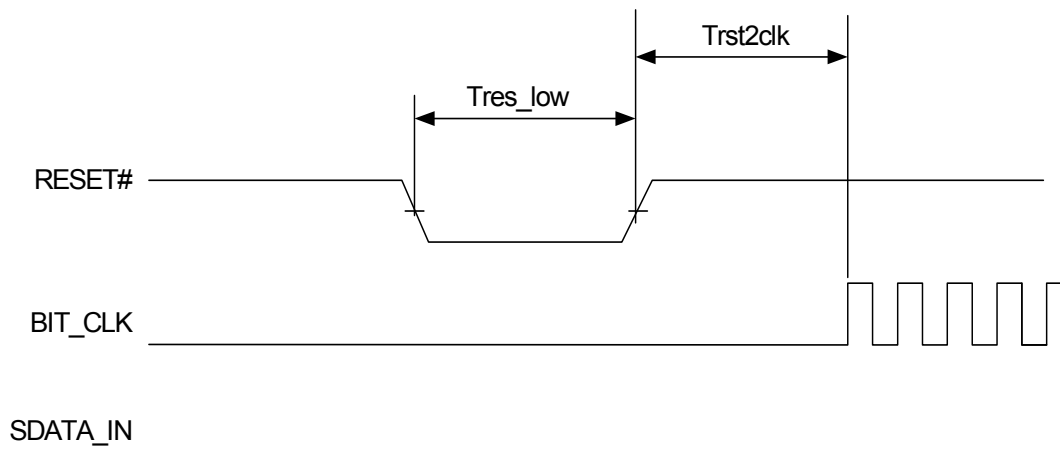


Table 1. Cold Reset Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|--|-----------------------|-------|-----|-----|---------------|
| RESET# active low pulse width | $T_{\text{res_low}}$ | 1.0 | - | - | μs |
| RESET# inactive to BIT_CLK startup delay | Trst2clk | 162.8 | - | - | ns |

Note: BIT_CLK and SDATAIN are in a high impedance state during reset.

2.2.2. Warm Reset

Figure 3. Warm Reset Timing

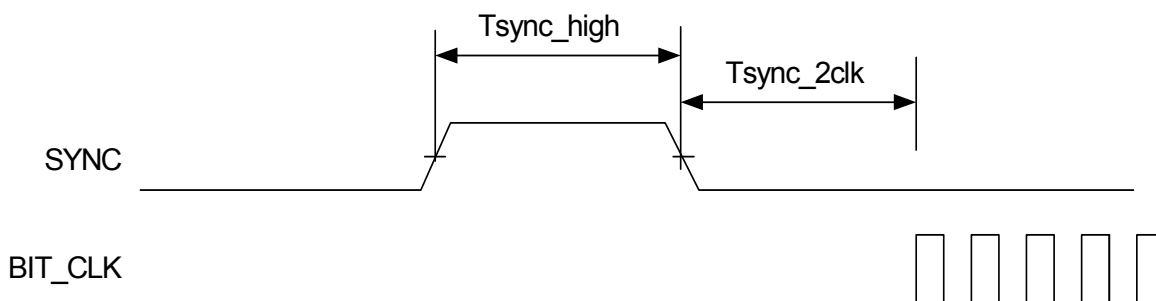


Table 2. Warm Reset Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|--|-------------------------|-------|-----|-----|---------------|
| SYNC active high pulse width | $T_{\text{sync_high}}$ | 1.0 | 1.3 | - | μs |
| SYNC inactive to BIT_CLK startup delay | T_{sync2clk} | 162.8 | - | - | ns |

2.2.3. Clocks

Figure 4. Clocks Timing

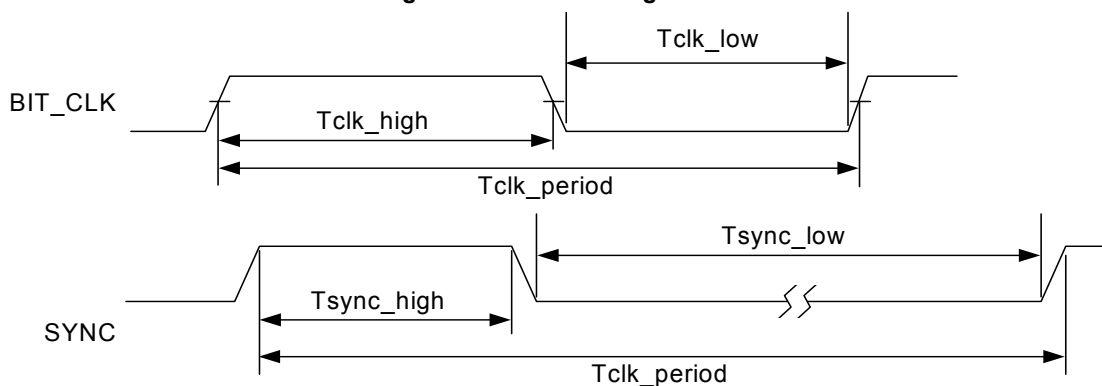


Table 3. Clocks Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|-----------------------------------|--------------|-----|--------|-----|-------|
| BIT_CLK frequency | | - | 12.288 | - | MHz |
| BIT_CLK period | Tclk_period | - | 81.4 | - | ns |
| BIT_CLK output jitter | | - | 750 | - | ps |
| BLT_CLK high pulse width (Note 1) | Tclk_high | 36 | 40.7 | 45 | ns |
| BIT_CLK low pulse width (Note 1) | Tclk_low | 36 | 40.7 | 45 | ns |
| SYNC frequency | | - | 48.0 | - | KHz |
| SYNC period | Tsync_period | - | 20.8 | - | μs |
| SYNC high pulse width | Tsync_high | - | 1.3 | - | μs |
| SYNC low pulse width | Tsync_low | - | 19.5 | - | μs |

Note: 1. Worst case duty cycle restricted to 45/55.

The STAC9750/9751 supports several clock frequency inputs as described in the following table. In general, when a 24.576 MHz clock XTAL is not used, the XTAL_OUT pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

Table 4. Clock Mode Configuration

| XTL_OUT Pin Config | CID1 Pin Config | CID0 Pin Config | Clock Source Input | CODEC Mode | CODEC ID |
|--------------------|-----------------|-----------------|---------------------|------------|----------|
| XTAL | float | float | 24.576 MHz XTAL | P | 0 |
| XTAL or open | float | pulldown | 12.288 MHz BIT_CLK | S | 1 |
| XTAL or open | pulldown | float | 12.288 MHz BIT_CLK | S | 2 |
| XTAL or open | pulldown | pulldown | 12.288 MHz BIT_CLK | S | 3 |
| short to ground | float | float | 14.31818 MHz source | P | 0 |
| short to ground | float | pulldown | 27 MHz source | P | 0 |
| short to ground | pulldown | float | 48 MHz source | P | 0 |
| short to ground | pulldown | pulldown | 24.576 MHz source | P | 0 |

2.2.4. Data Setup and Hold

(47.5-75 pF external load)

Figure 5. Data Setup and Hold Timing

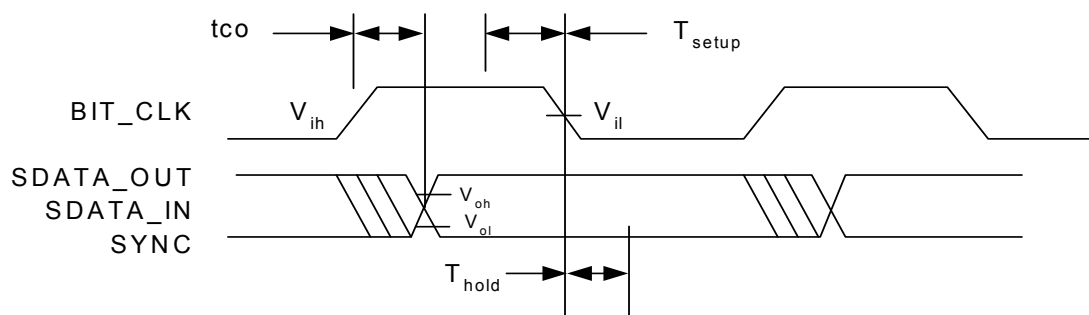


Table 5. Data Setup and Hold Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|-----------------------------------|--------|-----|-----|-----|-------|
| Setup to falling edge of BIT_CLK | Tsetup | 10 | - | - | ns |
| Hold from falling edge of BIT_CLK | Thold | 10 | - | - | ns |

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

2.2.5. Signal Rise and Fall Times

(75pF external load; from 10% to 90% of Vdd)

Figure 6. Signal Rise and Fall Times Timing

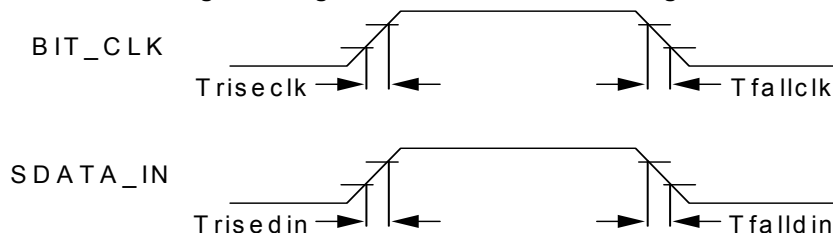


Table 6. Signal Rise and Fall Times Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|--------------------|----------|-----|-----|-----|-------|
| BIT_CLK rise time | Triseclk | - | - | 6 | ns |
| BIT_CLK fall time | Tfallclk | - | - | 6 | ns |
| SDATA_IN rise time | Trisedin | - | - | 6 | ns |
| SDATA_IN fall time | Tfalldin | - | - | 6 | ns |

2.2.6. AC-Link Low Power Mode Timing

Figure 7. AC-Link Low Power Mode Timing

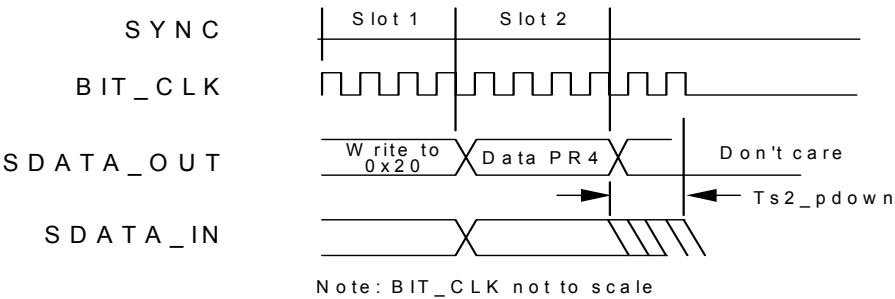


Table 7. AC-Link Low Power Mode Timing Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|--|-----------|-----|-----|-----|-------|
| End of Slot 2 to BIT_CLK, SDATA_IN low | Ts2_pdown | - | - | 1.0 | µs |

2.2.7. ATE Test Mode

Figure 8. ATE Test Mode Timing

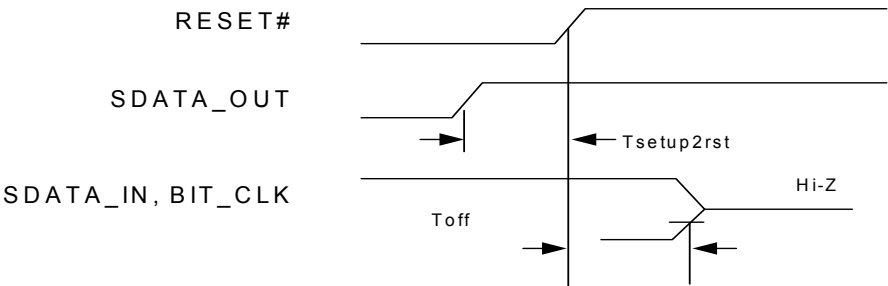


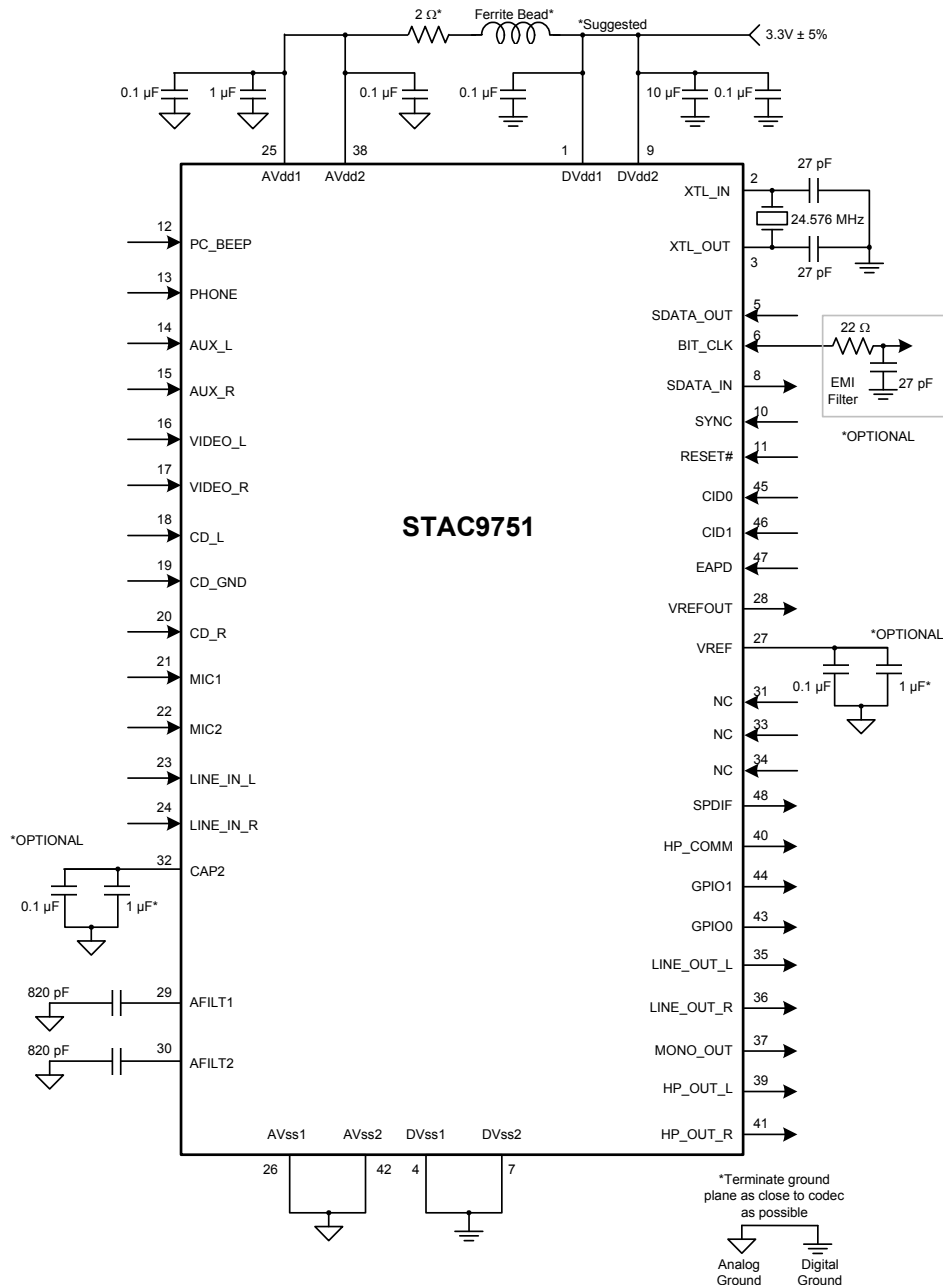
Table 8. ATE Test Mode Specifications

| Parameter | Symbol | Min | Typ | Max | Units |
|---|------------|------|-----|------|-------|
| Setup to trailing edge of RESET# (also applies to SYNC) | Tsetup2rst | 15.0 | - | - | ns |
| Rising edge of RESET# to Hi-Z delay | Toff | - | - | 25.0 | ns |

- Note:**
- 1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes the STAC9750/9751 AC-Link outputs to go high-impedance, which is suitable for ATE in-circuit testing.
 - 2. Once the test mode has been entered, the STAC9750/9751 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.
 - 3. # denotes active low.

3. TYPICAL CONNECTION DIAGRAM

Figure 9. STAC9751 Typical Connection Diagram

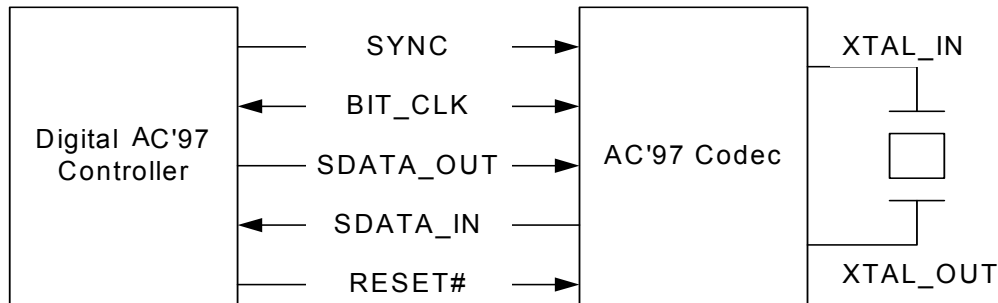


- Note:**
1. See Appendix A for specific connection requirements prior to operation.
 2. See Figure 24 on page 66 for split supply connections.
 3. **PIN 48: TO ENABLE SPDIF, USE AN 1 KW-10 KW EXTERNAL PULLDOWN. TO DISABLE SPDIF, USE AN 1 KW-10 KW EXTERNAL PULLUP. DO NOT LEAVE PIN 48 FLOATING.**
 4. The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect.

4. AC-LINK

Figure 10 shows the AC-Link point to point serial interconnect between the STAC9750/9751 and its companion controller. All digital audio streams and command/status information are communicated over this AC-Link. See “Digital Interface” on page 21 for details.

Figure 10. AC-Link to its Companion Controller



4.1. Clocking

STAC9750/9751 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator, through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288 MHz.

The beginning of all audio sample packets, or “Audio Frames”, transferred over AC-Link is synchronized to the rising edge of the “SYNC” signal driven by the AC'97 controller. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

4.2. Reset

There are 3 types of resets:

1. a “cold” reset where all STAC9750/9751 logic and registers are initialized to their default state
2. a “warm” reset where the contents of the STAC9750/9751 register set are left unaltered
3. a “register” reset which only initializes the STAC9750/9751 registers to their default states

After signaling a reset to the STAC9750/9751, the AC'97 controller should not attempt to play or capture audio data until it has sampled a “CODEC Ready” indication via register 26h from the STAC9750/9751.

For proper reset operation SDATA_OUT should be 0 during cold reset.

5. DIGITAL INTERFACE

5.1. AC-Link Digital Serial Interface Protocol

The STAC9750/9751 communicates to the AC'97 controller via a 5-wire, digital, serial, AC-Link interface, which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point-to-point serial interconnect. The AC-Link handles multiple input and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC'97 controller synchronizes all AC-Link data transaction. Table 9 shows the data streams available on the STAC9750/9751:

Table 9. STAC9750/9751 Available Data Streams

| | | |
|-----------------|----------------|---------------------------------------|
| PCM Playback | 2 output slots | 2 Channel composite PCM output stream |
| PCM Record data | 2 input slots | 2 Channel composite PCM input stream |
| Control | 2 output slots | Control register write port |
| Status | 2 input slots | Control register read port |

Synchronization of all AC-Link data transactions is handled by the AC'97 controller. The STAC9750/9751 drives the serial bit clock onto AC-Link. The AC'97 controller then qualifies with a synchronization signal to construct audio frames.

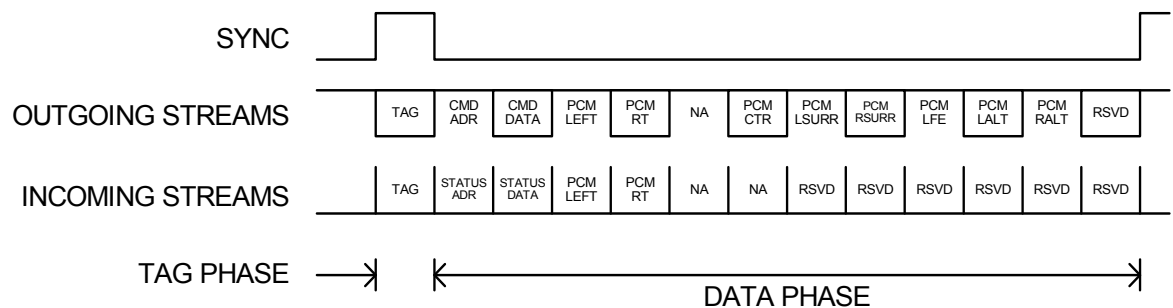
SYNC, fixed at 48 KHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support twelve 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-Link data, STAC9750/9751 for outgoing data and AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-Link protocol provides for a special 16-bit (13-bits defined, with 3 Reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a "slot-valid" tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (STAC9750/9751 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, SYNC, and data signals can be halted by the controller.

Figure 11. AC'97 Standard Bi-directional Audio Frame

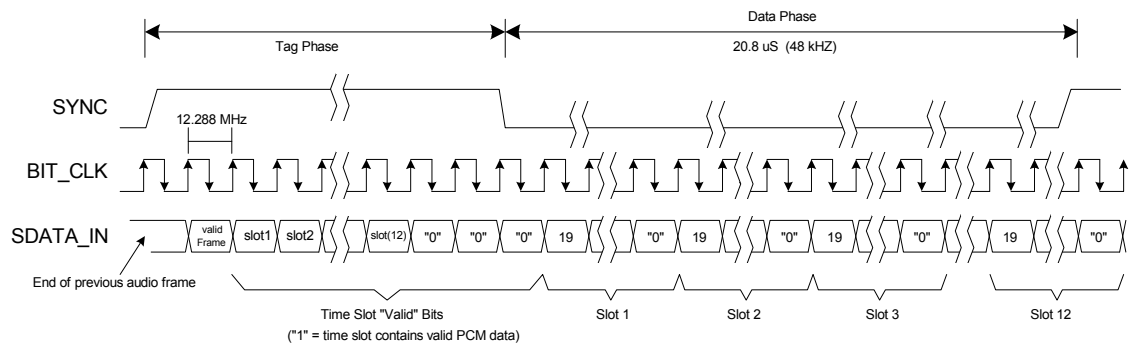


5.1.1. AC-Link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the STAC9750/9751 DAC inputs, and control registers. Each audio output frame supports up to twelve 20-bit outgoing data time slots. Slot 0 is a special Reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

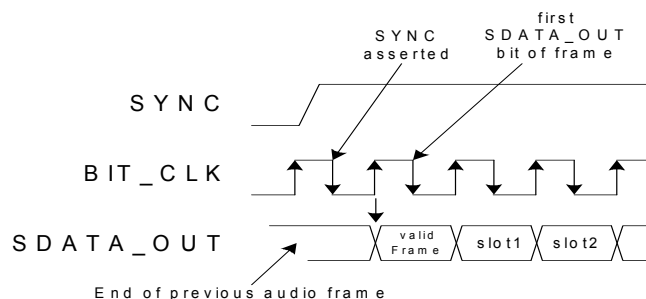
Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the STAC9750/9751 indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-Link at its fixed 48 KHz audio frame rate. The following diagram illustrates the time slot based AC-Link protocol.

Figure 12. AC-Link Audio Output Frame



A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the STAC9750/9751 samples the assertion of SYNC. This following edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and subsequently sampled by the STAC9750/9751 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams, are time aligned.

Figure 13. Start of an Audio Output Frame



SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0s by the AC'97 controller.

When mono audio sample streams are sent from the AC'97 controller, it is necessary that BOTH left and right sample stream time slots be filled with the same data.

5.1.1.1. Slot 1: Command Address Port

The command port is used to control features and monitor status (see Audio Input Frame Slots 1 and 2) of the STAC9750/9751 functions including, but not limited to, mixer settings and power management (refer to the Control Register section of this specification).

The control interface architecture supports up to sixty-four 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid. Odd accesses are considered invalid and return 0000h.

Audio output frame slot 1 communicates control register address and write/read command information to the STAC9750/9751.

Table 10. Command Address Port Bit Assignments

| Bit | Description | Comments |
|-------|------------------------|--|
| 19 | Read/Write command | 1= read, 0=write |
| 18:12 | Control Register Index | Sixty-four 16-bit locations, addressed on even byte boundaries |
| 11:0 | Reserved | Stuffed with 0s |

The first bit (MSB) sampled by STAC9750/9751 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are Reserved and must be stuffed with 0s by the AC'97 controller.

5.1.1.2. Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19).

Table 11. Command Data Port Bit Assignments

| Bit | Description | Comments |
|------|-----------------------------|--|
| 19:4 | Control Register Write Data | Stuffed with 0s if current operation is a read |
| 3:0 | Reserved | Stuffed with 0s |

If the current command port operation is a read cycle, then the entire slot time must be stuffed with 0s by the AC'97 controller.

5.1.1.3. Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

5.1.1.4. Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (on the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0s.

5.1.1.5. Slot 5: Reserved

Audio output frame slot 5 is Reserved for modem operation and is not used by the STAC9750/9751.

5.1.1.6. Slot 6: PCM Center Channel

Audio output frame slot 6 is the composite digital audio center stream used in a multi-channel application where the STAC9750/9751 is programmed to accept the primary DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

5.1.1.7. Slot 7: PCM Left Surround Channel

Audio output frame slot 7 is the composite digital audio left surround stream. In the default state, the STAC9750/9751 accepts PCM data from slots 7 and 8 for the surround DACs, for output to the DAC_OUT pins. As a programming option, PCM data from slots 7 and 8 may be used to supply data to the primary DACs when slots 6 and 9 are used to drive the surround DACs. Please refer to the register programming section for details on the multi-channel programming options.

5.1.1.8. Slot 8: PCM Right Surround Channel

Audio output frame slot 8 is the composite digital audio right surround stream. As a programming option, PCM data from slots 7 and 8 may be used to supply data to the primary DACs. Please refer to the register programming section for details on the multi-channel programming options.

5.1.1.9. Slot 9: PCM Low Frequency Channel

Audio output frame slot 9 is the composite digital audio low frequency stream used in a multi-channel application where the STAC9750/9751 is programmed to accept the primary DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

5.1.1.10. Slot 10: PCM Alternate Left

Audio output frame slot 10 is the composite digital audio alternate left stream used in a multi-channel applications. Please refer to the register programming section for details on the multi channel programming options.

5.1.1.11. Slot 11: PCM Alternate Right

Audio output frame slot 11 is the composite digital audio alternate right stream used in a multi-channel applications. Please refer to the register programming section for details on the multi channel programming options.

5.1.1.12. Slot 12: Reserved

Audio output frame slot 12 is Reserved for modem operations and is not used by the STAC9750/9751.

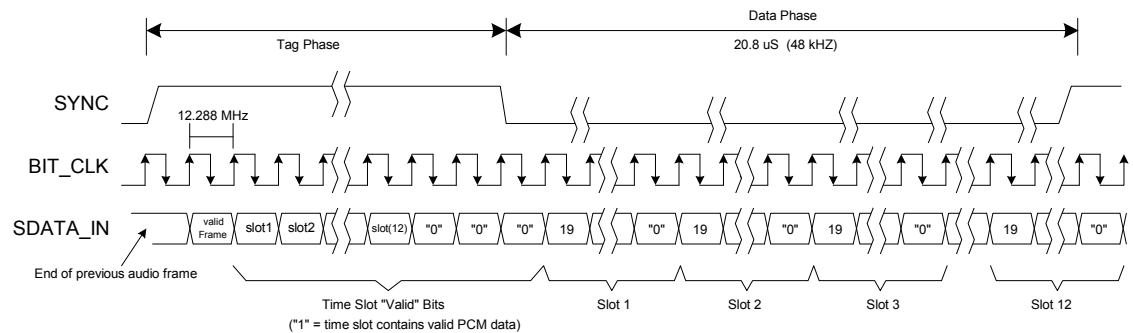
5.1.2. AC-Link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-Link audio input frame consists of twelve 20-bit time slots. Slot 0 is a special Reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the STAC9750/9751 is in the "CODEC Ready" state or not. If the "CODEC Ready" bit is a 0, this indicates that STAC9750/9751 is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while STAC9750/9751's voltage references settle. When the AC-Link "CODEC Ready" indicator bit is a 1, it indicates that the AC-Link and STAC9750/9751 control/status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control Status Register (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

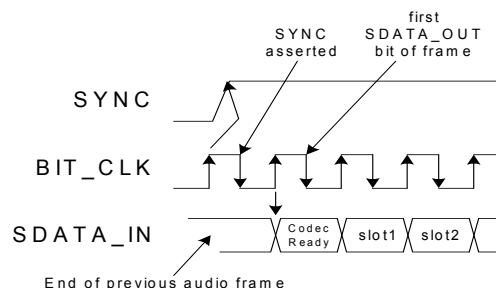
Prior to any attempts at putting STAC9750/9751 into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that STAC9750/9751 has become "CODEC Ready". Once the STAC9750/9751 is sampled "CODEC Ready", the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-Link protocol.

Figure 14. STAC9750/9751 Audio Input Frame



A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. Immediately following the falling edge of BIT_CLK, the STAC9750/9751 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the STAC9750/9751 transitions SDATA_IN into the first bit position of slot 0 ("CODEC Ready" bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 15. Start of an Audio Input Frame



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SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0s by STAC9750/9751. SDATA_IN data is sampled on the falling edges of BIT_CLK.

5.1.2.1. Slot 1: Status Address Port

The status port is used to monitor status for STAC9750/9751 functions including, but not limited to, mixer settings and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by STAC9750/9751 during slot 0.)

Table 12. Status Address Port Bit Assignments

| Bit | Description | Comments |
|-------|------------------------|---|
| 19 | Reserved | Stuffed with 0 |
| 18:12 | Control Register Index | Echo of register index for which data is being returned |
| 11:2 | Slot Request | see sections below |
| 1:0 | Reserved | Stuffed with 0 |

The first bit (MSB) generated by STAC9750/9751 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0 by the STAC9750/9751.

5.1.2.2. Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Table 13. Status Data Port Bit Assignments

| Bit | Description | Comments |
|------|----------------------------|------------------------------------|
| 19:4 | Control Register Read Data | Stuffed with 0 if tagged "invalid" |
| 3:0 | Reserved | Stuffed with 0 |

If Slot 2 is tagged "invalid" by STAC9750/9751, then the entire slot will be stuffed with 0's.

5.1.2.3. Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

5.1.2.4. Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

5.1.2.5. Slot 5: Reserved

Audio input frame slot 5 is Reserved for modem operation and is not used by the STAC9750/9751. This slot is always stuffed with 0.

5.1.2.6. Slot 6: PCM Left Record Channel

Audio input frame slot 6 is the left channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

See section 6.5.25; page 48 for slot configurations and register settings.

5.1.2.7. Slot 7: PCM Left Record Channel

Audio input frame slot 7 is the left channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

See section 6.5.25; page 48 for slot configurations and register settings.

5.1.2.8. Slot 8: PCM Right Record Channel

Audio input frame slot 8 is the right channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

See section 6.5.25; page 48 for slot configurations and register settings.

5.1.2.9. Slot 9: PCM Right Record Channel

Audio input frame slot 9 is the right channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

See section 6.5.25; page 48 for slot configurations and register settings.

5.1.2.10. Slot 10: PCM Left Record Channel

Audio input frame slot 10 is the left channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

See section 6.5.25; page 48 for slot configurations and register settings.

5.1.2.11. Slot 11: PCM Right Record Channel

Audio input frame slot 11 is the right channel output of STAC9750/9751 input MUX, post-ADC.

STAC9750/9751 ADCs are implemented to support 18-bit resolution.

STAC9750/9751 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0 to fill out its 20-bit time slot.

See section 6.5.25; page 48 for slot configurations and register settings.

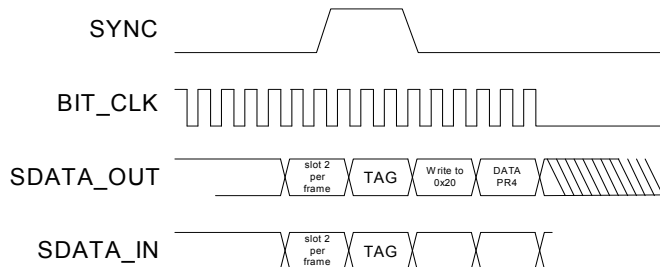
5.1.2.12. Slot 12: Reserved

Audio input frame slot 12 is Reserved for modem operation and is not used by the STAC9750/9751. This slot is always stuffed with 0.

5.2. AC-Link Low Power Mode

The STAC9750/9751 AC-Link can be placed in the low power mode by programming register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC'97 controller can wake up the STAC9750/9751 by providing the appropriate reset signals.

Figure 16. STAC9750/9751 Powerdown Timing



Note: BIT_CLK not to scale

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC, and SDATA_OUT low after programming the STAC9750/9751 to this low power mode.

5.3. Waking up the AC-Link

Once the STAC9750/9751 has halted BIT_CLK, there are only two ways to “wake up” the AC-Link. Both methods must be activated by the AC'97 controller. The AC-Link protocol provides for a “Cold AC'97 Reset”, and a “Warm AC'97 Reset”. The current power down state would ultimately dictate which form of reset is appropriate. Unless a “cold” or “register” reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes. Once powered down, re-activation of the AC-Link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-Link powers up it indicates readiness via the CODEC Ready bit (input slot 0, bit 15).

Cold Reset - a cold reset is achieved by asserting RESET# for the minimum specified time, and then bringing RESET# back HIGH. The reset occurs on the rising edge when RESET# is deasserted. By asserting and deasserting RESET#, BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all STAC9750/9751 control registers will be initialized to their default power-on-reset values.

Note: RESET# is an asynchronous input. (# denotes active low)

Warm Reset - a warm reset will re-activate the AC-Link without altering the current STAC9750/9751 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 μ s in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the STAC9750/9751.

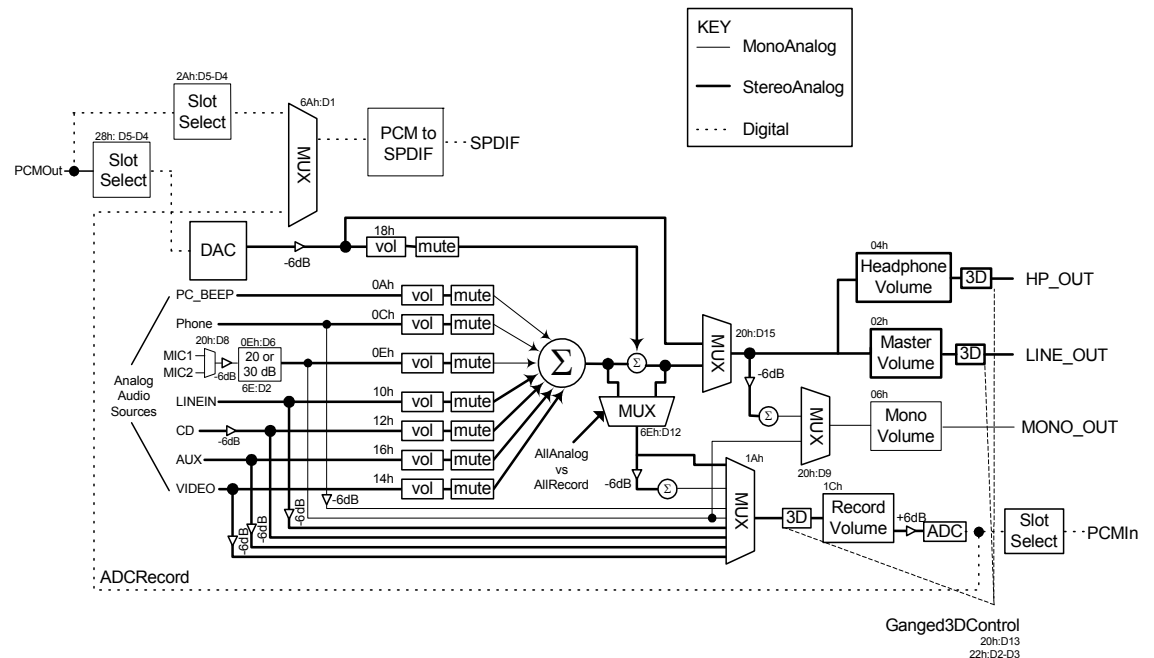
6. STAC9750/9751 MIXER

The STAC9750/9751 includes analog and digital mixers for maximum flexibility. The analog mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. The analog mixer also includes several extensions of the AC'97 specification to support "all analog record" capability as well as "POP BYPASS" mode for all digital playback. The analog sources include:

- **System Audio:** digital PCM input and output for business, games and multimedia
- **CD/DVD:** analog CD/DVD-ROM audio with internal connections to CODEC mixer
- **Mono microphone:** choice of desktop microphone, with programmable boost and gain
- **Speakerphone:** use of system microphone and speakers for telephone, DSVD, and video conferencing
- **Video:** TV tuner or video capture card with internal connections to CODEC mixer
- **AUX/synth:** analog FM or wavetable synthesizer, or other internal source

The digital mixer includes inputs for the PCM DAC and the recorded ADC output

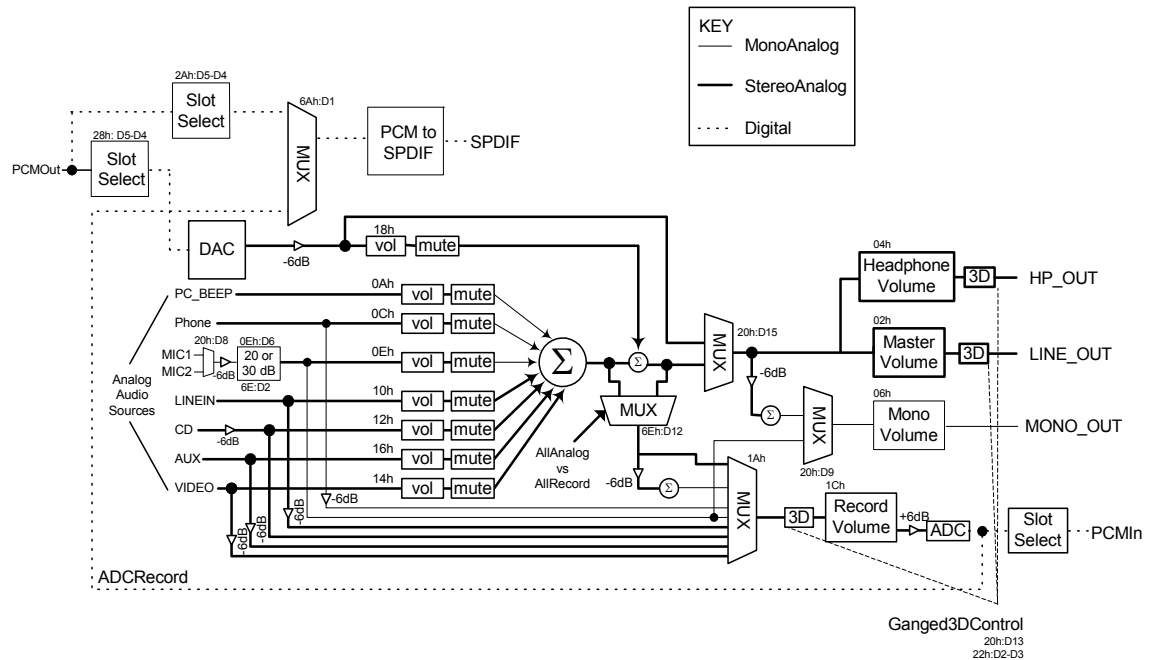
Figure 17. STAC9750 2-Channel Mixer Functional Diagram



| Source | Function | Connection |
|---------|--|------------------------------|
| PC_BEEP | PC BEEP pass through to LINE_OUT | From PC_BEEP output |
| PHONE | MONO input | From telephony subsystem |
| MIC1 | Desktop microphone | From microphone jack |
| MIC2 | Second microphone | From second microphone jack |
| LINE_IN | External audio source | From line-in jack |
| CD | Audio from CD-ROM | Cable from CD-ROM |
| VIDEO | Audio from TV tuner or video camera | Cable from TV or VidCap card |
| AUX | Upgrade synth or other external source | Internal connector |
| PCM out | Digital audio output from AC'97 Controller | AC-Link |

| Destination | Function | Connection |
|-------------|---|---------------------------|
| HP_OUT | Stereo mix of all sources | To headphone out jack |
| LINE_OUT | Stereo mix of all sources | To output jack |
| MONO_OUT | Microphone or MONO Analog mixer output | To telephony subsystem |
| PCM in | Digital data from the CODEC to the AC'97 Controller | AC-Link |
| SPDIF | SPDIF digital audio output | To SPDIF output connector |

Figure 18. STAC9751 2-Channel Mixer Functional Diagram



6.1. Analog Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The STAC9750/9751 supports the following input sources:

- Any mono or stereo source
- Mono or stereo mix of all sources
- Two-channel input with mono output reference (microphone + stereo mix)

Note: All unused inputs should be tied together connected to ground through a capacitor (0.1 μ F suggested).

6.2. Analog Mixer Output

The mixer generates three distinct outputs:

- A stereo mix of all sources for output to the LINE_OUT and HP_OUT
- A stereo mix of all analog sources for recording
- Microphone only or mono mix of all sources for MONO_OUT

Note: Mono output of stereo mix is attenuated by -6 dB.

6.3. SPDIF Digital Mux

The STAC9750/9751 incorporates a digital output that supports SPDIF formats. A multiplexer determines which of two digital input streams are used for the digital output conversion process. These two streams include the PCM OUT data from the audio controller and the ADC recorded output. The normal analog LINE_OUT signal can be converted to the SPDIF formats by using the internal ADC to record the "MIX" output, which is the combination of all analog and all digital sources. In the case of digital controllers with support for 4 or more channels, the SPDIF output mode can be used to support compressed 6-channel output streams for delivery to home theater systems. These can be routed on alternate AC-Link slots to the SPDIF output, while the standard 2-channel output is delivered as selected by bits D5 and D4 in Register 6E. If the digital controller supports 6 channels, a SPDIF output with 4 analog channels can also be configured (in a multi-CODEC setup). For more information for SPDIF please see 6.5.12.2; page 43.

PIN 48: TO ENABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLDOWN. TO DISABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLUP. DO NOT LEAVE PIN 48 FLOATING.

6.4. PC Beep Implementation

PC Beep is active on power up and defaults to an un-muted state. The PC_BEEP input is routed directly to the MONO_OUT, LINE_OUT and HP_OUT pins of the CODEC. Because the PC_BEEP input drive is often a full scale digital signal, some resistive attenuation of the PC_BEEP input is recommended to keep the beep tone within reasonable volume levels. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation. This style of PC Beep is related to the AC'97 Specification Rev 2.2. To use the analog PC Beep, a value of 00h to bits F[7:0](D[12:5]) disables the Digital PC Beep generation. PV[3:0] (D[4:1]) controls the volume level from 0 to 45dB of attenuation in 3dB steps.

6.5. Programming Registers

Table 14. Programming Registers

| Address | Name | Default | Location |
|---------|-------------------------------|---------|-------------------------|
| 00h | Reset | 6990h | 6.5.1; page 34 |
| 02h | Master Volume | 8000h | 6.5.2.1; page 34 |
| 04h | HP_OUT Mixer Volume | 8000h | 6.5.2.2; page 34 and 35 |
| 06h | Master Volume MONO | 8000h | 6.5.2.3; page 35 |
| 0Ah | PC Beep Mixer Volume | 0000h | 6.5.3; page 35 |
| 0Ch | Phone Mixer Volume | 8008h | 6.5.4.1; page 36 |
| 0Eh | Microphone Mixer Volume | 8008h | 6.5.4.2; page 36 |
| 10h | Line In Mixer Volume | 8808h | 6.5.4.3; page 36 |
| 12h | CD Mixer Volume | 8808h | 6.5.4.4; page 37 |
| 14h | Video Mixer Volume | 8808h | 6.5.4.5; page 37 |
| 16h | Aux Mixer Volume | 8808h | 6.5.4.6; page 37 |
| 18h | PCM Out Mixer Volume | 8808h | 6.5.4.7; page 37 |
| 1Ah | Record Select | 0000h | 6.5.5; page 37 |
| 1Ch | Record Gain | 8000h | 6.5.6; page 38 |
| 20h | General Purpose | 0000h | 6.5.7; page 38 |
| 22h | 3D Control | 0000h | 6.5.8; page 39 |
| 24h | Audio Interrupt | 0000h | 6.5.9; page 39 |
| 26h | Powerdown Control/Status | 000Fh | 6.5.10; page 40 |
| 28h | Extended Audio ID | 0205h | 6.5.11; page 41 |
| 2Ah | Extended Audio Control/Status | 0400h | 6.5.12; page 42 |
| 2Ch | PCM DAC Rate | BB80h | 6.5.14; page 44 |
| 32h | PCM LR ADC Rate | BB80h | 6.5.15; page 44 |
| 3Ah | SPDIF Control | 2A00h | 6.5.16; page 44 |
| 3Eh | Extended Modem Control/Status | 0100h | 6.5.17; page 45 |
| 4Ch | GPIO Pin Configuration | 0003h | 6.5.18; page 45 |
| 4Eh | GPIO Pin Polarity/Type | FFFFh | 6.5.19; page 46 |
| 50h | GPIO Pin Sticky | 0000h | 6.5.20; page 46 |
| 52h | GPIO Wake-up | 0000h | 6.5.21; page 47 |
| 54h | GPIO Pin Status | 0000h | 6.5.22; page 47 |
| 6Ah | Digital Audio Control | 0000h | 6.5.16; page 44 |
| 6Ch | Revision Code | 00xxh | 6.5.24; page 48 |
| 6Eh | Analog Special | 0000h | 6.5.25; page 48 |
| 70h | 72h Enable | 0000h | 6.5.25.6; page 50 |
| 72h | Analog Current Adjust | 0000h | 6.5.25.7; page 50 |
| 74h* | GPIO Current Access | 0000h | 6.5.26; page 51 |
| 76h | 78h Enable | 0000h | 6.5.27.1; page 51 |
| 78h | Clock Access | 0000h | 6.5.27.2; page 52 |
| 7Ch | Vendor ID1 | 8384h | 6.5.28.1; page 52 |
| 7Eh | Vendor ID2 | 76xxh | 6.5.28.2; page 52 |

* Register 74h is used for GPIO control in revision CA3.

6.5.1. Reset (00h)

Default: 6990h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|--------|-----|-----|-----|-----|-----|-----|-----|
| RSRVD4 | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 |

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part.

6.5.2. Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo LINE_OUT master volume (both right and left channels), register 04h controls the Headphone Out master volume, and register 06h controls the MONO volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at $-\infty$ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel. When bits D5 and D13 are set in any of these registers it automatically writes all 1 to the next lower 5-bits.

The default value is 8000h for registers 02h, 04h, and 06h, which corresponds to 0 dB attenuation with mute on.

Table 15. Play Master Volume Register

| Mute | Mx5...Mx0 | Function | Range |
|------|-----------|-------------------------|-------|
| 0 | 00 0000 | 0dB Attenuation | Req. |
| 0 | 01 1111 | 46.5 Attenuation | Req. |
| 1 | xx xxxx | ∞ dB Attenuation | Req. |

6.5.2.1. Master Volume (02h)

Default: 8000h

Note: If optional bits D13 & D5 of register 02h are set to 1, then the corresponding attenuation is set to 46.5dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------|-----|-----|-----|-----|-----|-----|
| Mute | RSRVD | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 |

6.5.2.2. Headphone Out Volume (04h)

Default: 8000h

Note: If optional bits D13 & D5 of register 04h are set to 1, then the corresponding attenuation is set to 46.5dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-------|------|------|------|------|------|------|
| Mute | RSRVD | HPL5 | HPL4 | HPL3 | HPL2 | HPL1 | HPL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | HPR5 | HPR4 | HPR3 | HPR2 | HPR1 | HPR0 |

6.5.2.3. Master Volume MONO (06h)

Default: 8000h

Note: If optional bit D5 of register 06h is set to 1, then the corresponding attenuation is set to 46.5dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | MM5 | MM4 | MM3 | MM2 | MM1 | MM0 |

6.5.3. PC Beep Mixer Volume (Index 0Ah)

Default: 0000h

Note: PC_BEEP defaults to 0000h, mute off.

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-------|
| Mute | Reserved | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | PV3 | PV2 | PV1 | PV0 | RSRVD |

This register controls the level for the PC Beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel is set at $-\infty$ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the STAC9750/9751 mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable, the PC_BEEP signal needs to reach the output jack at all times. NOTE: the PC_BEEP is routed to the mono outputs when the STAC9750/9751 is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet. The default value is 0000h, which corresponds to 0 dB attenuation with mute off.

Table 16. PC_BEEP Register

| Mute | PV3...PV0 | Function |
|------|-----------|-------------------------|
| 0 | 0000 | 0 dB Attenuation |
| 0 | 1111 | 45 dB Attenuation |
| 1 | xxxx | ∞ dB Attenuation |

6.5.4. Analog Mixer Input Gain Registers (Index 0Ch - 18h)

These registers control the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at $-\infty$ dB.

The default value for stereo registers is 8808h, corresponding to 0 dB gain with mute on.

Table 17. Analog Mixer Input Gain Register

| Mute | Gx4...Gx0 | Function |
|------|-----------|---------------|
| 0 | 0 0000 | +12 dB gain |
| 0 | 0 1000 | 0 dB gain |
| 0 | 1 1111 | -34.5 dB gain |

6.5.4.1. Phone Mixer Volume (0Ch)

Default: 8008h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | GN4 | GN3 | GN2 | GN1 | GN0 |

6.5.4.2. Mic Mixer Volume (0Eh)

Default: 8008h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-------|----------|-------|-----|-----|-----|-----|-----|
| Mute | Reserved | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RSRVD | BOOST_EN | RSRVD | GN4 | GN3 | GN2 | GN1 | GN0 |

Register 0Eh (Mic Volume Register) Bit D6 is the Mic boost enable. To select between 20dB or 30dB Mic Boost, see register 6Eh, D2 in section 6.5.25; page 48.

6.5.4.3. Line In Mixer Volume (10h)

Default: 8808h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | GL4 | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | GR4 | GR3 | GR2 | GR1 | GR0 |

6.5.4.4. CD Mixer Volume (12h)

Default: 8808h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | GL4 | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | GR4 | GR3 | GR2 | GR1 | GR0 |

6.5.4.5. Video Mixer Volume (14h)

Default: 8808h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | GL4 | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | GR4 | GR3 | GR2 | GR1 | GR0 |

6.5.4.6. AUX Mixer Volume (16h)

Default: 8808h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | GL4 | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | GR4 | GR3 | GR2 | GR1 | GR0 |

6.5.4.7. PCM Out Mixer Volume (18h)

Default: 8808h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | GL4 | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | GR4 | GR3 | GR2 | GR1 | GR0 |

6.5.5. Record Select (1Ah)

Default: 0000h (corresponding to Mic in)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|-----|-----|
| Reserved | | | | | SL2 | SL1 | SL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | SR2 | SR1 | SR0 |

Used to select the record source independently for right and left.

Table 18. Record Select Control Registers

| Bit(s) | Reset | Name | Description |
|--------|-------|----------|--|
| 15:11 | 0 | Reserved | Bits not used, should read back 0 |
| 10:8 | 0 | SL2:SL0 | Left Channel Input Select 000 = Mic 100 = Line In (left) 001 = CD In (left) 101 = Stereo Mix (left) 010 = Video In (left) 110 = Mono Mix 011 = Aux In (left) 111 = Phone |
| 7:3 | 0 | Reserved | Bits not used, should read back 0 |
| 2:0 | 0 | SR2:SR0 | Right Channel Input Select 000 = Mic 100 = Line In (right) 001 = CD In (right) 101 = Stereo Mix (right) 010 = Video In (right) 110 = Mono Mix 011 = Aux In (right) 111 = Phone |

6.5.6. Record Gain (1Ch)

Default: 8000h (corresponding to 0 dB gain with mute on)

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|-----|-----|-----|
| Mute | Reserved | | | GL3 | GL2 | GL1 | GL0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | GR3 | GR2 | GR1 | GR0 |

The 1Ch register adjusts the stereo input record gain. Each step corresponds to 1.5dB. 22.5dB corresponds to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at $-\infty$ dB.

Table 19. Record Gain Registers

| Mute | Gx3... Gx0 | Function |
|------|------------|----------------|
| 0 | 1111 | +22.5 dB gain |
| 0 | 0000 | 0 dB gain |
| 1 | xxxx | $-\infty$ gain |

6.5.7. General Purpose (20h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---------|----------|-----|----------|-----|-----|-----|----|
| POP BYP | RSRVD | 3D | Reserved | | | MIX | MS |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| LPBK | Reserved | | | | | | |

This register is used to control some miscellaneous functions. Below is a summary of each bit and its function. The MS bit controls the MIC selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-Link, allowing for full system performance measurements.

Table 20. General Purpose Register

| Bit | Function |
|---------|--|
| 3D | 3D Stereo Enhancement ON/OFF - 1 = on |
| MIX | Mono output select - 0 = Mix, 1 = Mic |
| MS | Mic select - 0 = Mic1, 1 = Mic2 |
| POP BYP | DAC bypasses mixer and connects directly to Line Out |
| LPBK | ADC/DAC loopback mode |

6.5.8. 3D Control (22h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----------|----|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | DP3 | DP2 | Reserved | |

This register is used to control the 3D stereo enhancement function, TSI Surround 3D (SS3D), built into the AC'97 component. Note that register bits DP3-DP2 are used to control the separation ratios in the 3D control for LINE_OUT. SS3D provides for a wider soundstage extending beyond the normal 2-speaker arrangement. Note that the 3D bit in the general purpose register (20h) must be set to 1 to enable SS3D functionality and for the bits in 22h to take effect.

Table 21. 3D Control Registers

| DP3, DP2 | LINE_OUT SEPARATION RATIO |
|----------|---------------------------|
| 0 0 | 0 (Off) |
| 0 1 | 3 (Low) |
| 1 0 | 4.5 (Med) |
| 1 1 | 6 (High) |

The three separation ratios are implemented as shown in Table 21. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during two-channel playback. The ratios provide for options to narrow or widen the soundstage.

6.5.9. Audio Interrupt (24h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|----------|-----|-----|----------|----|----|
| I4 | I3 | Reserved | | I0 | Reserved | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | | |

| Bit(s) | Reset Value | R/W | Name | Description |
|--------|-------------|-----|----------|--|
| 15 | 0 | RW | I4 | 0 = Interrupt is clear 1 = Interrupt is set Interrupt event is cleared by writing a 1 to this bit. The interrupt bit will change regardless of condition of interrupt enable (I0) status. An interrupt in the GPI in slot 12 in the AC-Link will follow this bit change when interrupt enable (I0) is unmasked. |
| 14 | 0 | RO | I3 | Interrupt Cause 0 = No Interrupt Caused 1 = Change in GPIO input status These bits will reflect the general cause of the first interrupt event generated. It should be read after interrupt status has been confirmed as interrupting. The information should be used to scan possible interrupting events in proper pages. |
| 13-12 | 0 | RW | Reserved | Bits not used, should read back 0 |
| 11 | 0 | RW | I0 | Interrupt Enable 0 = Interrupt generation is masked. 1 = Interrupt generation is un-masked. The driver should not un-mask the interrupt unless ensured by the AC '97 controller that no conflict is possible with modem slot 12 - GPI functionality. Some AC'97 2.2 compliant controllers do not support audio CODEC interrupt infrastructure. In either case, S/W should poll the interrupt status after initiating a sense cycle and wait for Sense Cycle Max Delay to determine if an interrupting event has occurred. |
| 10:0 | 0 | RO | Reserved | Bits not used, should read back 0 |

6.5.10. Powerdown Ctrl/Stat (26h)

Default: 000Fh

| | | | | | | | |
|------------|------------|------------|------------|------------|------------|-----------|-----------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | REF | ANL | DAC | ADC |

This read/write register is used to program power down states and monitor subsystem readiness. The EAPD external control is also supported through this register.

Table 22. Powerdown Status Registers

| Bit | Function |
|------|------------------------------------|
| EAPD | External Amplifier Power Down |
| REF | VREF's up to nominal level |
| ANL | Analog mixers, etc. ready |
| DAC | DAC section ready to playback data |
| ADC | ADC section ready to playback data |

6.5.10.1. Ready Status

The lower half of this register is read only status, a 1 indicating that the subsection is ready. Ready is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

When the AC-Link “CODEC Ready” indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready. When this register is written, the bit values that come in on AC-Link will have no effect on read only bits 0-7.

6.5.10.2. Powerdown Controls

The STAC9750/9751 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). See the section “Low Power Modes” for more information.

6.5.10.3. External Amplifier Power Down Control

The EAPD bit 15 of the Powerdown Control/Status Register (Index 26h) directly controls the output of the EAPD output (pin 45), and produces a logical 1 when this bit is set to logic high. This function is used to control an external audio amplifier power down. EAPD = 0 places approximately 0V on the output pin, enabling an external audio amplifier. EAPD = 1 places approximately DVdd on the output pin, disabling the external audio amplifier. Audio amplifiers that operate with reverse polarity will likely require an external inverter to maintain software driver compatibility.

6.5.11. Extended Audio ID (28h)

Default: 0605h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|----------|------|------|-------|------|------|
| ID1 | ID0 | Reserved | | REV1 | REV0 | AMAP | LDAC |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SDAC | CDAC | DSA1 | DSA0 | VRM | SPDIF | DRA | VRA |

The Extended Audio ID register is a read-only register, except for bits D5:D4. ID1 and ID0 echo the configuration of the CODEC as defined by the programming of pins 45 and 46 externally. A returned 00 defines the CODEC as the primary CODEC, while any other code identifies the CODEC as one of three secondary CODEC possibilities. SDAC = 0 tells the controller that the STAC9750/9751 is a two-channel CODEC as defined by the Intel specification. The AMAP bit, D9, will return a 1 indicating that the CODEC supports the optional “AC'97 2.2 compliant AC-link slot to audio DAC mappings”. The default condition assumes that 00 are loaded in the DSA0 and DSA1 bits of the Extended Audio ID (Index 28h). With 00 in the DSAx bits, the CODEC slot assignments are as per the AC'97 specification recommendations. If the DSAx bits do not contain 00, the slot assignments are as per the table in the section describing the Extended Audio ID (Index 28h). The VRA bit, D0, will return a 1 indicating that the CODEC supports the optional variable sample rate conversion as defined by the AC'97 specification.

Table 23. Extended Audio ID

| Bit | Name | Access | Reset Value | Function |
|-------|----------|-----------|-------------|---|
| 15:14 | ID [1:0] | Read only | variable | 00 = XTAL_OUT grounded (Note 1) CID1#, CID0# = XTAL_OUT crystal or floating |
| 13:12 | Reserved | Read only | 00 | Reserved |
| 11:10 | Rev[1:0] | Read only | 01 | Indicates CODEC is AC'97 Rev 2.2 compliant |
| 9 | AMAP | Read only | 1 | Multi-channel slot support (Always = 1) |
| 8 | LDAC | Read only | 0 | Low Frequency Effect, not supported (Always=0) |
| 7 | SDAC | Read only | 0 | Surround DAC, not supported (Always = 0) |
| 6 | CDAC | Read only | 0 | Center channel, not supported (Always = 0) |

Table 23. Extended Audio ID

| | | | | |
|-----|-----------|------------|----|---|
| 5:4 | DSA [1,0] | Read/Write | 00 | DAC slot assignment If CID[1:0] = 00 then DSA[1:0] resets to 00 If CID[1:0] = 01 then DSA[1:0] resets to 01 If CID[1:0] = 10 then DSA[1:0] resets to 01 If CID[1:0] = 11 then DSA[1:0] resets to 10 00 = left slot 3, right slot 4 01 = left slot 7, right slot 8 10 = left slot 6, right slot 9 11 = left slot 10, right slot 11 |
| 3 | VRM | Read only | 0 | Variable Sample Rate Mic, not supported (Always = 0) |
| 2 | SPDIF | Read only | 1 | 0 = SPDIF pulled high on reset, SPDIF disabled 1 = default, SPDIF enabled (Note 2) |
| 1 | DRA | Read only | 0 | Double Rate Audio, not supported (Always = 0) |
| 0 | VRA | Read only | 1 | Variable sample rates supported (Always = 1) |

1. External CID pin status (from analog) these bits are the logical inversion of the pin polarity (pin 45-46). These bits are zero if XTAL_OUT is grounded with an alternate external clock source in primary mode only. Secondary mode can either be through BIT CLK driven or 24 MHz clock driver with XTAL_OUT floating/shorted.
2. If pin 48 is held high at powerup, this bit will be held to zero, to indicate the SPDIF is not available. **PIN 48: TO ENABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLDOWN. TO DISABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLUP. DO NOT LEAVE PIN 48 FLOATING.**

6.5.12. Extended Audio Control/Status (2Ah)

Default: 0400h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-------|-------|-------|-------|----------|------------|
| Reserved | | | | | SPCV | Reserved | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | SPSA1 | SPSA0 | RSRVD | SPDIF | RSRVD | VRA enable |

6.5.12.1. Variable Rate Sampling Enable

The Extended Audio Status Control register also contains one active bit to enable or disable the Variable Sampling Rate capabilities of the DACs and ADCs. If the VRA, bit D0, is 1, the variable sample rate control registers (2Ch and 32h) are active, and “on-demand” slot data required transfers are allowed. If the VRA bit is 0, the DACs and ADCs will operate at the default 48 KHz data rate.

The STAC9750/9751 supports “on-demand” slot request flags. These flags are passed from the CODEC to the AC'97 controller in every audio input frame. Each time a slot request flag is set (active low) in a given audio frame, the controller will pass the next PCM sample for the corresponding slot in the audio frame that immediately follows. The VRA enable bit must be set to 1 to enable “on-demand” data transfers. If the VRA enable bit is not set, the CODEC will default to 48 KHz transfers and every audio frame will include an active slot request flag and data is transferred every frame.

For variable sample rate output, the CODEC examines its sample rate control registers, the state of the FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to

determine which SLOTREQ bits to set active (low). SLOTREQ bits are asserted during the current audio input frame for active output slots, which will require data in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the CODEC is always the master: for SDATA_IN (CODEC to controller), the CODEC sets the TAG bit; for SDATA_OUT (controller to CODEC), the CODEC sets the SLOTREQ bit and then checks for the TAG bit in the next frame. Whenever VRA is set to 0, the PCM rate registers (2Ch and 32h) are overwritten with BB80h (48 KHz).

6.5.12.2. SPDIF

The SPDIF bit in the Extended Audio Status Control Register is used to enable and disable the SPDIF functionality within the STAC9750/9751. If the SPDIF is set to a 1, then the function is enabled and when set to a 0 it is disabled.

6.5.12.3. SPCV (SPDIF Configuration Valid)

The SPCV bit is read only and indicates whether or not the SPDIF system is set up correctly. When SPCV is a 0, it indicates the system configuration is invalid and valid if it is a 1.

6.5.12.4. SPSA1, SPSA0 (SPDIF Slot Assignment)

SPSA1 and SPSA0 combine to provide the slot assignments for the SPDIF data. The following details the slot assignment relationship between SPSA1 and SPSA0.

Table 24. Slot assignment relationship between SPSA1 and SPSA0

| SPSA[1,0] | Slot Assignment | Comments |
|-----------|-----------------|-----------------------------------|
| 00 | 3 & 4 | SPDIF source data slot assignment |
| 01 | 7 & 8 | 2-channel CODEC primary default |
| 10 | 6 & 9 | 4-channel CODEC primary default |
| 11 | 10 & 11 | 6-channel CODEC primary default |

The STAC9750/9751 are AMAP compliant with the following table.

Table 25. STAC9750/9751 AMAP compliant

| CODEC ID | Function | SPSA = 00 | SPSA = 01 | SPSA = 10 | SPSA = 11 |
|----------|------------------------------|-----------|-----------|-----------|-----------|
| 00 | 2-channel Primary w/SPDIF | 3 & 4 | 7 & 8* | 6 & 9 | 10 & 11 |
| 01 | 2-channel Dock CODEC w/SPDIF | 3 & 4 | 7 & 8 | 6 & 9* | 10 & 11 |
| 10 | +2-channel Surr w/ SPDIF | 3 & 4 | 7 & 8 | 6 & 9* | 10 & 11 |
| 11 | +2-channel Cntr/LFE w/ SPDIF | 3 & 4 | 7 & 8 | 6 & 9 | 10 & 11* |

Note: * is the default slot assignment

6.5.13. PCM DAC Rate Registers (2Ch and 32h)

The internal sample rate for the DACs and ADCs are controlled by the value in these read/write registers that contain a 16-bit unsigned value between 0 and 65535 representing the conversion rate in Hertz (Hz). In VRA mode (register 2Ah bit D0 = 1), if the value written to these registers is supported, that value will be echoed back when read, otherwise the closest (higher in the case of a tie) sample rate is supported and returned. Per PC 99 / PC 2001 specification, independent sample rates are

supported for record and playback. Whenever VRA is set to 0, the PCM rate registers (2Ch and 32h) will read back with BB80h (48 KHz).

Table 26. Hardware Supported Sample Rates

| Sample Rate | SR15-SR0 Value |
|-------------|----------------|
| 8 KHz | 1F40h |
| 11.025 KHz | 2B11h |
| 16 KHz | 3E80h |
| 22.05 KHz | 5622h |
| 32 KHz | 7D00h |
| 44.1 KHz | AC44h |
| 48 KHz | BB80h |

6.5.14. PCM DAC Rate (2Ch)

Default: BB80h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |

6.5.15. PCM LR ADC Rate (32h)

Default: BB80h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 |

6.5.16. SPDIF Control (3Ah)

Default: 2A00h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-------|-------|-----|------|------------|-----|
| #V | DRS | SPSR1 | SPSR2 | L | CC6 | CC5 | CC4 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CC3 | CC2 | CC1 | CC0 | PRE | COPY | #PCM/AUDIO | PRO |

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or sub-frame in the V case). With exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit register 2 Ah is 0). This ensures that control and status information start up correctly at the beginning of SPDIF transmission. The default is 2A00h which sets the SPDIF output sample rate at 48 KHz and the normal SPDIF expectations.

1. If pin 48 is held high at powerup, 28h D2 will be low indicating no SPDIF available and the register 3Ah will then read back 0000h. **PIN 48: TO ENABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLDOWN. TO DISABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLUP. DO NOT LEAVE PIN 48 FLOATING.**
2. Bits D15, D13-D00 of this register cannot be written to without first setting Reg 2Ah bit D2 = 0 (SPDIF disabled) and Register 28h bit D2 = 1 (SPDIF available).

Table 27. SPDIF Control

| Bit(s) | Reset | Access | Name | Description (note 1-2) |
|--------|-------|--------------|-----------|---|
| 15 | 0 | Read & Write | #V | Validity bit is set indicating each sub-frame's samples are invalid. If #V is 0, then it indicates that each sub-frame was transmitted and received correctly by the interface. |
| 14 | 0 | Read Only | DRS | 1 = Double Rate SPDIF support (always = 0) |
| 13:12 | 10 | Read & Write | SPSR[1,0] | SPDIF Sample Rate. 00 44.1 KHz Rate 01 Reserved 10 48 KHz Rate (default) 11 32 KHz Rate |
| 11 | 0 | Read & Write | L | Generation Level is defined by the IEC standard, or as appropriate. (Always = 1) |
| 10:4 | 0 | Read & Write | CC[6, 0] | Category Code is defined by the IEC standard or as appropriate by media. |
| 3 | 0 | Read & Write | PRE | 0 = 0 μ sec Pre-emphasis 1 = Pre-emphasis is 50/15 μ sec |
| 2 | 0 | Read & Write | COPY | 0 = Copyright not asserted 1 = Copyright is asserted |
| 1 | 0 | Read & Write | /AUDIO | 0 = PCM data 1 = Non-Audio or non-PCM format |
| 0 | 0 | Read & Write | PRO | 0 = Consumer use of the channel 1 = Professional use of the channel |

6.5.17. Extended Modem Status and Control Register (3Eh)

Default: 0100h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----|------|
| Reserved | | | | | | | PRA |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | | GPIO |

Table 28. Extended Modem Status and Control

| Bit(s) | Access | Reset Value | Name | Description |
|--------|--------------|-------------|----------|---|
| 15:9 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 8 | Read / Write | 1 | PRA | 0 = GPIO powered up / enabled 1 = GPIO powered down / disabled |
| 7:1 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 0 | Read Only | 0 | GPIO | 0 = GPIO not ready (powered down) 1 = GPIO ready (powered up) |

6.5.18. GPIO Pin Configuration Register (4Ch)

Default: 0003h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----------------|----------------|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | GC1 (GPIO1) | GC0 (GPIO0) |

Table 29. GPIO Pin Configuration Register

| Bit(s) | Access | Reset Value | Name | Description |
|--------|--------------|-------------|----------|---|
| 15:2 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 1 | Read / Write | 1 | GC1 | 0 = GPIO1 configured as output 1 = GPIO1 configured as input |
| 0 | Read / Write | 1 | GC0 | 0 = GPIO0 configured as output 1 = GPIO0 configured as input |

6.5.19. GPIO Pin Polarity/Type Register (4Eh)

Default: FFFFh

| | | | | | | | |
|----------|-----|-----|-----|-----|-----|----------------|----------------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | GP1 (GPIO1) | GP0 (GPIO0) |

Table 30. GPIO Pin Polarity/Type Register

| Bit(s) | Access | Reset Value | Name | Description |
|--------|--------------|-------------|----------|--|
| 15:2 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 1 | Read / Write | 1 | GP1 | 0 = GPIO1 Input Polarity Inverted, CMOS output drive. 1 = GPIO1 Input Polarity Non-inverted, Open-Drain output drive. |
| 0 | Read / Write | 1 | GP0 | 0 = GPIO0 Input Polarity Inverted, CMOS output drive. 1 = GPIO0 Input Polarity Non-inverted, Open-Drain output drive. |

6.5.20. GPIO Pin Sticky Register (50h)

Default: 0000h

| | | | | | | | |
|----------|-----|-----|-----|-----|-----|----------------|----------------|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | GS1 (GPIO1) | GS0 (GPIO0) |

Table 31. GPIO Pin Sticky Register

| Bit(s) | Access | Reset Value | Name | Description |
|--------|--------------|-------------|----------|--|
| 15:2 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 1 | Read / Write | 0 | GS1 | 0 = GPIO1 Non Sticky configuration. 1 = GPIO1 Sticky configuration. |
| 0 | Read / Write | 0 | GS0 | 0 = GPIO0 Non Sticky configuration. 1 = GPIO0 Sticky configuration. |

6.5.21. GPIO Pin Mask Register (52h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----------------|----------------|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | GW1 (GPIO1) | GW0 (GPIO0) |

Table 32. GPIO Pin Mask Register

| Bit(s) | Access | Reset Value | Name | Description |
|--------|--------------|-------------|----------|---|
| 15:2 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 1 | Read / Write | 0 | GW1 | 0 = GPIO1 interrupt not passed to GPIO_INT slot 12. 1 = GPIO1 interrupt is passed to GPIO_INT slot 12. |
| 0 | Read / Write | 0 | GW0 | 0 = GPIO0 interrupt not passed to GPIO_INT slot 12. 1 = GPIO0 interrupt is passed to GPIO_INT slot 12. |

6.5.22. GPIO Pin Status Register (54h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----------------|----------------|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | GI1 (GPIO1) | GI0 (GPIO0) |

Table 33. GPIO Pin Status Register

| Bit(s) | Access | Reset Value | Name | Description |
|--------|--------------|-------------|----------|--|
| 15:2 | Read Only | 0 | Reserved | Bit not used, should read back 0 |
| 1 | Read / Write | x | GI1 | When GPIO1 is configured as output and Register 74h bit[0] = 0 (default), the value of this register will be placed on the GPIO1 pad. When GPIO1 is configured as output and Register 74h bit[0] = 1, the GPIO1 pad will get its value from slot12. When GPIO1 is configured as input and configured as a sticky writing a 1 does nothing, writing a 0 clears this bit. When GPIO1 is configured as input this register reflects the value on the GPIO1 pad after interpretation of the polarity and sticky configurations. |
| 0 | Read / Write | x | GI0 | When GPIO0 is configured as output and Register 74h bit[0] = 0 (default), the value of this register will be placed on the GPIO0 pad. When GPIO0 is configured as output and Register 74h bit[0] = 1, the GPIO0 pad will get its value from slot12. When GPIO0 is configured as input and configured as a sticky writing a 1 does nothing, writing a 0 clears this bit. When GPIO0 is configured as input this register reflects the value on the GPIO0 pad after interpretation of the polarity and sticky configurations. |

6.5.23. Digital Audio Control (6Ah)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|-----|-----|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | DO1 | DO0 |

Table 34. Digital Audio Control Register

| Bit(s) | Reset | Name | Description |
|--------|-------|----------|--|
| 15:2 | 0 | Reserved | Bits not used, should read back 0 |
| 1 | 0 | DO1 | SPDIF Digital Output Source Selection: DO1 = 0; PCM data from the AC-Link to SPDIF DO1 = 1; ADC record data to SPDIF |
| 0 | 0 | DO0 | Always reads zero |

This read/write register is used to program the digital mixer input status. In the default state, the PCM DAC path is enabled and the ADC record inputs are disabled.

The DO1 and DO0 bits control the input source for the PCM to digital output converters. The table describes the available options.

6.5.24. Revision Code (6Ch)

Default: 00xxh

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The device Revision Code register (index 6Ch) contains a software readable revision-specific code used to identify performance, architectural, or software differences between various device revisions. Bits 7:0 of the Revision Code register are user readable; bits 15:8 are not used at this time and will return zeros when read. This value can be used by the audio driver, or miniport driver in the case of WIN98® WDM approaches, to adjust software functionality to match the feature-set of the STAC9750/9751. This will allow the software driver to identify any required operational differences between the existing STAC9750/9751 and future versions.

6.5.25. Analog Special (6Eh)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|---------------------|---------|--------------|----------|-----------|------------|----------------|
| Reserved | | | AC97 ALL MIX | Reserved | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| RSVD | MUTE FIX DISABLE | ADCSLT1 | ADCSLT0 | Reserved | 20/30 SEL | SPLYOVR EN | SPLYOVR VAL |

The Analog Special register has several bits used to control various functions specific to the STAC9750/9751.

6.5.25.1. ALL MIX

The AC'97 ALL_MIX, bit D12 of register 6Eh, controls the record source when the Stereo Mix option is selected for recording. If the AC'97 mode is default logic 1, the "Stereo Mix Record" option will include the sum of the analog sources with or without 3D enhancement, and the main PCM DAC output. If the "ALL Analog Record" option is selected, the Stereo Mix Record option will include the sum of the analog sources only, with or without 3D enhancement. The "AC'97 mode" is useful for recording all sound sources. The "ALL Analog Record" mode is useful in conjunction with the POP BYPASS mode for recording all analog sources, which are often further processed and combined with other PCM data to be output directly to the DAC outputs which are configured in POP_BYPASS mode using the General Purpose register (index 20h).

6.5.25.2. ADC Data on AC LINK

Bits D5-D4 select slots for ADC data on ACLINK.

Table 35. ADC data on AC LINK

| Value | Function |
|-------|-----------------------------|
| 00 | left slot 3, right slot 4 |
| 01 | left slot 7, right slot 8 |
| 10 | left slot 6, right slot 9 |
| 11 | left slot 10, right slot 11 |

6.5.25.3. MuteFix Disable

Bit D6 controls the enable and disable of the MuteFix functions.

- 0 = MUTE FIX Enabled
- 1 = MUTE FIX Disabled

When this bit is zero, and either channel is set to -46.5dB attenuation (1Fh), then that channel is fully muted. When this bit is one, then operation is per AC'97 specification.

This bit is reserved in revisions prior to CC1.

6.5.25.4. Mic Boost Select

The Mic boost value can be selected with bit D2, which is enabled by Register 0Eh, bit D6. Writing a zero to bit D2 will provide 20dB of Mic Boost. Writing a one will provide 30dB of Mic Boost.

Table 36. Mic Boost Select

| Value | Function |
|-------|----------|
| 0 | 20dB |
| 1 | 30dB |

6.5.25.5. Supply Override Select

The Supply Override bit, D1, allows override of the supply detect. Writing a zero disables the override on supply detect. Writing a one, overrides supply detect with bit D0. Bit D0 provides the supply override value. A zero forces 3.3 V analog operation and one forces 5 V analog operation.

6.5.25.6. 72h Enable (70h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 |

6.5.25.7. Analog Current Adjust (72h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-----|-----|-----|--------|--------|------|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| INT APOP | Reserved | | | | IBIAS1 | IBIAS0 | RSVD |

The Analog Current Adjust register (index 72h) is a locked register and can only be properly written and read from when ABBAh has been written into register 70h. The IBIASx bits allow the analog current to be adjusted with minimal reduction in performance. A lower analog current setting is NOT recommended when a 5V analog supply is used. A lower setting for 3.3V supplies is recommended for notebook computers to reduce power consumption to its lowest level.

Table 37. Analog Current Adjust

| IBIAS1 | IBIAS0 | Analog Current |
|--------|--------|--------------------------------|
| 0 | 0 | Normal Current |
| 0 | 1 | 80% of nominal Analog Current |
| 1 | 0 | 120% of nominal Analog Current |
| 1 | 1 | 140% of nominal Analog Current |

6.5.25.8. Internal Power-On/Off Anti-Pop Circuit

The STAC9750/9751 includes an internal power supply anti-pop circuit that prevents audible clicks and pops from being heard when the CODEC is powered on and off. This function is accomplished by delaying the charge/discharge of the VREF capacitor (Pin 27). C_{VREF} value of 1 μ F will cause a turn-on delay of roughly 3 seconds, which will allow the power supplies to stabilize before the CODEC outputs are enabled. The delay can be extended to 30 seconds if a value of C_{VREF} value of 10 μ F is used. The CODEC outputs are also kept stable for the same amount of time at power-off to allow the system to be gracefully turned off. The INT_APOP bit D7 of register 72h allows this delay circuit to be bypassed for rapid production testing. Any external component anti-pop circuit is unaffected by the internal circuit.

6.5.26. GPIO Access Register (74h)

Default: 0800h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|----------|-------|-------|----------|----------|-----------|-----------|
| EAPD | Reserved | GPIO1 | GPIO0 | EAPD_OEN | Reserved | GPIO1_OEN | GPIO0_OEN |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | | |

Table 38. GPIO Access Registers (74h)

| Bit(s) | Reset Value | Name | Description |
|--------|-------------|-----------|---|
| 15 | 0 | EAPD | EAPD data output on EAPD when bit D11 = 1 EAPD data input from pin when bit D11 = 0 |
| 14 | 0 | Reserved | Reserved |
| 13 | 0 | GPIO1 | GPIO1 data output on GPIO1 when bit D9 = 1 GPIO1 data input from pin when bit D9 = 0 |
| 12 | 0 | GPIO0 | GPIO0 data output on GPIO0 when bit D8 = 1 GPIO0 data input from pin when bit D8 = 0 |
| 11 | 1 | EAPD_OEN | 0 = EAPD data out disabled 1 = EAPD data output enabled |
| 10 | 0 | Reserved | Reserved |
| 9 | 0 | GPIO1_OEN | 0 = GPIO1 data out disabled 1 = GPIO1 data output enabled |
| 8 | 0 | GPIO0_OEN | 0 = GPIO0 data out disabled 1 = GPIO0 data output enabled |
| 7:0 | 0 | Reserved | Reserved |

The GPIO Access Register requires that the output enable bits (D11, D9 and D8) be used in conjunction with the data source selection (input or output) for the EAPD, GPIO0 and GPIO1 (pins 47, 43 and 44 respectively). For example, to use GPIO1 as an output, set D9 = 1 to enable the output, and use D13 to write the output value desired. To use GPIO1 as an input, set D9 = 0 to disable the output, and use D13 to read the input value.

6.5.27. High Pass Filter Bypass (Index 76h and 78h)

The High Pass Filter Bypass register (index 78h) is a locked register and can only be properly written and read from when ABBAh has been written into register 76h. Bit D0 controls the High Pass Filter Bypass. Default is zero which provides for normal operation where the high pass filter is active. Writing a one, will disable, or bypass the ADC high pass filter.

6.5.27.1. 78h Enable (76h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|------|------|------|------|------|------|-----|-----|
| EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 |

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6.5.27.2. ADC High Pass Filter Bypass(78h)

Default: 0000h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|----------|-----|-----|-----|-----|-----|----|-------------|
| Reserved | | | | | | | |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Reserved | | | | | | | ADC HPF BYP |

6.5.28. Vendor ID1 and ID2 (Index 7Ch and 7Eh)

These two registers contain four 8-bit ID codes. The first three codes have been assigned by Microsoft using their Plug and Play Vendor ID methodology. The fourth code is an TSI assigned code identifying the STAC9750/9751. The ID1 register (index 7Ch) contains the value 8384h, which is the first (83h) and second (84h) characters of the Microsoft ID code. The ID2 register (index 7Eh) contains the value 7650h, which is the third (76h) of the Microsoft ID code, and 50h which is the STAC9750/9751 ID code.

Note: The lower half of the Vendor ID2 register (index 7Eh) currently contains the value xxh identifying the STAC9750/9751. This value can be used by the audio driver, or miniport driver in the case of WIN98®, to adjust software functionality to match the feature-set of the STAC9750/9751. This portion of the register will likely contain different values if the software profile of the STAC9750/9751 changes, as in the case of silicon level device modifications. This will allow the software driver to identify any required operational differences between the existing STAC9750/9751 and any future versions.

6.5.28.1. Vendor ID1 (7Ch)

Default: 8384h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

6.5.28.2. Vendor ID2 76xx (7Eh)

Default: 7650h

| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|-----|-----|-----|-----|-----|-----|----|----|
| 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

7. LOW POWER MODES

The STAC9750/9751 is capable of operating at reduced power when no activity is required. The state of power-down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. The power down options are listed in Table 39. The first three bits, PR0..PR2, can be used individually or in combination with each other, and control power distribution to the ADCs, DACs and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR0, PR1, and PR2. PR3 essentially removes power from all analog sections of the CODEC, and is generally only asserted when the CODEC will not be needed for long periods. PR0 and PR1 control the PCM ADCs and DACs only. PR2 and PR3 do not need to be “set” before a PR4, but PR0 and PR1 must be “set” before PR4. PR5 disables the internal CODEC clock and requires an external cold reset for recovery. PR6 disables the headphone driver amplifier for additional analog power saving.

Table 39. Low Power Modes

| GRP Bits | Function |
|----------|---|
| PR0 | PCM in ADCs & Input Mux Powerdown |
| PR1 | PCM out DACs Powerdown |
| PR2 | Analog Mixer power down (VREF still on) |
| PR3 | Analog Mixer power down (VREF off) |
| PR4 | Digital Interface (AC-Link) power down (external clock off) |
| PR5 | Internal Clock disable |
| PR6 | Powerdown HEADPHONE_OUT |

The Figure 19 illustrates one example procedure to do a complete power down of STAC9750/9751. From normal operation, sequential writes to the Powerdown Register are performed to power down STAC9750/9751 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-Link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-Link (resetting PR4 to zero). The STAC9750/9751 can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states. When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

Figure 19. Example of STAC9750/9751 Powerdown/Powerup Flow

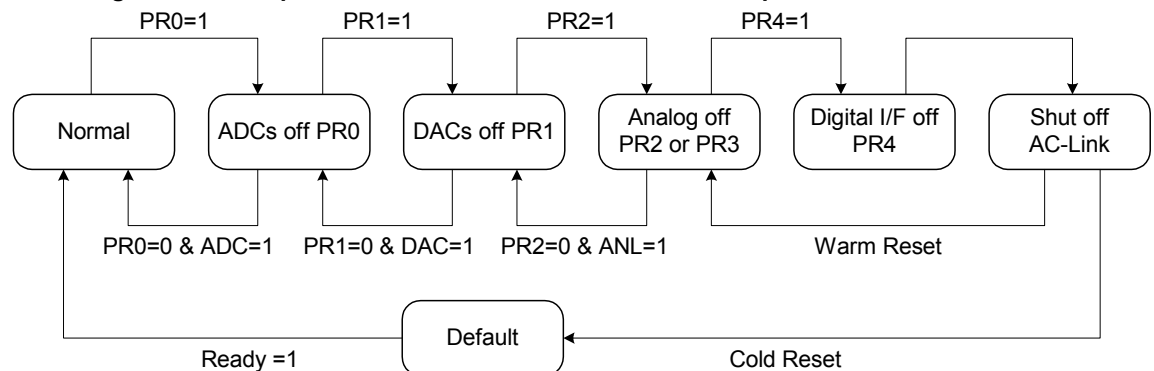
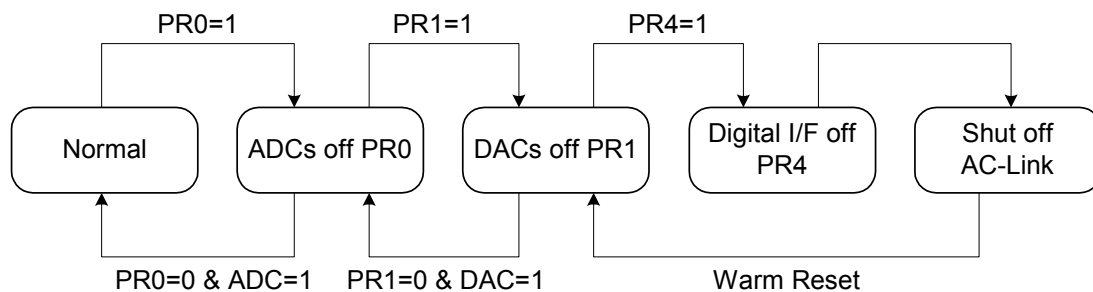


Figure 20 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through STAC9750/9751 to the speakers, while most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

Figure 20. STAC9750/9751 Powerdown/Powerup Flow With Analog Still Active

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8. MULTIPLE CODEC SUPPORT

The STAC9750/9751 provides support for the multi-CODEC option according to the Intel AC'97, rev 2.2 specification. By definition there can be only one Primary CODEC (CODEC ID 00) and up to three Secondary CODECs (CODEC IDs 01, 10, and 11). The CODEC ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

8.1. Primary/Secondary CODEC Selection

In a multi-CODEC environment the CODEC ID is provided by external programming of pins 45 and 46 (CID0 and CID1). The CID pin electrical function is logically inverted from the CODEC ID designation. The corresponding pin state and its associated CODEC ID are listed in the "CODEC ID Selection" table. Also see slot assignment discussion, "Multi-Channel Programming Register (Index 74)".

Table 40. CODEC ID Selection

| CID1 State | CID0 State | CODEC ID | CODEC Status |
|------------------|------------------|----------|--------------|
| DVdd or floating | DVdd or floating | 00 | Primary |
| DVdd or floating | 0 V | 01 | Secondary |
| 0 V | DVdd or floating | 10 | Secondary |
| 0 V | 0 V | 11 | Secondary |

8.1.1. Primary CODEC Operation

As a Primary device the STAC9750/9751 is completely compatible with existing AC'97 definitions and extensions. Primary CODEC registers are accessed exactly as defined in the AC'97 Component Specification and AC'97 Extensions. The STAC9750/9751 operates as Primary by default, and the external ID pins (45 and 46), have internal pull-ups so that these pins may be left as no-connects for primary operation.

When used as the Primary CODEC, the STAC9750/9751 generates the master AC-Link BIT_CLK for both the AC'97 Digital Controller and any Secondary CODECs. The STAC9750/9751 can support up to four loads of 10 K Ω and 50 pF on the BIT_CLK line. This is to ensure that implementations of up to four CODECs will not load down the clock output.

8.1.2. Secondary CODEC Operation

When the STAC9750/9751 is configured as a Secondary device the BIT_CLK pin is configured as an input at power up. Using the BIT_CLK provided by the Primary CODEC insures that everything on the AC-Link will be synchronous. As a Secondary device it can be defined as CODEC ID 01, 10 or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

8.2. Secondary CODEC Register Access Definitions

The AC'97 Digital Controller can independently access Primary and Secondary CODEC registers by using a 2-bit CODEC ID field (chip select) which is defined as the LSBs of Output Slot 0. For Secondary CODEC access, the AC'97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the CODEC ID field (Slot 0, bits 1 and 0).

As a Secondary CODEC, the STAC9750/9751 will disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when it sees a 2-bit CODEC ID value (Slot 0, bits 1 and 0) that matches its configuration. In a sense the Secondary CODEC ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary CODECs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary CODEC ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary CODEC ID bits are set.

This method is designed to be backward compatible with existing AC'97 controllers and CODECs. There is no change to output Slot 1 or 2 definitions.

Table 41. Secondary CODEC Register Access Slot 0 Bit Definitions

| Output Tag Slot (16-bits) | |
|---------------------------|---|
| Bit | Description |
| 15 | Frame Valid |
| 14 | Slot 1 Valid Command Address bit († Primary CODEC only) |
| 13 | Slot 2 Valid Command Data bit († Primary CODEC only) |
| 12-3 | Slot 3-12 Valid bits as defined by AC'97 |
| 2 | Reserved (Set to 0) |
| †1-0 | 2-bit CODEC ID field (00 Reserved for Primary; 01, 10, 11 indicate Secondary) |

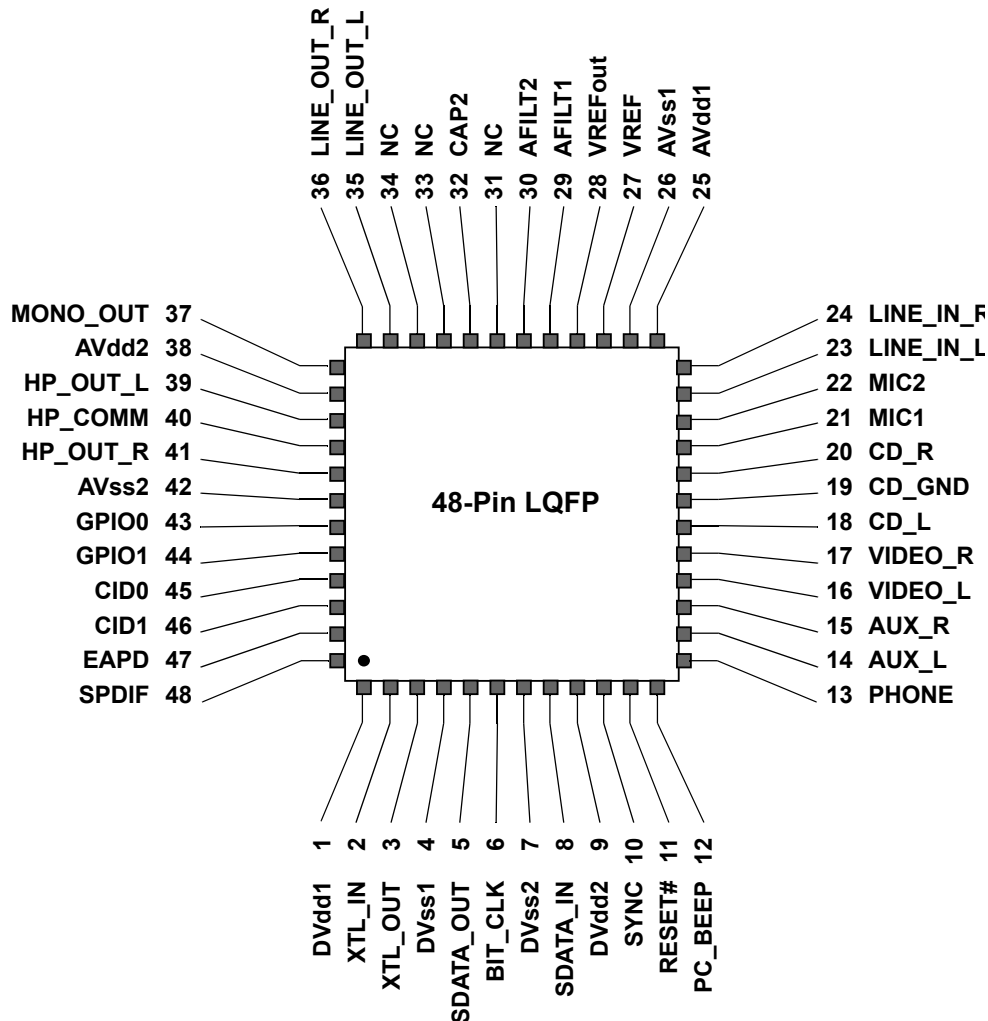
Note: † New definitions for Secondary CODEC Register Access

9. TESTABILITY

The STAC9750/9751 has two test modes. One is for ATE in-circuit test and the other is restricted for TSI's internal use. STAC9750/9751 enters the ATE in-circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-Link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. Use of the ATE test mode is the recommended means of removing the CODEC from the AC-Link when another CODEC is to be used as the primary. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the STAC9750/9751 must be issued another RESET# with all AC-link signals held low to return to the normal operating mode.

10. PIN DESCRIPTION

Figure 21. STAC9750/9751 Pin Description Drawing

**PIN 48:**

TO ENABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLDOWN.

TO DISABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLUP.

DO NOT LEAVE PIN 48 FLOATING.

The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect

10.1. Digital I/O

These signals connect the STAC9750/9751 to its AC'97 controller counterpart, an external crystal, multi-CODEC selection and external audio amplifier.

Table 42. Digital Connection Signals

| Pin Name | Pin # | Type | Description |
|-----------|-------|------|--|
| XTL_IN | 2 | I | 24.576 MHz Crystal or External Clock Source |
| XTL_OUT | 3 | I/O | 24.576 MHz Crystal or ground if external clock source connected to XTAL_IN |
| SDATA_OUT | 5 | I | Serial, time division multiplexed, AC'97 input stream |
| BIT_CLK | 6 | I/O | 12.288 MHz serial data clock |
| SDATA_IN | 8 | O | Serial, time division multiplexed, AC'97 output stream |
| SYNC | 10 | I | 48 KHz fixed rate sample sync |
| RESET# | 11 | I | AC'97 Master H/W Reset |
| NC | 31 | I/O | No Connect |
| NC | 33 | I/O | No Connect |
| NC | 34 | I/O | No Connect |
| GPIO0 | 43 | I/O | General Purpose I/O |
| GPIO1 | 44 | I/O | General Purpose I/O |
| CID0 | 45 | I | Multi-CODEC ID select - bit 0 |
| CID1 | 46 | I | Multi-CODEC ID select - bit 1 |
| EAPD | 47 | I/O | External Amplifier Power Down |
| SPDIF | 48 | O | SPDIF digital output PIN 48: - TO ENABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLDOWN. TO DISABLE SPDIF, USE AN 1 K Ω -10 K Ω EXTERNAL PULLUP. DO NOT LEAVE PIN 48 FLOATING. |

10.2. Analog I/O

These signals connect the STAC9750/9751 to analog sources and sinks, including microphones and speakers.

Table 43. Analog Connection Signals

| Pin Name | Pin # | Type | Description |
|------------|-------|------|--|
| PC-BEEP | 12 | I* | PC Speaker beep pass-through |
| PHONE | 13 | I* | From telephony subsystem speakerphone (or DLP - Down Line Phone) |
| AUX_L | 14 | I* | Aux Left Channel |
| AUX_R | 15 | I* | Aux Right Channel |
| VIDEO_L | 16 | I* | Video Audio Left Channel |
| VIDEO_R | 17 | I* | Video Audio Right Channel |
| CD_L | 18 | I* | CD Audio Left Channel |
| CD_GND | 19 | I* | CD Audio analog signal return [†] |
| CD_R | 20 | I* | CD Audio Right Channel |
| MIC1 | 21 | I* | Desktop Microphone Input |
| MIC2 | 22 | I* | Second Microphone Input |
| LINE_IN_L | 23 | I* | Line In Left Channel |
| LINE_IN_R | 24 | I* | Line In Right Channel |
| LINE_OUT_L | 35 | O | Line Out Left Channel |
| LINE_OUT_R | 36 | O | Line Out Right Channel |
| MONO_OUT | 37 | O | To telephony subsystem speakerphone (or DLP - Down Line Phone) |
| HP_OUT_L | 39 | O | Headphone Out Left Channel |
| HP_COMM | 40 | O | Headphone Ground Return |
| HP_OUT_R | 41 | O | Headphone Out Right Channel |

* any unused input pins should be tied together through a capacitor (0.1 μ F suggested) to ground, except the MIC inputs which should have their own capacitor to ground if not used.

[†]The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5 V. The name of the pin in the AC'97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect

10.3. Filter/References/GPIO

These signals are connected to resistors, capacitors, specific voltages, or provide General Purpose I/O.

Table 44. Filtering and Voltage References

| Signal Name | Pin Number | Type | Description |
|-------------|------------|------|--|
| VREF | 27 | O | Analog ground ($0.45 * V_{dd}$, at 5 V; $0.41 * V_{dd}$ at 3 V) |
| VREFOUT | 28 | O | Reference Voltage out 5 mA drive (intended for MIC bias) ($\sim V_{dd}/2$) |
| AFILT1 | 29 | O | Anti-Aliasing Filter Cap - ADC left channel |
| AFILT2 | 30 | O | Anti-Aliasing Filter Cap - ADC right channel |
| CAP2 | 32 | O | ADC reference Cap |

10.4. Power and Ground Signals

Table 45. Power and Ground Signals

| Pin Name | Pin # | Type | Description |
|----------|-------|------|--|
| AVdd1 | 25 | I | Analog Vdd = 5.0 V or 3.3 V |
| AVdd2 | 38 | I | Analog Vdd = 5.0 V or 3.3 V (headphone power source) |
| AVss1 | 26 | I | Analog Gnd |
| AVss2 | 42 | I | Analog Gnd |
| DVdd1 | 1 | I | Digital Vdd = 3.3 V |
| DVdd2 | 9 | I | Digital Vdd = 3.3 V |
| DVss1 | 4 | I | Digital Gnd |
| DVss2 | 7 | I | Digital Gnd |

11. ORDERING INFORMATION**Ordering Information**

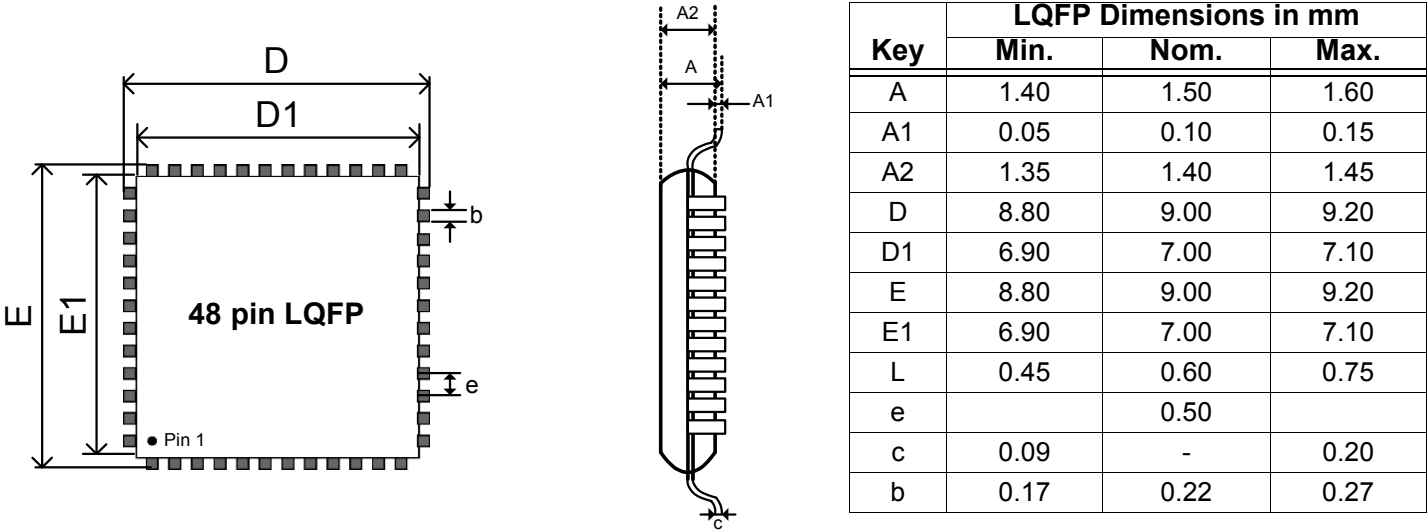
| Part Number | Package | Temp Range | Supply Range |
|------------------|------------------------------------|----------------|--------------------------|
| STAC9750XXTAEyyX | 48-pin RoHS LQFP 7mm x 7mm x 1.4mm | 0° C to +70° C | DVdd = 3.3V, AVdd = 5.0V |
| STAC9751XXTAEyyX | 48-pin RoHS LQFP 7mm x 7mm x 1.4mm | 0° C to +70° C | DVdd = 3.3V, AVdd = 3.3V |

NOTE: When ordering these parts the “yy” will be replaced with the CODEC revision. Add an “R” to the end of any of these part numbers for delivery on Tape and Reel. The minimum order quantity for Tape and Reel is 2,000 units.

12. PACKAGE DRAWINGS

12.1. 48-Pin LQFP

Figure 22. Package Drawing - 48-pin LQFP



13. SOLDER REFLOW PROFILE

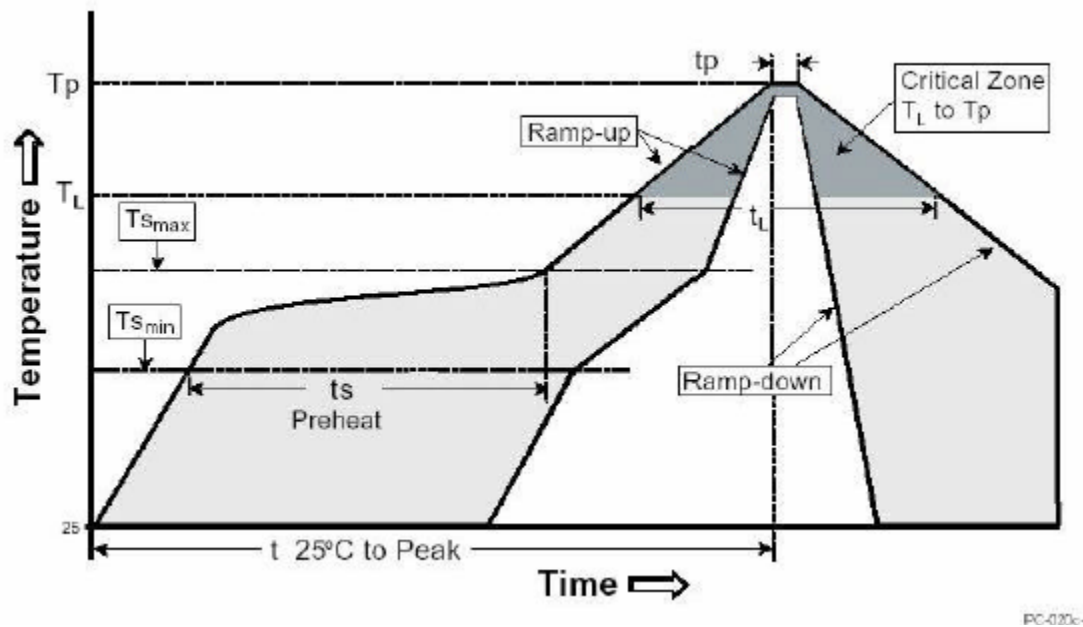
13.1. Standard Reflow Profile Data

Note: These devices can be hand soldered at 360 °C for 3 to 5 seconds.

FROM: IPC / JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices” (www.jedec.org/download).

| Profile Feature | | Pb Free Assembly |
|---|--------------------------------------|--|
| Average Ramp-Up Rate ($T_{s_{max}} - T_p$) | | 3 °C / second max |
| Preheat | Temperature Min ($T_{s_{min}}$) | 150 °C |
| | Temperature Max ($T_{s_{max}}$) | 200 °C |
| | Time ($t_{s_{min}} - t_{s_{max}}$) | 60 - 180 seconds |
| Time maintained above | Temperature (T_L) | 217 °C |
| | Time (t_L) | 60 - 150 seconds |
| Peak / Classification Temperature (T_p) | | See “Package Classification Reflow Temperatures” on page 64. |
| Time within 5 °C of actual Peak Temperature (t_p) | | 20 - 40 seconds |
| Ramp-Down rate | | 6 °C / second max |
| Time 25 °C to Peak Temperature | | 8 minutes max |
| Note: All temperatures refer to topside of the package, measured on the package body surface. | | |

Figure 23. Reflow Profile



13.2. Pb Free Process - Package Classification Reflow Temperatures

| Package Type | MSL | Reflow Temperature |
|--------------|-----|--------------------|
| LQFP 48-pin | 3 | 260 °C* |

14. APPENDIX A: SPLIT INDEPENDENT POWER SUPPLY OPERATION

In PC applications, one power supply input to the STAC9750/9751 may be derived from a supply regulator (as shown in Figure 24) and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's CODECs would be subject to on-chip SCR type latch-up.

TSI's STAC9750/9751 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the CODEC. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

However, the STAC9750/9751 is not designed to operate for extended periods with only the analog supply active.

NOTE: PIN 48:

TO ENABLE SPDIF, USE A 1 K Ω -10 K Ω EXTERNAL PULLDOWN.

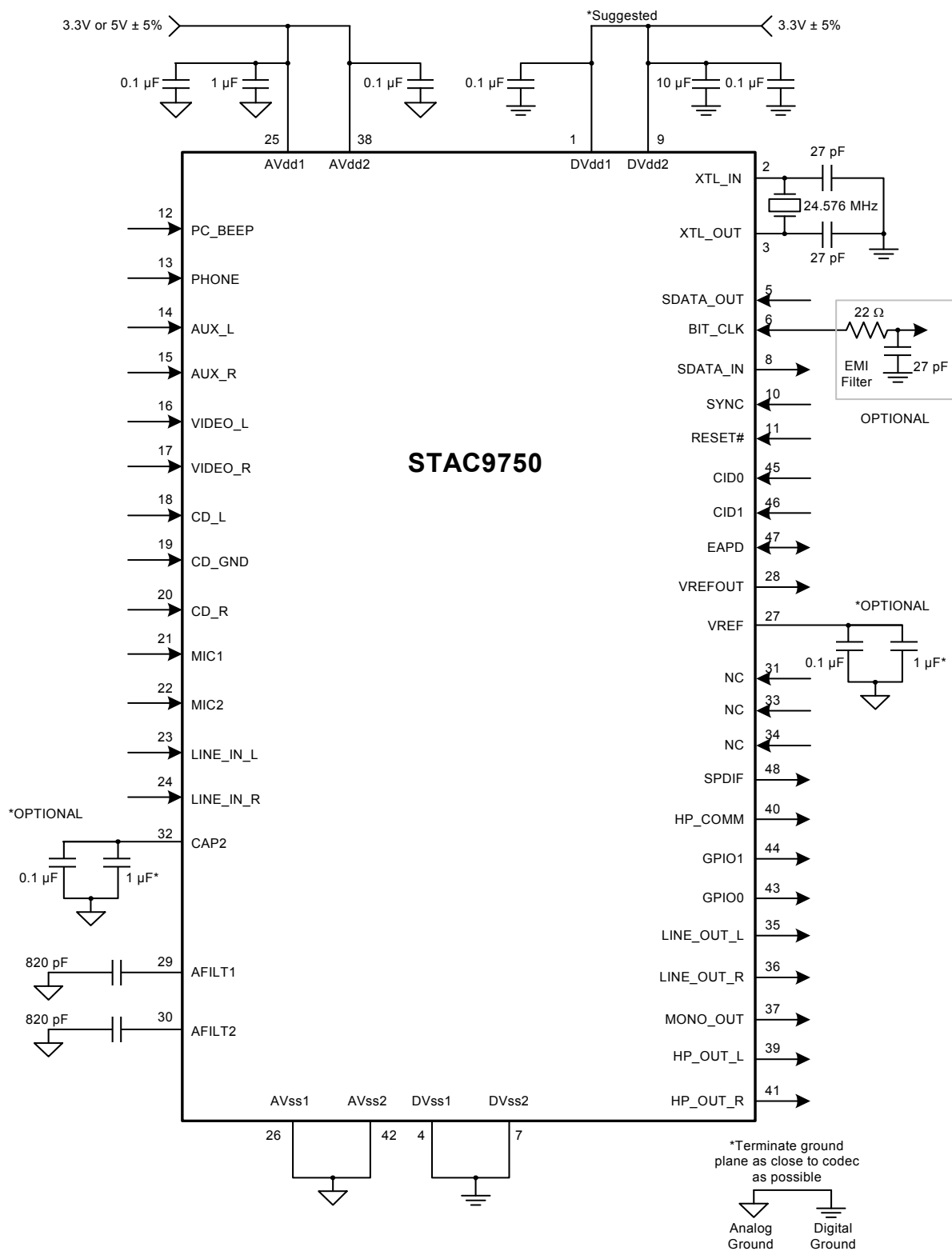
TO DISABLE SPDIF, USE A 1 K Ω -10 K Ω EXTERNAL PULLUP.

DO NOT LEAVE PIN 48 FLOATING.

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Figure 24. STAC9750/9751 Split Independent Power Supply Operation Typical Connection Diagram



15. APPENDIX B: PROGRAMMING REGISTERS

| Reg # | Name | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Default |
|-------|-------------------------------|----------|----------|----------|--------------|----------|----------|-----------|-----------|----------|-----------------|----------|----------|-------|----------------|-------------|--------------|-------------|---------|
| 00h | Reset | RSRVD | SE4 | SE3 | SE2 | SE1 | SE0 | ID9 | ID8 | ID7 | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | 6990h | |
| 02h | Master Volume | Mute | RSRVD | ML5 | ML4 | ML3 | ML2 | ML1 | ML0 | Reserved | | MR5 | MR4 | MR3 | MR2 | MR1 | MR0 | 8000h | |
| 04h | HP_OUT Mixer Volume | Mute | RSRVD | HPL5 | HPL4 | HPL3 | HPL2 | HPL1 | HPL0 | Reserved | | HPR5 | HPR4 | HPR3 | HPR2 | HPR1 | HPR0 | 8000h | |
| 06h | Master Volume Mono | Mute | Reserved | | | | | | | | | MM5 | MM4 | MM3 | MM2 | MM1 | MM0 | 8000h | |
| 0Ah | PC_BEEP Volume | Mute | Reserved | | | | | | | | | | | PV3 | PV2 | PV1 | PV0 | RSRVD | 0000h |
| 0Ch | Phone Volume | Mute | Reserved | | | | | | | | | | | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 0Eh | Mic Volume | Mute | Reserved | | | | | | | | | boosted | RSRVD | GN4 | GN3 | GN2 | GN1 | GN0 | 8008h |
| 10h | Line In Volume | Mute | Reserved | GL4 | GL3 | GL2 | GL1 | GL0 | Reserved | | Reserved | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | |
| 12h | CD Volume | Mute | Reserved | GL4 | GL3 | GL2 | GL1 | GL0 | Reserved | | Reserved | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | |
| 14h | Video Volume | Mute | Reserved | GL4 | GL3 | GL2 | GL1 | GL0 | Reserved | | Reserved | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | |
| 16h | AUX Volume | Mute | Reserved | GL4 | GL3 | GL2 | GL1 | GL0 | Reserved | | Reserved | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | |
| 18h | PCM Out Volume | Mute | Reserved | GL4 | GL3 | GL2 | GL1 | GL0 | Reserved | | Reserved | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | |
| 1Ah | Record Select | Reserved | | | | | SL2 | SL1 | SL0 | Reserved | | | | | SR2 | SR1 | SR0 | 0000h | |
| 1Ch | Record Gain | Mute | Reserved | | | GL3 | GL2 | GL1 | GL0 | Reserved | | | | GR3 | GR2 | GR1 | GR0 | 8000h | |
| 20h | General Purpose | POP BYP | RSRVD | 3D | Reserved | | | MIX | MS | LPBK | Reserved | | | | | | | 0000h | |
| 22h | 3D Control | Reserved | | | | | | | | | | | | DP3 | DP2 | Reserved | | 0000h | |
| 24h | Audio Interrupt | I4 | I3 | Reserved | | I0 | Reserved | | | | | | | | | | | | 0000h |
| 26h | Powerdown Ctrl/Stat | EAPD | PR6 | PR5 | PR4 | PR3 | PR2 | PR1 | PR0 | Reserved | | | | REF | ANL | DAC | ADC | 000Fh | |
| 28h | Extended Audio ID | ID1 | ID0 | Reserved | | REV1 (0) | REV0 (1) | AMAP | LDAC | SDAC | CDAC | DSA1 | DSA0 | RSVD | SPDIF | DRA | VRA | 0605h | |
| 2Ah | Extended Audio Control/Status | Reserved | | | | | SPCV | RSRVD | | | | SPSA1 | SPSA0 | RSRVD | SPDIF | RSRVD | VRA enable | 0400h | |
| 2Ch | PCM DAC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h | |
| 32h | PCM LR ADC Rate | SR15 | SR14 | SR13 | SR12 | SR11 | SR10 | SR9 | SR8 | SR7 | SR6 | SR5 | SR4 | SR3 | SR2 | SR1 | SR0 | BB80h | |
| 3Ah | SPDIF Control | #V | DRS | SPSR1 | SPSR2 | L | CC6 | CC5 | CC4 | CC3 | CC2 | CC1 | CC0 | PRE | COPY | #PCM/AUDIO | PRO | 2A00h | |
| 3Eh | Extended Modem Status | Reserved | | | | | | | PRA | Reserved | | | | | | | GPIO | | 0100h |
| 4Ch | GPIO Pin Config | Reserved | | | | | | | | | | | | | | GC1 (GPIO1) | GC0 (GPIO0) | 0300h | |
| 4Eh | GPIO Pin Polarity/Type | Reserved | | | | | | | | | | | | | | GP1 (GPIO1) | GP0 (GPIO0) | FFFFh | |
| 50h | GPIO Pin Sticky | Reserved | | | | | | | | | | | | | | GS1 (GPIO1) | GS0 (GPIO0) | 0000h | |
| 52h | GPIO Pin Mask | Reserved | | | | | | | | | | | | | | GW1 (GPIO1) | GW0 (GPIO0) | 0000h | |
| 54h | GPIO Pin Status | Reserved | | | | | | | | | | | | | | GI1 (GPIO1) | GI0 (GPIO0) | 0000h | |
| 60h | Z_DATA Volume | Mute | Reserved | GL4 | GL3 | GL2 | GL1 | GL0 | Reserved | | | | GR4 | GR3 | GR2 | GR1 | GR0 | 8808h | |
| 6Ah | Digital Audio Control | Reserved | | | | | | | | | | | | | | DO1 | | DO0 | 0000h |
| 6Ch | Revision Code | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00xxh | |
| 6Eh | Analog Special | Reserved | | | AC97 ALL MIX | Reserved | | | | | MUTE FIX DISBLE | ADCslot1 | ADCslot0 | RSVD | MIC GAIN VALUE | SPLY OVR EN | SPLY OVR VAL | 1000h | |
| 70h | 72h Enable | EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | 0000h | |
| 72h | Analog Current Adjust | Reserved | | | | | | | | INT | APOP | Reserved | | | | IBIAS<1:0> | | RSVD | 0000h |
| 74h* | GPIO Access | EAPD | RSVD | GPIO1 | GPIO0 | EAPD_OEN | Reserved | GPIO1_OEN | GPIO0_OEN | Reserved | | | | | | | | | 0000h |
| 76h | 78h Enable | EN15 | EN14 | EN13 | EN12 | EN11 | EN10 | EN9 | EN8 | EN7 | EN6 | EN5 | EN4 | EN3 | EN2 | EN1 | EN0 | 0000h | |
| 78h | High Pass Filter Bypass | RSEERVED | | | | | | | | | | | | | | | | ADC HPF BYP | 0000h |
| 7Ch | Vendor ID1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8384h | |
| 7Eh | Vendor ID2 9750 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 7650h | |

Note: All registers not shown, and those labeled "Reserved", can be written to but are "Don't Care" on read back.

Note: PC_BEEP defaults to 0000h, mute off.

16. REVISION HISTORY

| Revision | Date | Description of Change |
|----------|-----------------|--|
| 5.2 | October 2003 | Corrected error on page 26: Slot 1 Status Address Port, bit D2 is a SSlot Request not Reserved as stated in rev 5.1 Added CD_GND elaboration note on connection diagram, pin list and pin out diagrams: The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect. |
| 5.3 | June 2004 | Corrected Note 4 in performance characteristics, was missing the text "Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a". Complete note now reads "Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. 48 KHz Sample Frequency". |
| 5.4 | January 2005 | Added updated 48-pin package drawing. Added reflow profile information. |
| 5.5 | February 2005 | Revised reflow profile information |
| 5.6 | March 2005 | Revised TQFP to say LQFP. |
| 5.7 | December 2005 | Updated with new logo template Added Part order information for RoHS package, with EOL information to Pb-bearing Removed references to older revisions (CA3) and their relationship to CC1, as CA3 is EOL and CC1 is the only production revision. |
| 5.8 | 30 October 2006 | Initial release in IDT format. |
| 5.9 | October 2014 | Released in TSI format. |



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