

HEF4017B

5-stage Johnson decade counter

Rev. 9 — 8 April 2016

Product data sheet

1. General description

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (Q0 to Q9), an active LOW carry output from the most significant flip-flop ($\overline{Q5-9}$), active HIGH and active LOW clock inputs (CP0, $\overline{CP1}$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW-to-HIGH transition at CP0 while $\overline{CP1}$ is LOW or a HIGH-to-LOW transition at $\overline{CP1}$ while CP0 is HIGH (see [Table 3](#)).

When cascading counters, the $\overline{Q5-9}$ output, which is LOW while the counter is in states 5, 6, 7, 8, and 9, can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0 = $\overline{Q5-9}$ = HIGH; Q1 to Q9 = LOW) independent of the clock inputs (CP0, $\overline{CP1}$).

Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt trigger action makes the clock inputs highly tolerant of slower rise and fall times.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD} , V_{SS} , or another input.

2. Features and benefits

- Automatic counter correction
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40 °C to $+125\text{ °C}$
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from -40 °C to $+125\text{ °C}$

| Type number | Package | | Version |
|-------------|---------|--|----------|
| | Name | Description | |
| HEF4017BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

4. Functional diagram

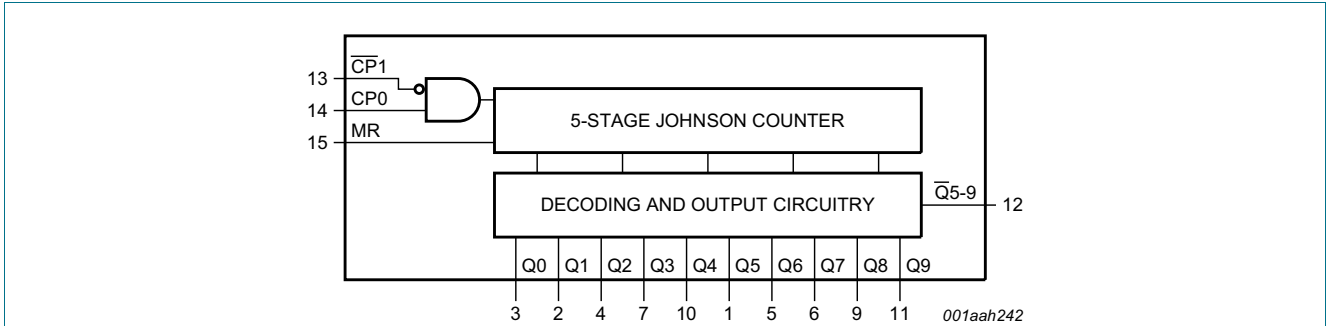


Fig 1. Functional diagram

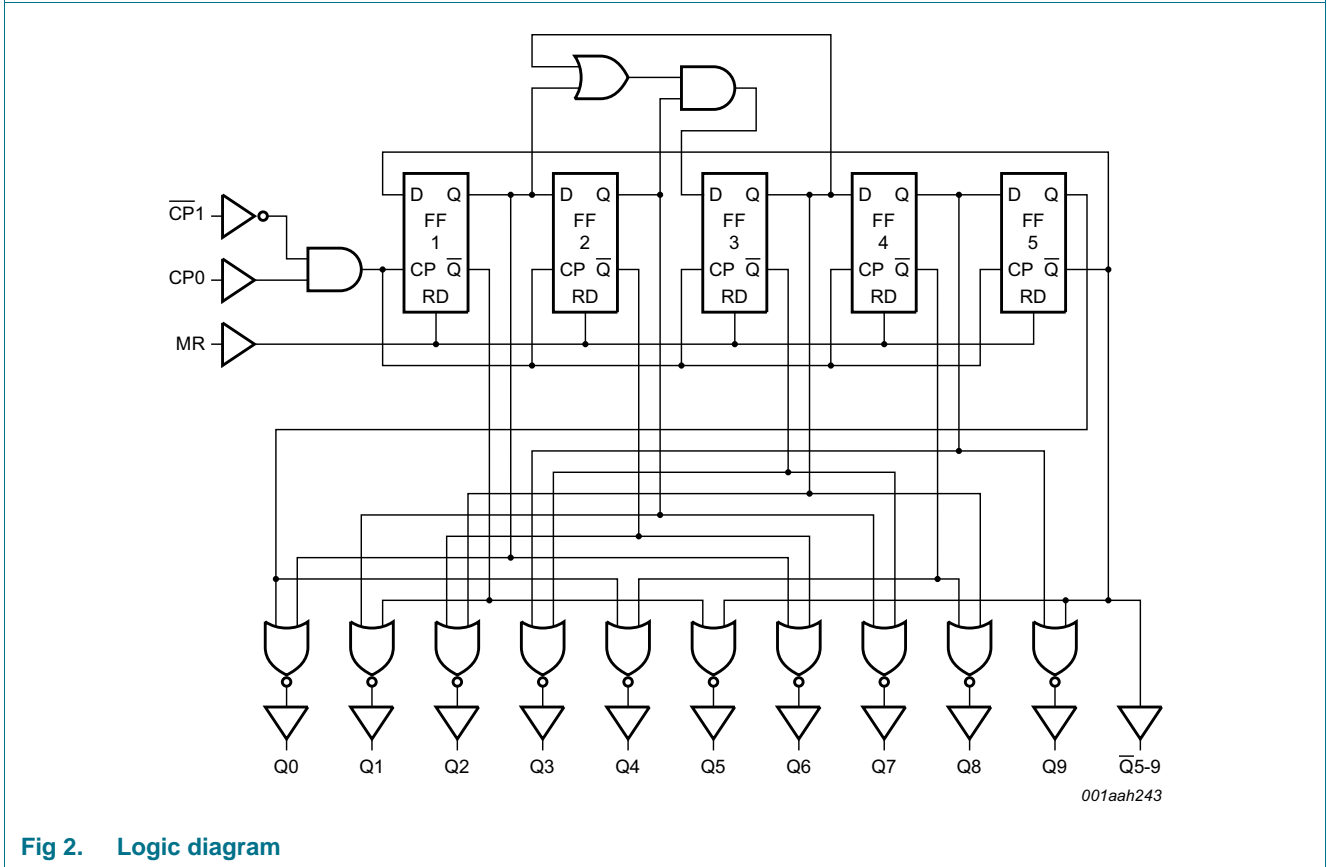


Fig 2. Logic diagram

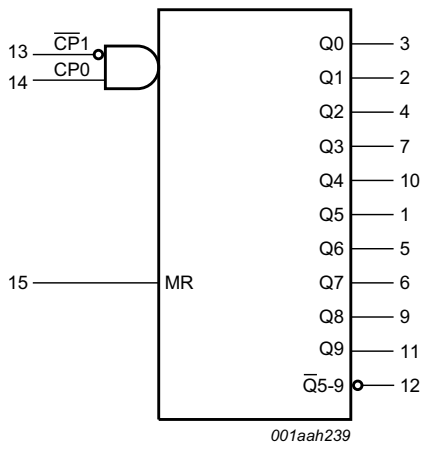


Fig 3. Logic symbol

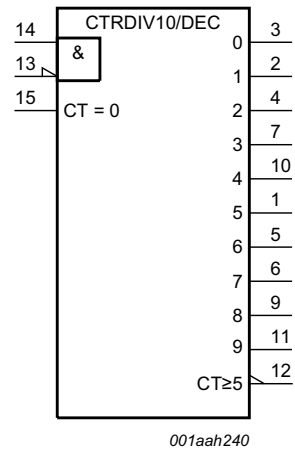


Fig 4. IEE logic symbol

5. Pinning information

5.1 Pinning

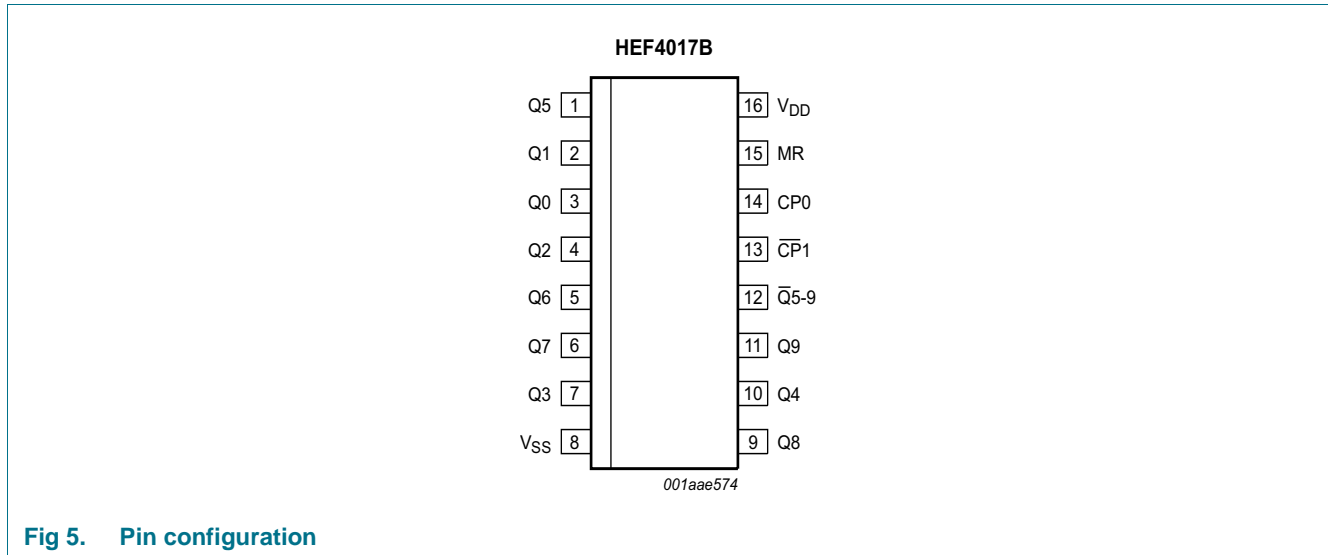


Fig 5. Pin configuration

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-------------------|--------------------------------|--|
| Q0 to Q9 | 3, 2, 4, 7, 10, 1, 5, 6, 9, 11 | decoded output |
| V _{SS} | 8 | ground supply voltage |
| $\overline{Q5-9}$ | 12 | carry output (active LOW) |
| $\overline{CP1}$ | 13 | clock input (HIGH-to-LOW edge-triggered) |
| CP0 | 14 | clock input (LOW-to-HIGH edge-triggered) |
| MR | 15 | master reset input |
| V _{DD} | 16 | supply voltage |

6. Functional description

Table 3. Function table [1]

| MR | CP0 | $\overline{CP1}$ | Operation |
|----|-----|------------------|--|
| H | X | X | Q0 = $\overline{Q5-9}$ = H; Q1 to Q9 = L |
| L | H | ↓ | counter advances |
| L | ↑ | L | counter advances |
| L | L | X | no change |
| L | X | H | no change |
| L | H | ↑ | no change |
| L | ↓ | L | no change |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care;
 ↑ = positive-going transition; ↓ = negative-going transition.

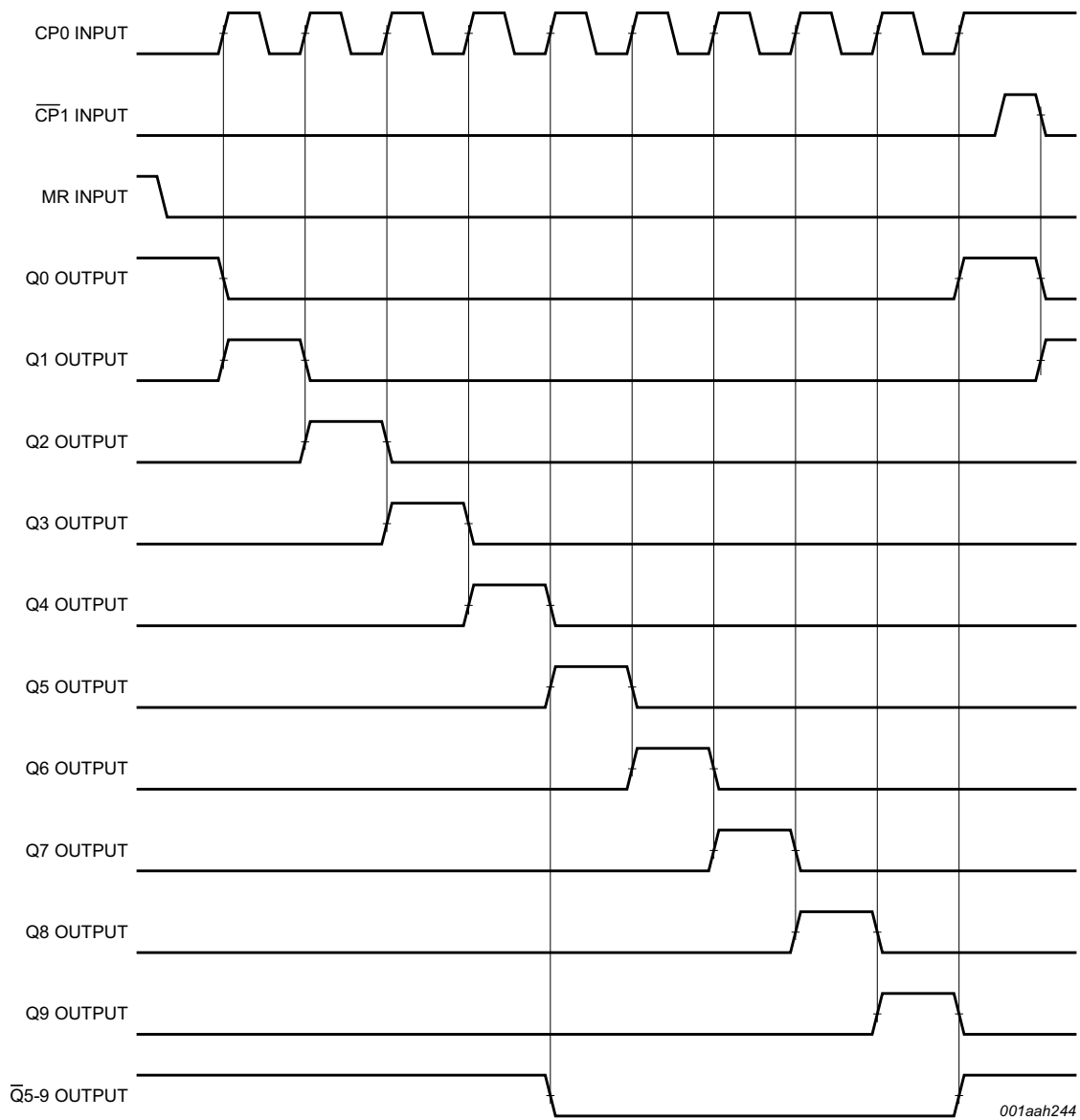


Fig 6. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|----------------|------|
| V_{DD} | supply voltage | | -0.5 | +18 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$ | - | ± 10 | mA |
| V_I | input voltage | | -0.5 | $V_{DD} + 0.5$ | V |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$ | - | ± 10 | mA |
| $I_{I/O}$ | input/output current | | - | ± 10 | mA |
| I_{DD} | supply current | | - | 50 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| T_{amb} | ambient temperature | | -40 | +125 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ | | | |
| | | SO16 package [1] | - | 500 | mW |
| P | power dissipation | per output | - | 100 | mW |

[1] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|------------------------|-----|-----|----------|-----------------|
| V_{DD} | supply voltage | | 3 | - | 15 | V |
| V_I | input voltage | | 0 | - | V_{DD} | V |
| T_{amb} | ambient temperature | in free air | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD} = 5\text{ V}$ | - | - | 3.75 | $\mu\text{s/V}$ |
| | | $V_{DD} = 10\text{ V}$ | - | - | 0.5 | $\mu\text{s/V}$ |
| | | $V_{DD} = 15\text{ V}$ | - | - | 0.08 | $\mu\text{s/V}$ |

9. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

| Symbol | Parameter | Conditions | V_{DD} | $T_{amb} = -40\text{ °C}$ | | $T_{amb} = 25\text{ °C}$ | | $T_{amb} = 85\text{ °C}$ | | $T_{amb} = 125\text{ °C}$ | | Unit |
|----------|---------------------------|--|----------|---------------------------|-----------|--------------------------|-----------|--------------------------|-----------|---------------------------|-----------|---------------|
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | |
| V_{IH} | HIGH-level input voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | 11.0 | - | V |
| V_{IL} | LOW-level input voltage | $ I_O < 1\text{ }\mu\text{A}$ | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | - | 4.0 | V |
| V_{OH} | HIGH-level output voltage | $ I_O < 1\text{ }\mu\text{A}$; $V_I = V_{SS}$ or V_{DD} | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | 14.95 | - | V |
| V_{OL} | LOW-level output voltage | $ I_O < 1\text{ }\mu\text{A}$; $V_I = V_{SS}$ or V_{DD} | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | - | 0.05 | V |
| I_{OH} | HIGH-level output current | $V_O = 2.5\text{ V}$ | 5 V | - | -1.7 | - | -1.4 | - | -1.1 | - | -1.1 | mA |
| | | $V_O = 4.6\text{ V}$ | 5 V | - | -0.64 | - | -0.5 | - | -0.36 | - | -0.36 | mA |
| | | $V_O = 9.5\text{ V}$ | 10 V | - | -1.6 | - | -1.3 | - | -0.9 | - | -0.9 | mA |
| | | $V_O = 13.5\text{ V}$ | 15 V | - | -4.2 | - | -3.4 | - | -2.4 | - | -2.4 | mA |
| I_{OL} | LOW-level output current | $V_O = 0.4\text{ V}$ | 5 V | 0.64 | - | 0.5 | - | 0.36 | - | 0.36 | - | mA |
| | | $V_O = 0.5\text{ V}$ | 10 V | 1.6 | - | 1.3 | - | 0.9 | - | 0.9 | - | mA |
| | | $V_O = 1.5\text{ V}$ | 15 V | 4.2 | - | 3.4 | - | 2.4 | - | 2.4 | - | mA |
| I_I | input leakage current | | 15 V | - | ± 0.1 | - | ± 0.1 | - | ± 1.0 | - | ± 1.0 | μA |
| I_{DD} | supply current | $I_O = 0\text{ A}$; $V_I = V_{SS}$ or V_{DD} | 5 V | - | 5 | - | 5 | - | 150 | - | 150 | μA |
| | | | 10 V | - | 10 | - | 10 | - | 300 | - | 300 | μA |
| | | | 15 V | - | 20 | - | 20 | - | 600 | - | 600 | μA |
| C_I | input capacitance | | - | - | - | 7.5 | - | - | - | - | pF | |

10. Dynamic characteristics

Table 7. Dynamic characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; for test circuit see [Figure 10](#)

| Symbol | Parameter | Conditions | V_{DD} | Extrapolation formula ^[1] | Min | Typ | Max | Unit |
|-----------|-------------------------------|--|----------|--|-----|-----|-----|------|
| t_{PHL} | HIGH to LOW propagation delay | CP0, $\overline{\text{CP1}} \rightarrow \text{Q0 to Q9}$; see Figure 7 | 5 V | $113\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 140 | 280 | ns |
| | | | 10 V | $44\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 55 | 110 | ns |
| | | | 15 V | $32\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 40 | 80 | ns |
| | | CP0, $\overline{\text{CP1}} \rightarrow \overline{\text{Q5-9}}$; see Figure 7 | 5 V | $118\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 145 | 290 | ns |
| | | | 10 V | $44\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 55 | 110 | ns |
| | | | 15 V | $32\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 40 | 80 | ns |
| | | MR $\rightarrow \text{Q1 to Q9}$; see Figure 8 | 5 V | $88\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 115 | 230 | ns |
| | | | 10 V | $39\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 50 | 100 | ns |
| | | | 15 V | $27\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 35 | 70 | ns |
| t_{PLH} | LOW to HIGH propagation delay | CP0, $\overline{\text{CP1}} \rightarrow \text{Q0 to Q9}$; see Figure 7 | 5 V | $98\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 125 | 250 | ns |
| | | | 10 V | $39\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 50 | 100 | ns |
| | | | 15 V | $32\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 40 | 80 | ns |
| | | CP0, $\overline{\text{CP1}} \rightarrow \overline{\text{Q5-9}}$; see Figure 7 | 5 V | $98\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 125 | 250 | ns |
| | | | 10 V | $39\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 50 | 100 | ns |
| | | | 15 V | $32\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 40 | 80 | ns |
| | | MR $\rightarrow \overline{\text{Q5-9}}$; see Figure 8 | 5 V | $83\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 110 | 220 | ns |
| | | | 10 V | $34\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 45 | 90 | ns |
| | | | 15 V | $27\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 35 | 70 | ns |
| | | MR $\rightarrow \text{Q0}$; see Figure 8 | 5 V | $103\text{ ns} + (0.55\text{ ns/pF})C_L$ | - | 130 | 260 | ns |
| | | | 10 V | $44\text{ ns} + (0.23\text{ ns/pF})C_L$ | - | 55 | 105 | ns |
| | | | 15 V | $32\text{ ns} + (0.16\text{ ns/pF})C_L$ | - | 40 | 75 | ns |
| t_t | transition time | see Figure 7 | 5 V | $10\text{ ns} + (1.00\text{ ns/pF})C_L$ | - | 60 | 120 | ns |
| | | | 10 V | $9\text{ ns} + (0.42\text{ ns/pF})C_L$ | - | 30 | 60 | ns |
| | | | 15 V | $6\text{ ns} + (0.28\text{ ns/pF})C_L$ | - | 20 | 40 | ns |
| t_h | hold time | CP0 $\rightarrow \overline{\text{CP1}}$; see Figure 9 | 5 V | | 90 | 45 | - | ns |
| | | | 10 V | | 40 | 20 | - | ns |
| | | | 15 V | | 20 | 10 | - | ns |
| | | $\overline{\text{CP1}} \rightarrow \text{CP0}$; see Figure 9 | 5 V | | 80 | 40 | - | ns |
| | | | 10 V | | 40 | 20 | - | ns |
| | | | 15 V | | 30 | 10 | - | ns |

Table 7. Dynamic characteristics ...continued $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; for test circuit see [Figure 10](#)

| Symbol | Parameter | Conditions | V _{DD} | Extrapolation formula ^[1] | Min | Typ | Max | Unit |
|------------------|-------------------|---|-----------------|--------------------------------------|-----|-----|-----|------|
| t _w | pulse width | CP0 input LOW; minimum width; see Figure 8 | 5 V | | 80 | 40 | - | ns |
| | | | 10 V | | 40 | 20 | - | ns |
| | | | 15 V | | 30 | 15 | - | ns |
| | | CP1 input HIGH; minimum width; see Figure 8 | 5 V | | 80 | 40 | - | ns |
| | | | 10 V | | 40 | 20 | - | ns |
| | | | 15 V | | 30 | 15 | - | ns |
| | | MR input HIGH; minimum width; see Figure 8 | 5 V | | 50 | 25 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 20 | 10 | - | ns |
| t _{rec} | recovery time | MR input; see Figure 8 | 5 V | | 60 | 30 | - | ns |
| | | | 10 V | | 30 | 15 | - | ns |
| | | | 15 V | | 20 | 10 | - | ns |
| f _{max} | maximum frequency | see Figure 8 | 5 V | | 6 | 12 | - | MHz |
| | | | 10 V | | 12 | 30 | - | MHz |
| | | | 15 V | | 15 | 30 | - | MHz |

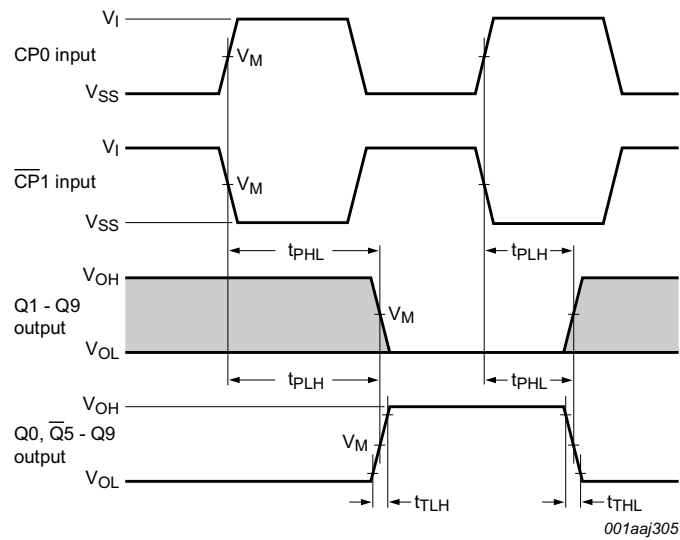
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

[2] t_t is the same as t_{THL} and t_{TLH}.

Table 8. Dynamic power dissipation P_D P_D can be calculated from the formulas shown. $V_{SS} = 0\text{ V}$; $t_r = t_f \leq 20\text{ ns}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

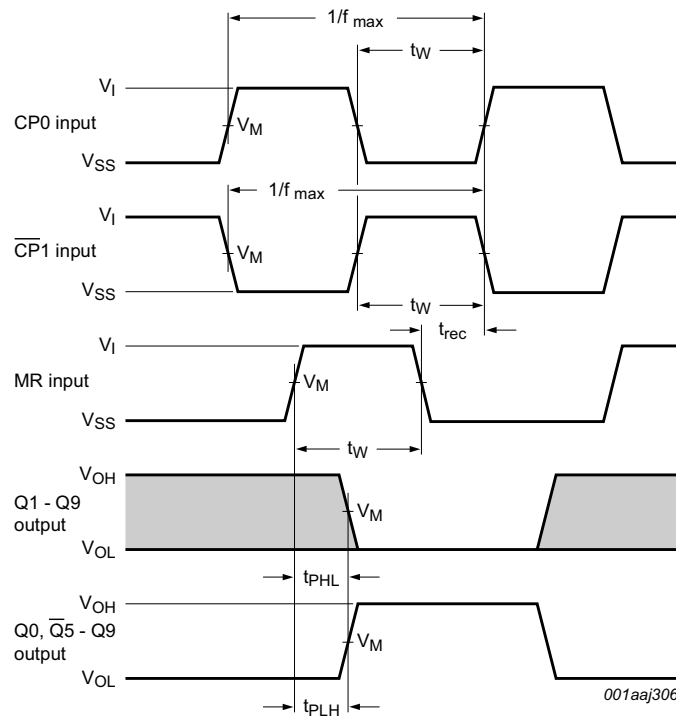
| Symbol | Parameter | V _{DD} | Typical formula for P _D (μW) | where: |
|----------------|---------------------------|-----------------|--|---|
| P _D | dynamic power dissipation | 5 V | $P_D = 500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | f _i = input frequency in MHz; f _o = output frequency in MHz; C _L = output load capacitance in pF; V _{DD} = supply voltage in V; Σ(C _L × f _o) = sum of the outputs. |
| | | 10 V | $P_D = 2200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 6000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

11. Waveforms



Conditions: $\overline{CP1} = \text{LOW}$, while CP0 triggers on a LOW-to-HIGH transition. $\overline{CP1}$ triggers on a HIGH-to-LOW transition;
 The shaded areas indicate where the output state is set by the input count.
 Measurement points given in [Table 9](#).

Fig 7. Waveforms showing the propagation delays for CP0, $\overline{CP1}$ to Qn, Q5-9 outputs and the output transition times

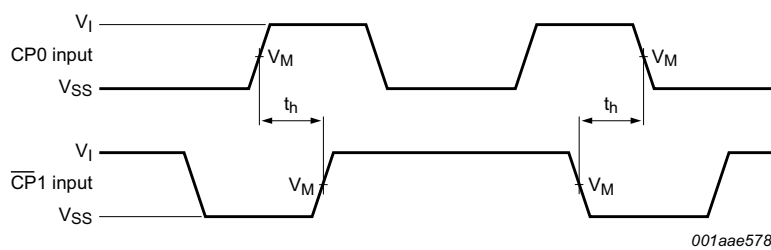


Conditions: $\overline{CP1} = \text{LOW}$, while CP0 triggers on a LOW-to-HIGH transition, t_W and t_{rec} are measured when CP0 = HIGH and $\overline{CP1}$ triggers on a HIGH-to-LOW transition.

The shaded areas indicate where the output state is set by the input count.

Measurement points given in [Table 9](#).

Fig 8. Waveforms showing the minimum pulse width for CP0, $\overline{CP1}$ and MR input; the maximum frequency for CP0 and CP1 input; the recovery time for MR and the MR input to Qn and Q5-9 output propagation delays



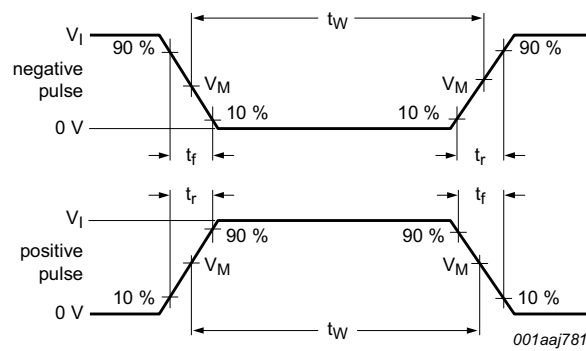
Hold times are shown as positive values, but may be specified as negative values;

Measurement points given in [Table 9](#).

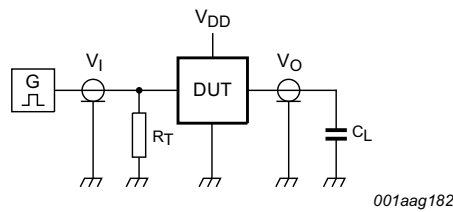
Fig 9. Waveforms showing hold times for CP0 to $\overline{CP1}$ and $\overline{CP1}$ to CP0

Table 9. Measurement points

| Supply voltage | Input | Output |
|----------------|-------------|-------------|
| V_{DD} | V_M | V_M |
| 5 V to 15 V | $0.5V_{DD}$ | $0.5V_{DD}$ |



a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test;

C_L = load capacitance including jig and probe capacitance;

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig 10. Test circuit for measuring switching times

Table 10. Test data

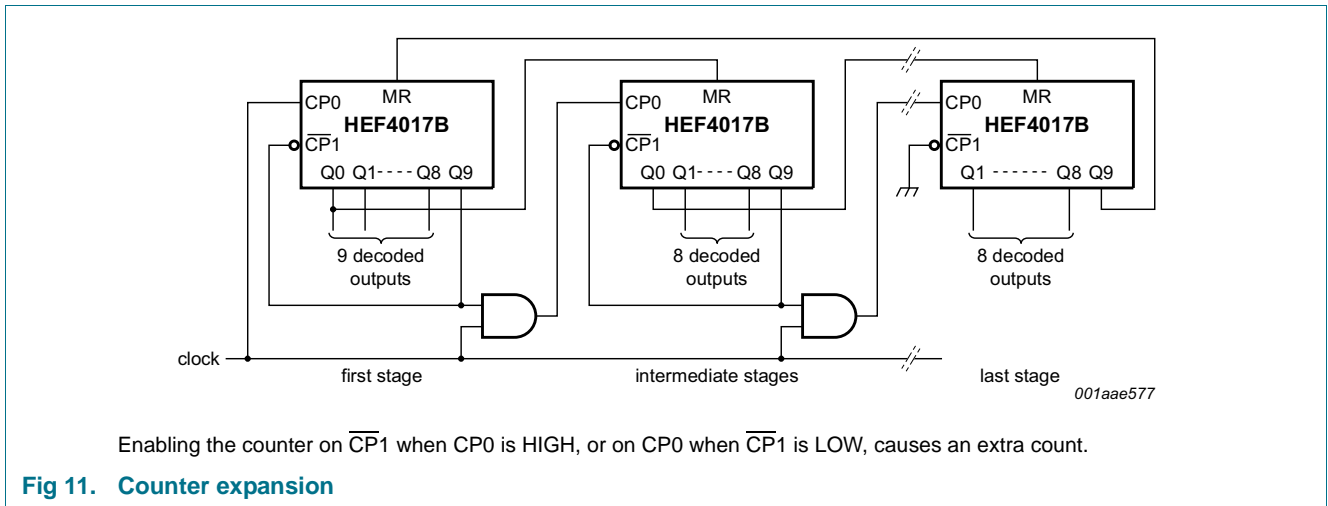
| Supply voltage | Input | Load |
|----------------|----------------------|-------|
| V_{DD} | V_I | C_L |
| 5 V to 15 V | V_{SS} or V_{DD} | 50 pF |

12. Application information

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer

Figure 11 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).



13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig 12. Package outline SOT109-1 (SO16)

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--|-----------------------|---------------|------------------|
| HEF4017B v.9 | 20160408 | Product data sheet | - | HEF4017B v.8 |
| Modifications: | <ul style="list-style-type: none"> Type number HEF4017BP (SOT38-4) removed. | | | |
| HEF4017B v.8 | 20111118 | Product data sheet | - | HEF4017B v.7 |
| Modifications: | <ul style="list-style-type: none"> Legal pages updated. Changes in “General description” and “Features and benefits”. Section “Applications” removed. | | | |
| HEF4017B v.7 | 20110914 | Product data sheet | - | HEF4017B v.6 |
| HEF4017B v.6 | 20091105 | Product data sheet | - | HEF4017B v.5 |
| HEF4017B v.5 | 20090709 | Product data sheet | - | HEF4017B v.4 |
| HEF4017B v.4 | 20081209 | Product data sheet | - | HEF4017B_CNV v.3 |
| HEF4017B_CNV v.3 | 19950101 | Product specification | - | HEF4017B_CNV v.2 |
| HEF4017B_CNV v.2 | 19950101 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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16. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

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