Quad 8-Bit Voltage Out CMOS DAC Complete with Internal 10 V Reference

DAC8426

FEATURES

No Adjustments Required, Total Error ±1 LSB Max Over Temperature
Four Voltage-Output DACs on a Single Chip
Internal 10 V Bandgap Reference
Operates from Single +15 V Supply
Fast 50 ns Data Load Time, All Temperatures
Pin-for-Pin Replacement for PM-7226 and AD7226, Eliminates External Reference

APPLICATIONS

Process Controls
Multichannel Microprocessor Controlled:
System Calibration
Op Amp Offset and Gain Adjust
Level and Threshold Setting

GENERAL DESCRIPTION

The DAC8426 is a complete quad voltage output D/A converter with internal reference. This product fits directly into any existing 7226 socket where the user currently has a 10 V external reference. The external reference is no longer necessary. The internal reference of the DAC8426 is laser-trimmed to ±0.4% offering a 25 ppm/°C temperature coefficient and 5 mA of external load driving capability.

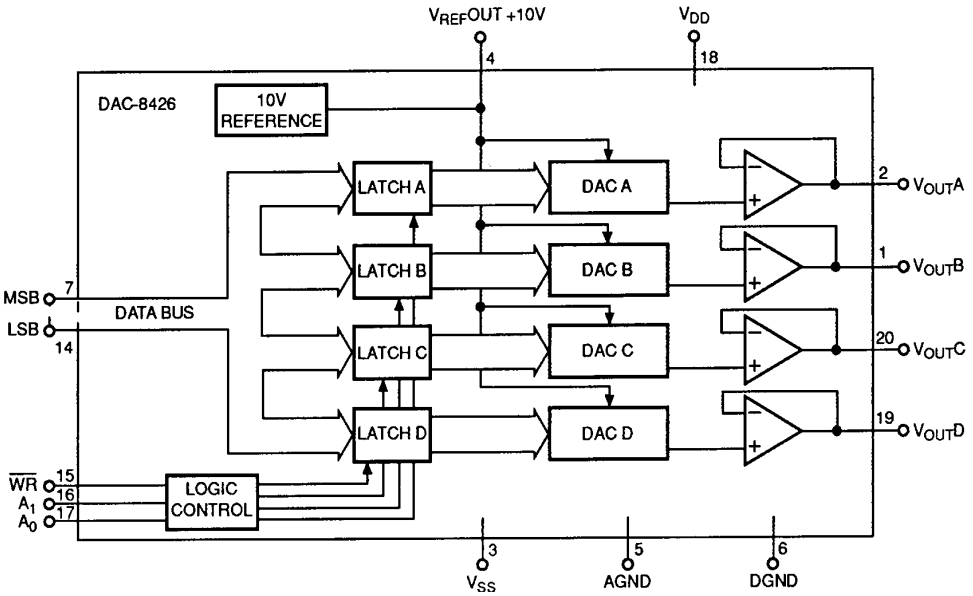
The DAC8426 contains four 8-bit voltage-output CMOS D/A converters on a single chip. A 10 V output bandgap reference sets the output full-scale voltage. The circuit also includes four input latches and interface control logic.

One of the four latches, selected by the address inputs, is loaded from the 8-bit data bus input when the write strobe is active low. All digital inputs are TTL/CMOS (5 V) compatible. The on-board amplifiers can drive up to 10 mA from either a single or dual supply. The on-board reference that is always connected to the internal DACs has 5 mA available to drive external devices.

Its compact size, low power, and economical cost-per-channel, make the DAC8426 attractive for applications requiring multiple D/A converters without sacrificing circuit-board space. System reliability is also increased due to reduced parts count.

PMI's advanced oxide-based, silicon-gate, CMOS process allows the DAC8426's analog and digital circuitry to be manufactured on the same chip. This, coupled with PMI's highly stable thin-film R-2R resistor ladder, aids in matching and temperature tracking between DACs.

FUNCTIONAL BLOCK DIAGRAM



REV. C

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DAC8426–SPECIFICATIONS (V_{DD} = +15 V ± 10%, AGND = DGND = 0 V, V_{SS} = 0 V, T_A = –55°C to +125°C applies for DAC8426AR/BR, T_A = –40°C to +85°C applies for DAC8426ER/EP/FR/FP/FS, unless otherwise noted.)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
STATIC PERFORMANCE							
Resolution	N			8			Bits
Total Unadjusted Error[1]	TUE	Includes Reference	A, E			±1	LSB
			B, F			±2	LSB
Relative Accuracy	INL		A, E			±1/2	LSB
			B, F			±1	LSB
Differential Nonlinearity[2]	DNL					±1	LSB
Full-Scale Temperature Coefficient	TCG_{FS}	Includes Reference			25		ppm/°C
Zero Scale Error	V_{ZSE}					20	mV
Zero Scale Error Temperature Coefficient	TCV_{ZS}	Dual Supply	V_{SS} = –5 V		10		µV/°C
REFERENCE OUTPUT							
Output Voltage	$V_{REF}OUT$	No Load	A, E	9.96		10.04	V
			B, F	9.92		10.08	V
Temperature Coefficient	$TCV_{REF}OUT$				20		ppm/°C
Load Regulation	LD_{REG}	ΔI_L = 5 mA			0.02	0.1	%/mA
Line Regulation	LN_{REG}	ΔV_{DD} ±10%			0.008	0.04	%/V
Output Noise[3]	e_n rms	f = 0.1 Hz to 10 Hz			3	10	µV p-p
Output Current	$I_{REF}OUT$	$\Delta V_{REF}OUT$ < 40 mV		5	7		mA
DIGITAL INPUTS							
Logic Input "0"	V_{INL}					0.8	V
Logic Input "1"	V_{INH}			2.4			V
Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}			0.1	10	µA
Input Capacitance[3]	C_{IN}				4	8	pF
POWER SUPPLIES							
Positive Supply Current[4]	I_{DD}				6	14	mA
Negative Supply Current[4]	I_{SS}	Dual Supply	V_{SS} = –5 V		4	10	mA
Power Dissipation[5]	P_{DISS}				90	210	mW
Power Supply Sensitivity	P_{SS}	ΔV_{DD} = ±5%			0.0002	0.01	%/%

ELECTRICAL CHARACTERISTICS V_{DD} = +15 V ± 10%, AGND = DGND = 0 V, V_{SS} = 0 V, T_A = –55°C to +125°C applies for DAC8426AR/BR, T_A = –40°C to +85°C applies for DAC8426ER/EP/FR/FP/FS, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ[6]	Max	Units
DAC OUTPUT						
Output Current (Source)[3]	I_{OUT}SOURCE	Digital In = All Ones	10			mA
Output Current (Sink)[3]	I_{OUT}SINK	Digital In = All Zeroes V_{SS} = –5 V	350	450		µA
Minimum Load Resistance	$R_{L(MIN)}$	Digital In = All Ones	2			kΩ
DYNAMIC PERFORMANCE[3]						
V_{OUT} Slew Rate	SR			4		V/µs
V_{OUT} Settling Time (Positive or Negative)	t_S	To ±1/2 LSB, R_L = 2 kΩ		3		µs
Digital Crosstalk	Q			10		nVs
SWITCHING CHARACTERISTICS[3]						
Address To Write Setup Time	t_{AS}		0			ns
Address To Write Hold Time	t_{AH}		0			ns
Data Valid To Write Setup Time	t_{DS}		70			ns
Data Valid To Write Hold Time	t_{DH}		10			ns
Write Pulse Width	t_{WR}		50			ns

NOTES
[1]Includes Full-Scale Error, Relative Accuracy, and Zero Code Error. Note ±1 LSB = ±0.39% error.
[2]All devices guaranteed monotonic over the full operating temperature range.
[3]Guaranteed and not subject to production test.
[4]Digital inputs V_{IN} = V_{INL} or V_{INH}; V_{OUT} and V_{REF}OUT unloaded.
[5]P_{DISS} calculated by $I_{DD} \times V_{DD}$.
[6]Typicals represent measured characteristics at T_A = +25°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND or DGND . . . . . –0.3 V, +17 V
V_{SS} to AGND or DGND . . . . . –7 V, V_{DD}
V_{DD} to V_{SS} . . . . . –0.3 V, +24 V
AGND to DGND . . . . . –0.3 V, +5 V
Digital Input Voltage to DGND . . . . . –0.3 V, V_{DD}
V_{REF}OUT to AGND[1] . . . . . –0.3 V, V_{DD}
V_{OUT} to AGND[1] . . . . . V_{SS}, V_{DD}
Operating Temperature
Military AR/BR . . . . . –55°C to +125°C
Extended Industrial ER/EP/FR/FP/FS . . . . –40°C to +85°C
Maximum Junction Temperature . . . . . +150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

THERMAL RESISTANCE

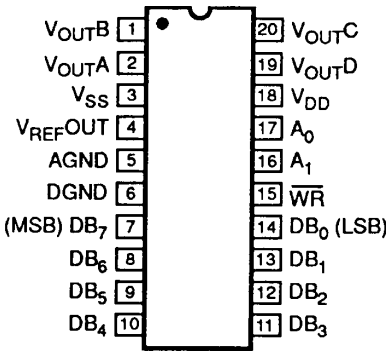
Package Type	θ_{JA}[2]	θ_{JC}	Units
20-Pin Cerdip (R)	70	7	°C/W
20-Pin Plastic DIP (P)	61	24	°C/W
20-Pin SOL(S)	80	22	°C/W

NOTES
[1]Outputs may be shorted to any terminal provided the package power dissipation is not exceeded. Typical output short-circuit current to AGND is 50 mA.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOL package.

CAUTION

1. Do not apply voltages higher than V_{DD} or less than V_{SS} potential on any terminal.
2. The digital control inputs are zener-protected; however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Do not insert this device into powered sockets. Remove power before insertion or removal.
4. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to device.

PIN CONNECTIONS

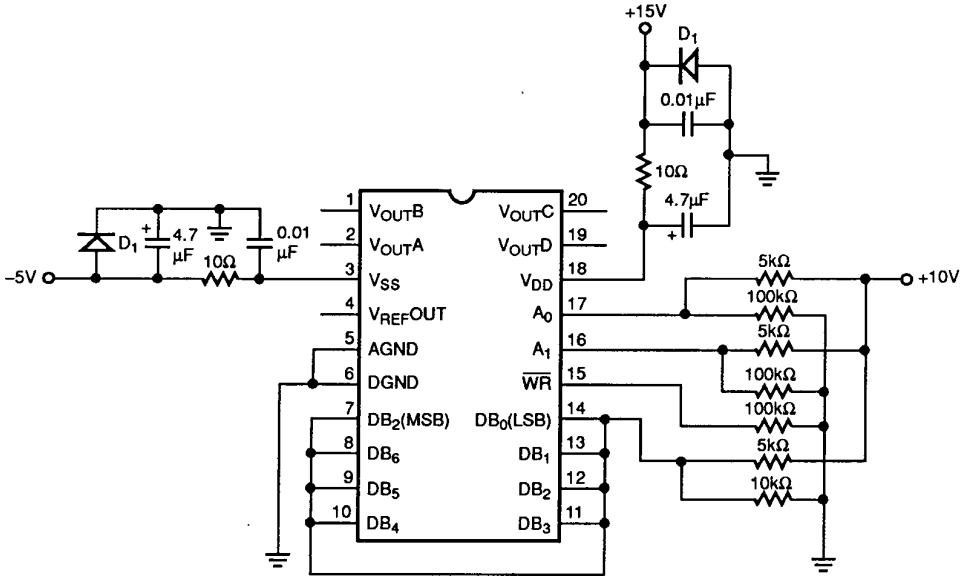


20-Pin Cerdip (R Suffix)
20-Pin Epoxy DIP (P Suffix)
20-Pin SOL (S Suffix)

ORDERING GUIDE[1]

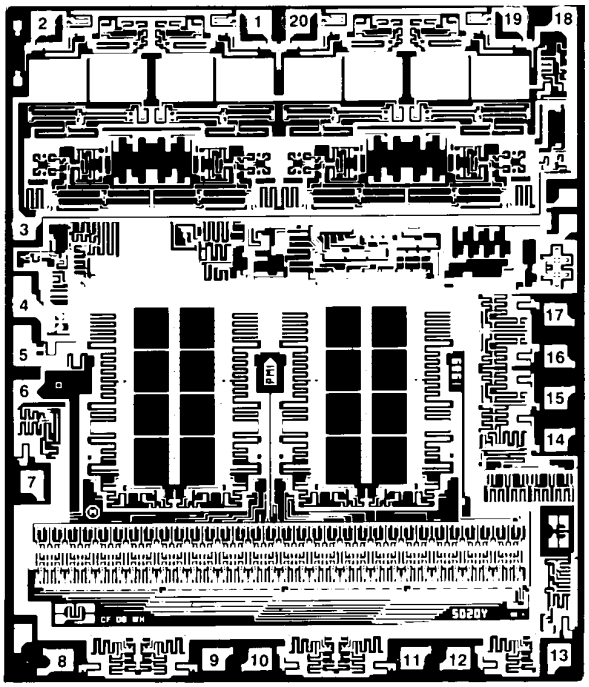
Model	Total Unadjusted Error	Temperature Range	Package Description
DAC8426AR[2]	±1 LSB	–55°C to +125°C	20-Pin Cerdip (Q-20)
DAC8426ER	±1 LSB	–40°C to +85°C	20-Pin Cerdip (Q-20)
DAC8426EP	±1 LSB	–40°C to +85°C	20-Pin Plastic DIP (N-20)
DAC8426BR[2]	±2 LSB	–55°C to +125°C	20-Pin Cerdip (Q-20)
DAC8426FR	±2 LSB	–40°C to +85°C	20-Pin Cerdip (Q-20)
DAC8426FP	±2 LSB	–40°C to +85°C	20-Pin Plastic DIP (N-20)
DAC8426FS[3]	±2 LSB	–40°C to +85°C	20-Lead SOL (R-20)

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in cerdip, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[3]For availability and burn-in information on SO and PLCC packages, contact your local sales office.



Burn-In Circuit

DICE CHARACTERISTICS



DIE SIZE 0.129 × 0.152 inch, 19,608 sq. mils
(3.28 × 3.86 mm, 12.65 sq. mm)

1. $V_{OUT\ B}$
2. $V_{OUT\ A}$
3. V_{SS}
4. V_{REF} OUT
5. AGND
6. DGND
7. DB_7 (MSB)
8. DB_6
9. DB_5
10. DB_4
11. DB_3
12. DB_2
13. DB_1
14. DB_0 (LSB)
15. $\overline{WR}$
16. A_1
17. A_0
18. V_{DD}
19. $V_{OUT\ D}$
20. $V_{OUT\ C}$

WAFER TEST LIMITS

at V_{DD} = +15 V ± 5%; V_{SS} = AGND = DGND = 0 V; unless otherwise specified. T_A = +25°C. All specifications apply for DACs A, B, C, and D.

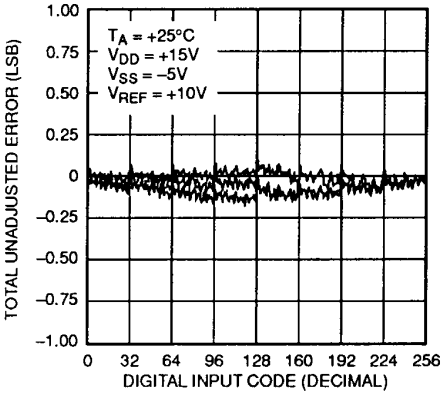
Parameter	Symbol	Conditions	DAC8426GBC Limits	Units
Total Unadjusted Error	TUE		±2	LSB max
Relative Accuracy	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Full-Scale Error	G_{FSE}		±1	LSB max
Zero Code Error	V_{ZSE}		±20	mV max
DAC Output Current	I_{OUT}SOURCE	Digital In = All Ones	10	mA min
Reference Output Voltage	V_{REF}OUT	No Load	10.04	V max
Load Regulation	LD_{REG}	ΔI_L = 5 mA	0.1	%/mA max
Line Regulation	LN_{REG}	ΔV_{DD} = ±10 V	0.04	%/V max
Reference Output Current	I_{REF}OUT	ΔV_{REF}OUT < 40 mV	5	mA min
Logic Inputs High	V_{INH}		2.4	V min
Logic Inputs Low	V_{INL}		0.8	V max
Logic Input Current	I_{IN}	V_{IN} = 0 V or V_{DD}	±1	µA max
Positive Supply Current	I_{DD}	V_{IN} = V_{INL} or V_{INH}	14	mA max
Negative Supply Current	I_{SS}	V_{IN} = V_{INL} or V_{INH}, V_{SS} = –5 V	10	mA max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

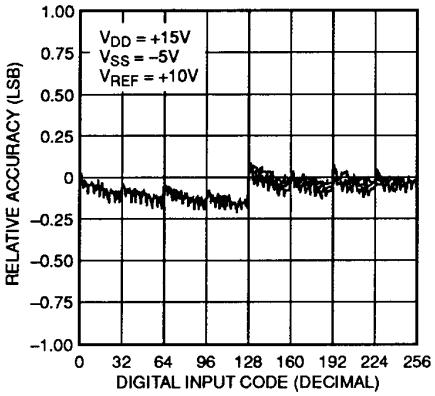
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8426 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

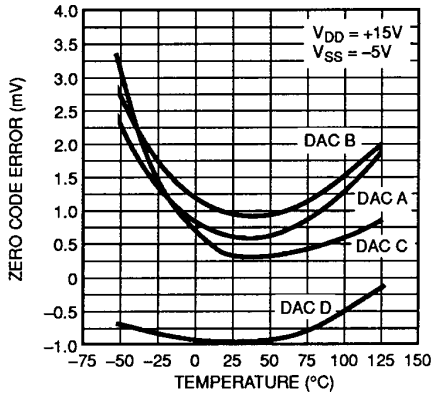
Typical Performance Characteristics–DAC8426



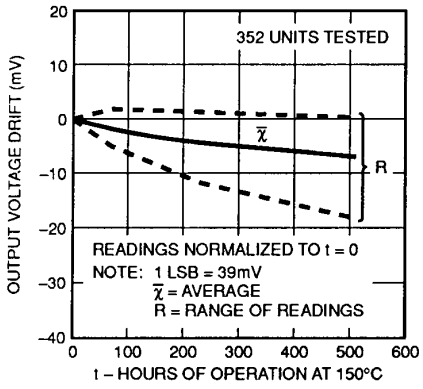
Channel-to-Channel Matching (DACs A, B, C, D, Superimposed)



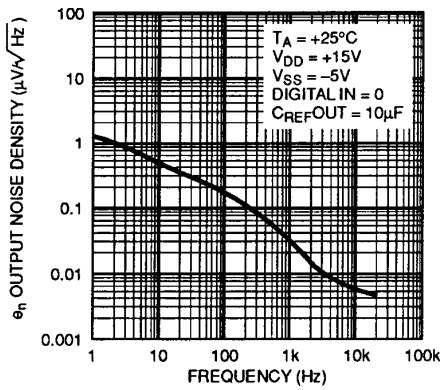
Relative Accuracy vs. Code at T_A = –55°C, +25°C, +125°C (All Superimposed)



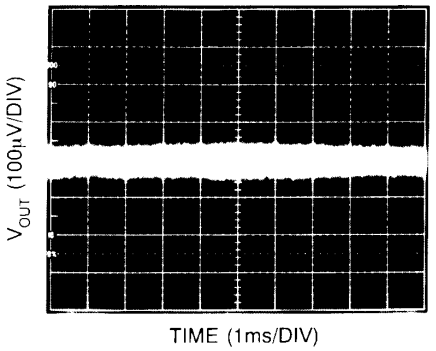
Zero Code Error vs. Temperature



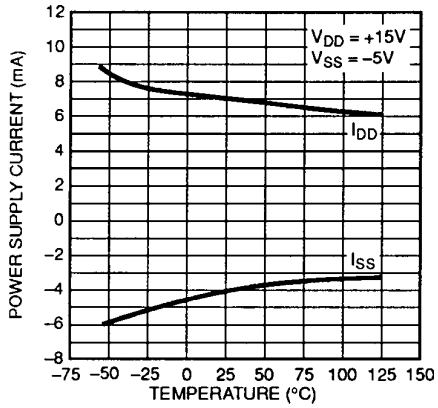
Long Term Drift Accelerated by Burn-In



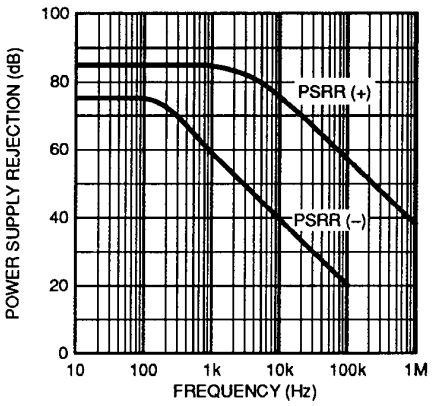
V_{OUT} Noise Density vs. Frequency



Broadband Noise (DC to 200 kHz)



Power Supply Current vs. Temperature



PSRR vs. Frequency

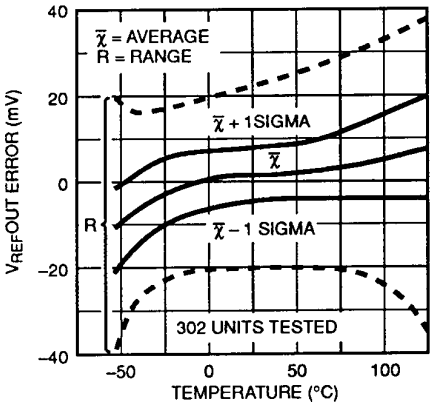
$$PSRR(+) = -20\ LOG\left(\frac{V_{OUT}\ (0)}{\Delta V_{DD}}\right),$$

V_{DD} = +15 V ±1 V_P, V_{SS} = 0 V

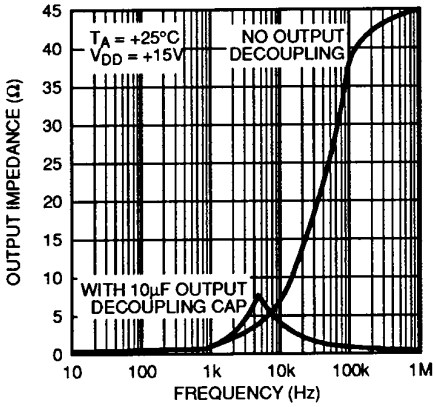
$$PSRR(-) = -20\ LOG\left(\frac{V_{OUT}\ (0)}{\Delta V_{SS}}\right),$$

V_{DD} = +15 V, V_{SS} = –4 V ±1 V_P

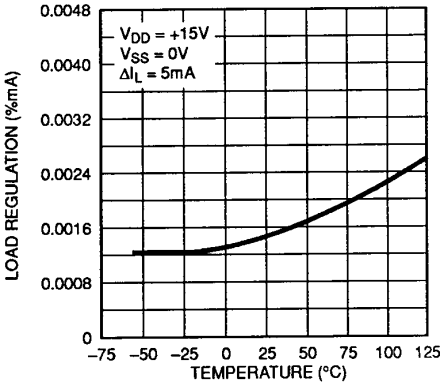
DAC8426–Typical Performance Characteristics



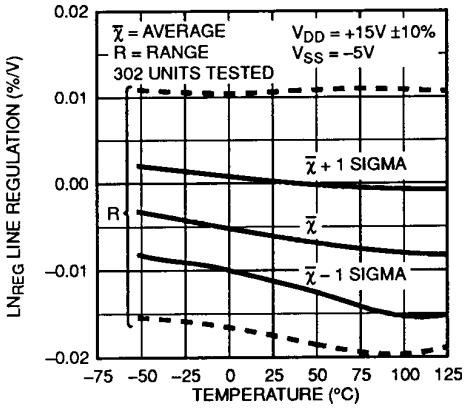
V_{REF}OUT Error from 10.000 V vs. Temperature



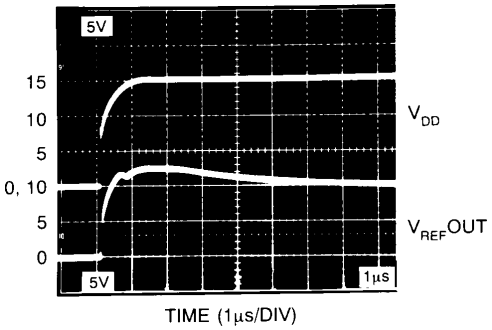
Output Impedance (V_{REF}OUT) vs. Frequency



V_{REF}OUT Load Regulation vs. Temperature



V_{REF}OUT Line Regulation vs. Temperature



V_{REF}OUT Start Up

PARAMETER DEFINITIONS

TOTAL UNADJUSTED ERROR (TUE)

This specification includes the Full-Scale-Error, Relative Accuracy Zero-Code-Error and the internal reference voltage. The ideal Full-Scale output voltage is 10 V minus 1 LSB which equals 9.961 volts. Each LSB equals 10 V × (1/256) = 0.039 volts.

DIGITAL CROSSTALK

Digital crosstalk is the signal coupled to the output of a DAC due to a changing digital input from adjacent DACs being updated. It is specified in nano-Volt-seconds (nVs).

CIRCUIT DESCRIPTION

The DAC8426 is a complete quad 8-bit D/A converter. It contains an internal bandgap reference, four voltage switched R-2R ladder DACs, four DAC latches, four output buffer amplifiers, and an address decoder. All four DACs share the internal ten volt reference and analog ground(AGND). Figure 1 provides an equivalent DAC plus buffer schematic.

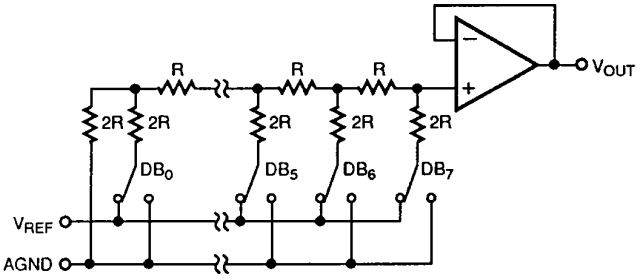


Figure 1. Simplified Circuit Configuration for One DAC. (Switches Are Shown for All "1s" on the Digital Inputs.)

The eleven digital inputs are compatible with both TTL and 5 V (or higher) CMOS logic. Table I shows the DAC control logic truth table for $\overline{WR}$, A_1, and A_0 operation. When $\overline{WR}$ is active low the input latch of the selected DAC is transparent, and the DAC's output responds to the data present on the eight digital data inputs (DBx). The data (DBx) is latched into the addressed DAC's latch on the positive edge of the $\overline{WR}$ control signal. The important timing requirements are shown in the Write Cycle Timing Diagram, Figure 2.

INTERNAL 10 VOLT REFERENCE

The internal 10 V bandgap reference of the DAC8426 is trimmed to the output voltage and temperature drift specifications. This internal reference is connected to the reference inputs of the four internal 8-bit D/A converters. The output terminal of the internal 10 V reference is available on pin 4. The 10 V output of the reference is produced with respect to the AGND pin. This reference output can be used to supply as much as 5 mA of additional current to external devices. Care has been taken in

Table I. DAC Control Logic Truth Table

Logic Control			DAC8426
$\overline{WR}$	A_1	A_0	Operation
H	X	X	No Operation Device Not Selected
L	L	L	DAC A Transparent
⨍	L	L	DAC A Latched
L	L	H	DAC B Transparent
⨍	L	H	DAC B Latched
L	H	L	DAC C Transparent
⨍	H	L	DAC C Latched
L	H	H	DAC D Transparent
⨍	H	H	DAC D Latched

L = Low State, H = High State, X = Don't Care

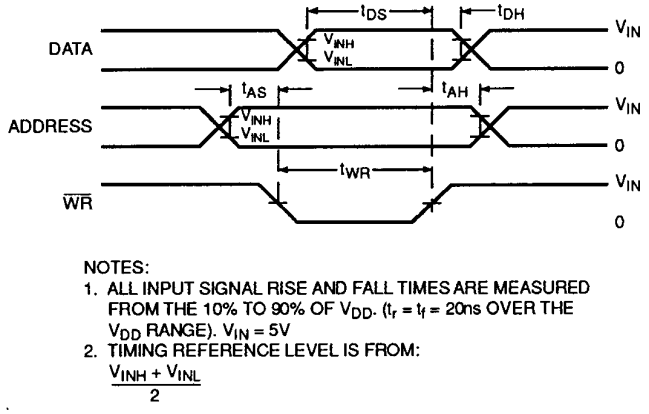
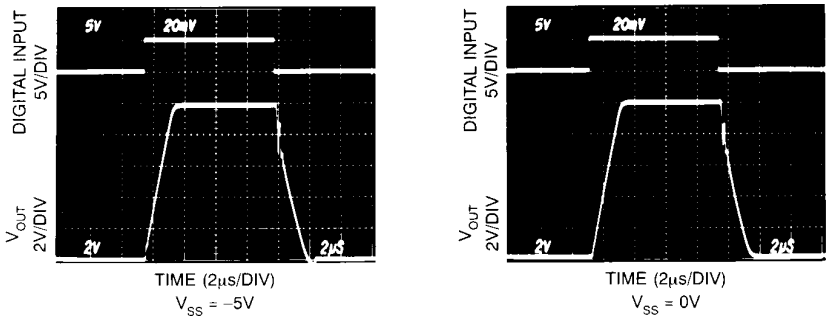


Figure 2. Write Cycle Timing Diagram

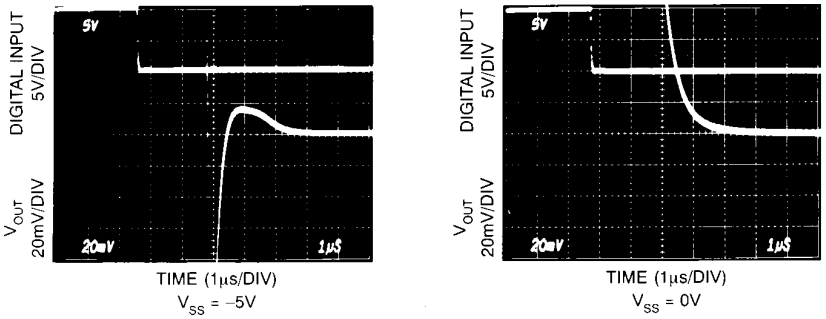
the design of the internal DAC switching to minimize transients on the reference voltage terminal (V_{REF}OUT). Other devices connected to this reference terminal should have well behaved input loading characteristics. D/A converters such as the PMI PM7226A have been designed to minimize reference input transient currents and can be directly connected to the DAC8426 10 V reference. Devices exhibiting large current transients due to internal switching should be buffered with an op amp to maintain good overall system noise performance. A 10 µF reference output bypass capacitor is required.

BUFFER AMPLIFIER SECTION

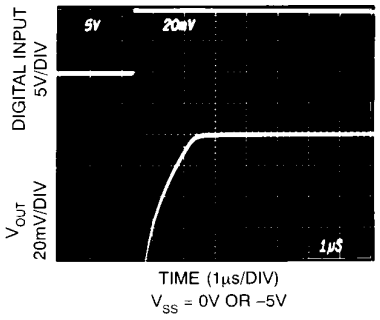
The four internal unity-gain voltage buffers provide low output impedance capable of sourcing 5 mA or sinking 350 µA. Typical output slew rates of ±4 V/µs are achieved with 10 V full-scale output changes and R_L = 2 kΩ. Figure 3 photographs show large signal and settling time response. Capacitive loads to 3300 pF maximum, and resistive loads to 2 kΩ minimum can be applied.



a) Large Signal



b) Settling Time Response (Negative Transition)



Test Conditions, All Photos:
V_{DD} = +15 V
C_{REF}OUT = 10 µF
R_L = 2 kΩ
Digital Input Sequence 0, 255, 0

c) Settling Time Response (Positive Transition)

Figure 3. Dynamic Response

The outputs can withstand an indefinite short-circuit to AGND to typically 50 mA. The output may also be shorted to any voltage between V_{DD} and V_{SS}; however, care must be taken to not exceed the device maximum power dissipation.

The amplifier's emitter follower output stage consists of an intrinsic NPN bipolar transistor with a 400 µA NMOS pull-down current-source load connected to V_{SS}. This circuit configuration shown in Figure 4 enables the output amplifier to develop output voltages very close to AGND. Only the negative supply of the four output buffer amplifiers are connected to V_{SS}. Operating the DAC8426 from dual supplies (V_{DD} = +15 V and V_{SS} = –5 V) improves negative going output settling time near zero volts.

When operating single supply (V_{DD} = +15 V and V_{SS} = 0 V) the output sink current decreases as the output approaches zero voltage. Within 200 mV of AGND (single-supply operation) the internal sinking capability appears resistive at a value of approximately 1200 Ω. The buffer amplifier output current and voltage characteristics are plotted in Figure 5.

APPLICATIONS SETUP

UNIPOLAR OUTPUT OPERATION

The output voltage appearing at any output V_{OUT} is equal to the internal 10 V reference multiplied by the decimal value of the latched digital input divided by 2^8 (= 256). In equation form:

$$V_{OUT}(D) = D/256 \times 10\ V$$

where $D = 0_{10}$ *to* 255_{10}

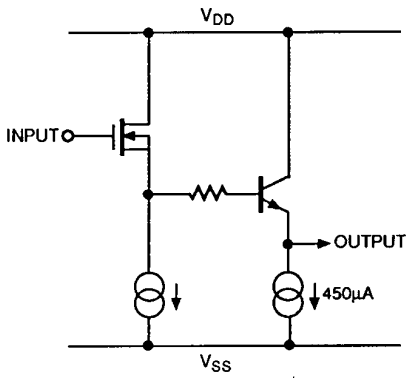


Figure 4. Amplifier Output Stage

Note that the maximum possible output is 1 LSB less than the internal 10 V reference, that is, 255/256 × 10 V = 9.961 V. Table II lists output voltages for a given digital input. The total unadjusted error (TUE) specification of the product grade used determines the output tolerances of the values listed in Table II. For example, a ±2 LSB grade DAC8426FP loaded with decimal 128_{10} (half-scale) would have a guaranteed output voltage occurring in the range of 5 V ±2 LSB, which is 5 V ±(2 × 10 V/256) = 5 V ±0.078 V. Therefore V_{OUT} is guaranteed to occur in the following range:

$$4.922\ V \le V_{OUT}(128) \le 5.078\ V$$

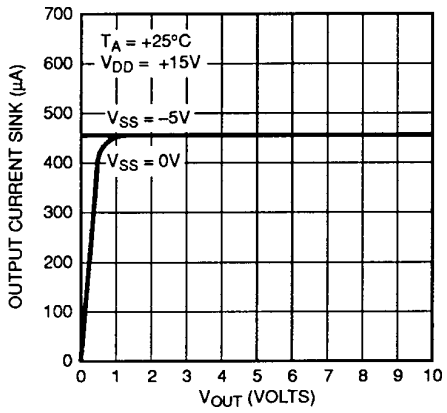


Figure 5. DAC Output Current Sink

For the top grade DAC8426EP ±1 LSB total unadjusted error (TUE), the guaranteed range is 4.961 V ≤ V_{OUT} (128_{10}) ≤ 5.039 V. These tolerances provide the worst case analysis including temperature changes.

One additional characteristic guaranteed is a DNL of ±1 LSB on all grades. The DAC8426 is therefore guaranteed to be monotonic. In the situation where a continuously positive 1 LSB digital increment is applied, the output voltage will always increase in value, never decrease. This is very important is servo applications and other closed-loop feedback systems. Finally, in the typical characteristic curves, long term output voltage drift (stability) is provided.

BIPOLAR OUTPUT OPERATION

An external op amp plus two resistors can easily convert any DAC output to bipolar output voltage swings. Figure 6 shows all four DACs output operating in bipolar mode. This is the general expression describing the bipolar output transfer equation:

$$V_{OUT}(D) = [(1 + R_2/R_1) \times D/256 \times 10\ V] - R_2/R_1 \times 10\ V,$$

where $D = 0_{10}$ to 255_{10}

If $R_1 = R_2$, then V_{OUT} becomes:

$$V_{OUT}\ (D) = (D/128 - 1) \times 10\ V$$

Table III lists various output voltages with $R_1 = R_2$ versus digital input code. This coding is considered offset binary. Note that the LSB step size is now 20 V/256 = 0.078 V, twice as large as the unipolar output case previously discussed. In order to minimize gain and offset errors, choose R_1 and R_2 to match and track within 0.1% over the selected operating temperature range of interest.

Table II. Unipolar Output Voltage as a Function of Digital Input Code

Digital Input Code	Analog Output Voltage (= D/256 × 10 V)	
255	9.961 V	Full-Scale (FS)
254	9.922 V	FS-1 LSB
129	5.039 V	
128	5.000 V	Half-Scale
127	4.961 V	
1	0.039 V	1 LSB
0	0.000 V	Zero-Scale

OFFSETTING AGND

Since the DAC ladder and bandgap reference are terminated at AGND, it is possible to offset AGND positive with respect to DGND. The 10 V output span remains if a positive offset is applied to AGND. The offset voltage source connected to AGND must be capable of sinking 14 mA. AGND cannot be taken negative with respect to DGND; this would forward bias an internal diode. Allowance must be made at V_{DD} to maintain 3.5 V of headroom above V_{REF}OUT. This connection setup is useful in single supply applications where virtual ground needs to be slightly positive with respect to ground. In this application connect V_{SS} to DGND to take advantage of the extra buffer output current sinking capability when the DAC output is programmed to all zeros code, see Figure 7.

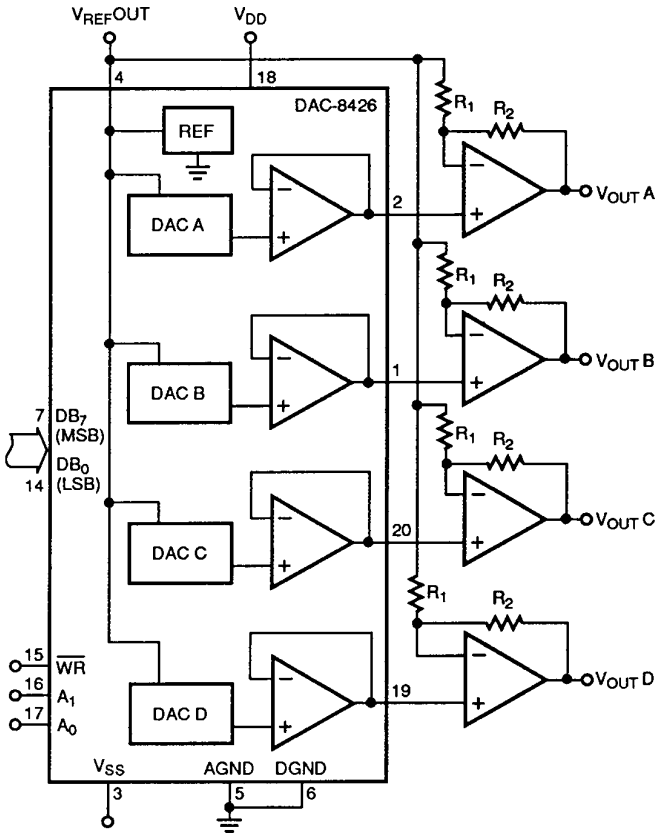


Figure 6. Bipolar Operation

Table III. Bipolar Output Voltage as a Function of Digital Input Code

Digital Input Code	Analog Output Voltage (= D/256 × 10 V)	
255	9.922 V	Full-Scale (FS)
254	9.844 V	FS-1 LSB
129	0.078 V	
128	0.000 V	Zero-Scale
127	–0.078 V	
1	–9.922 V	
0	–10.000 V	Neg Full-Scale

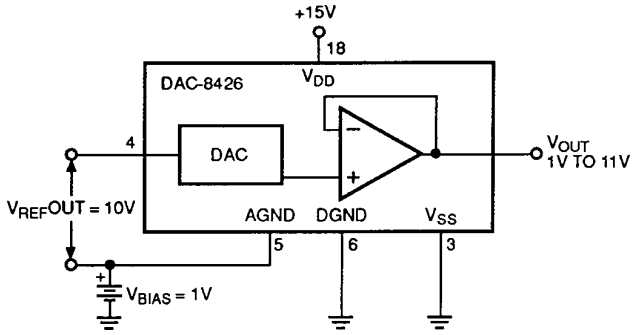


Figure 7. AGND Biasing Scheme Providing Offset Output Range

CONNECTION AND LAYOUT GUIDELINES

Layout and design techniques used in the interface between digital and analog circuitry require special attention to detail. The following considerations should be evaluated prior to PCB layout.

1. Return signal paths through the ground system should be carefully considered. High-speed digital logic current pulses traveling on return ground traces generate glitches that can be radiated to the analog circuits if the ground path layout produces loop antennas. Ground planes can minimize this situation. Separate digital and analog grounding areas to minimize crosstalk. Ideally a single common-point ground should be on the same PCB board as the DAC8426. The analog ground returns should take advantage of the appropriate placement of power supply bypass capacitors.
2. For optimum performance, bypass V_{DD} and V_{SS} (if using negative supply voltage) with 0.1 µF ceramic disk capacitors to shunt high-frequency spikes. Also use in parallel 6.8 µF to 10 µF capacitors to provide a charge reservoir for lower frequency load change requirements. The reference output ($V_{REF}OUT$) should be bypassed with a 10 µF tantalum capacitor to optimize reference output stability during data input changes. This helps to minimize digital crosstalk.
3. Power Supply Sequencing—No special requirements exist with the DAC8426. However, users should be aware that often the 5 V logic supply may be powered up momentarily prior to the +15 V analog supply. In this situation, the DAC8426 ESD input protection diodes will forward bias if the applied input logic is at logic "1". No damage will result to the input since the DAC8426 is designed to withstand momentary currents of up to 130 mA. This situation will likely exist for any DAC or ADC operating from a separate analog supply.
4. ESD input protection—Attention has been given in the design of the DAC8426 to ESD sensitivity. Using the human body model test technique (MIL-STD 3015.4) the DAC8426 generally will withstand 1500 V ESD transients on all pins. Handling and testing prior to PCB insertion generally exposes ICs to the toughest environment they will experience. Once the IC is soldered in the PCB, it is still important to consider any traces that connect to PCB edge connectors. These traces should be protected with appropriate devices especially if the boards will experience field replacement or adjustment. Handling the exposed edge connectors by field maintenance people in a low humidity environment can produce 20 kV ESD transients which will be detrimental to almost any integrated IC connected to the edge connector.

MICROPROCESSOR INTERFACING

The DAC8426 easily interfaces to most 8- and 16-bit wide databus systems. Serial and 4-bit busses can also be accommodated with additional latches and control circuitry. Interfacing can be accomplished with databus transfers running with 50 ns write pulse widths.

Examples of various microprocessor interface circuits are provided in Figures 8 through 12. These figures have omitted circuitry not essential to the bus interface. The design process should include review of the DAC8426 timing diagram with the µP system timing diagram.

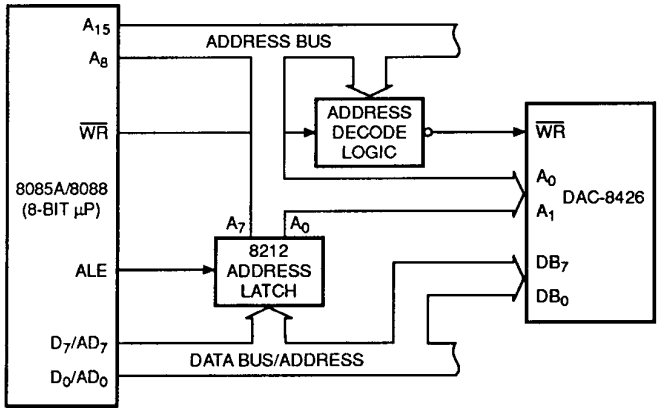


Figure 8. DAC8426 to 8085A Interface (Simplified circuit, only lines of interest are shown.)

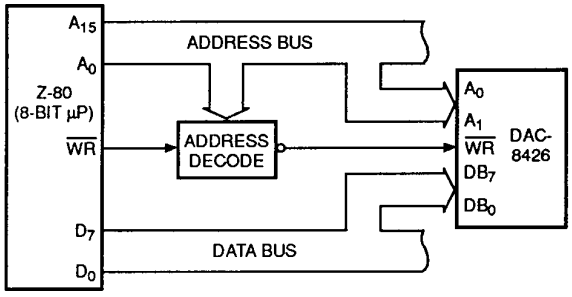


Figure 9. DAC8426 to Z-80 Interface (Simplified circuit, only lines of interest are shown.)

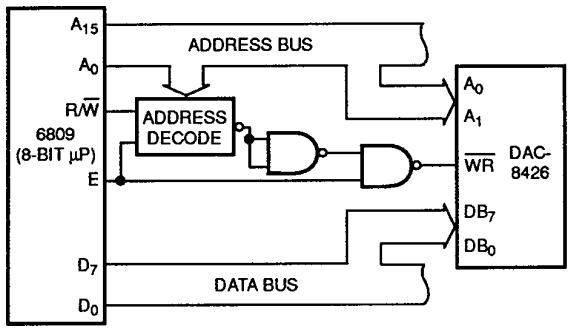


Figure 10. DAC8426 to 6809 Interface (Simplified circuit, only lines of interest are shown.)

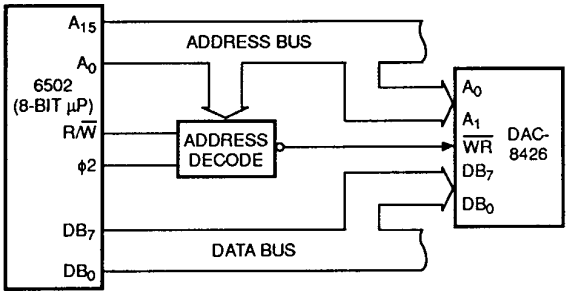


Figure 11. DAC8426 to 6502 Interface (Simplified circuit, only lines of interest are shown.)

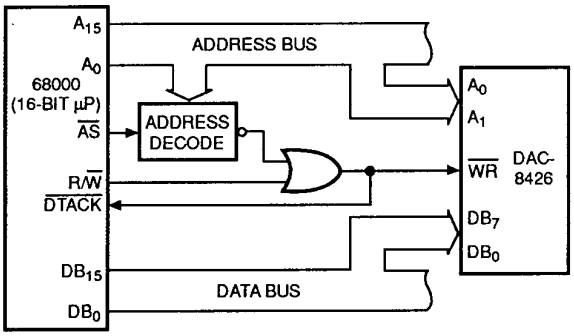
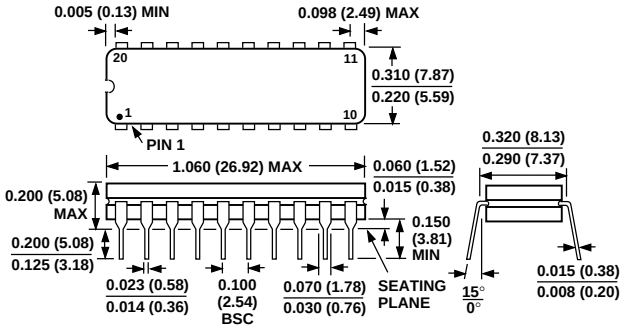


Figure 12. DAC8426 to 68000 Interface (Simplified circuit, only lines of interest are shown.)

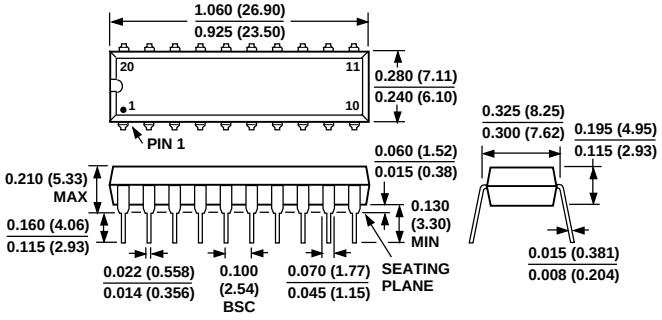
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

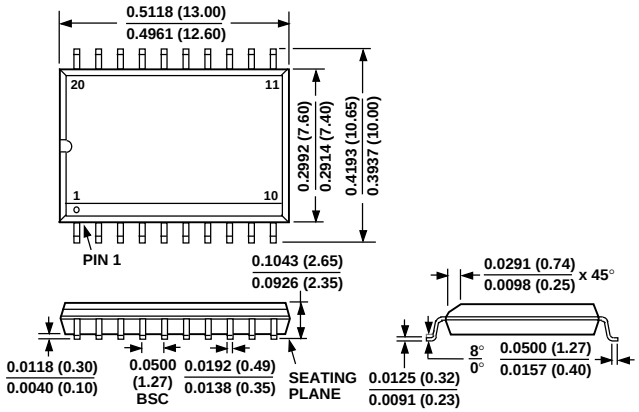
20-Pin Cerdip
(Q-20)



20-Pin Plastic DIP
(N-20)



20-Lead SOL
(R-20)



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- Техническая поддержка проекта;
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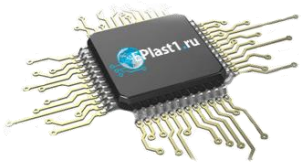

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