74AHC164; 74AHCT164

8-bit serial-in/parallel-out shift register

Rev. 03 — 24 April 2008 Product data sheet

1. General description

The 74AHC164; 74AHCT164 shift register is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7A.

The 74AHC164; 74AHCT164 input signals are 8-bit serial through one of two inputs (DSA or DSB); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock input (CP) and enters into output Q0, which is a logical AND of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW-level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
  - For 74AHC164: CMOS level
  - For 74AHCT164: TTL level
- ESD protection:
  - HBM EIA/JESD22-A114E exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
  - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC164				
74AHC164D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHC164PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHC164BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT164				
74AHCT164D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT164PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT164BQ	–40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

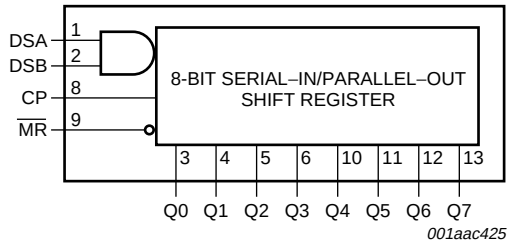

Fig 1. Functional diagram

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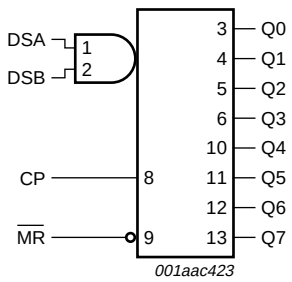

Fig 2. Logic symbol

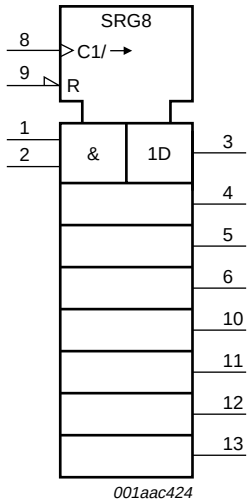

Fig 3. IEC logic symbol

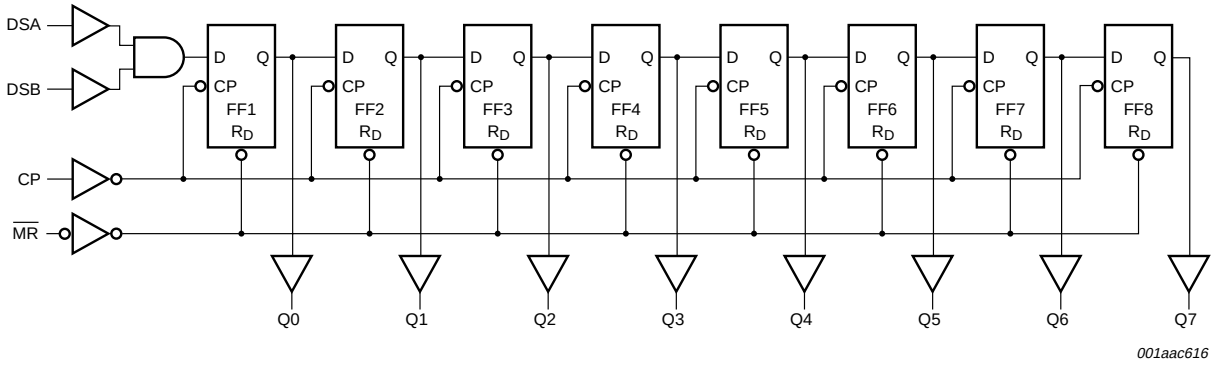

Fig 4. Logic diagram

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5. Pinning information

5.1 Pinning

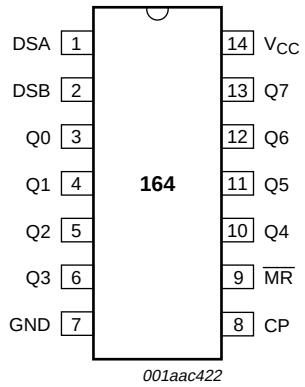
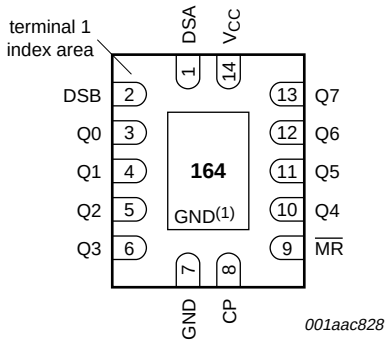


Fig 5. Pin configuration SO14 and TSSOP14



Transparent top view

(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig 6. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
DSA	1	serial data input A
DSB	2	serial data input B
Q0	3	output 0
Q1	4	output 1
Q2	5	output 2
Q3	6	output 3
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH edge-triggered)
$\overline{MR}$	9	master reset input (active LOW)
Q4	10	output 4
Q5	11	output 5
Q6	12	output 6
Q7	13	output 7
V_{CC}	14	supply voltage

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6. Functional description

Table 3. Function table[1]

Operating mode	Control		Input		Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
			l	h	L	q0 to q6
			h	l	L	q0 to q6
			h	h	H	q0 to q6

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑ = LOW-to-HIGH transition;
X = don't care;
q = lower case letter indicates the state of the referenced input one set-up time prior to the LOW-to-HIGH transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage			–0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1]	–20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	–20	+20	mA
I_O	output current	$V_O = -0.5$ V to ($V_{CC} + 0.5$ V)		–25	+25	mA
I_{CC}	supply current			-	+75	mA
I_{GND}	ground current			–75	-	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
For DHVQFN14 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

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8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC164						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT164						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC164										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V_{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V_{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V_{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V_{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = –50 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –50 μA; V_{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I_O = –50 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I_O = –8.0 mA; V_{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		I_O = 50 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 50 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I_O = 8.0 mA; V_{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

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Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C_I	input capacitance		-	3	10	-	-	-	-	pF
74AHCT164										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = –50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1$ V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance		-	3	10	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
74AHC164											
t_{pd}	propagation delay	CP to Qn; see Figure 7	[2]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	6.5	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50 pF		-	9.3	16.3	1.0	18.5	1.0	20.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.5	9.0	1.0	10.5	1.0	11.5	ns
		C_L = 50 pF		-	6.4	11.0	1.0	12.5	1.0	14.0	ns
		$\overline{MR}$ to Qn; see Figure 8	[3]								
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		-	5.3	12.8	1.0	15.0	1.0	16.0	ns
		C_L = 50 pF		-	7.6	16.3	1.0	18.5	1.0	20.5	ns
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		-	4.0	8.6	1.0	10.0	1.0	11.0	ns
		C_L = 50 pF		-	5.8	10.6	1.0	12.0	1.0	13.5	ns
f_{max}	maximum frequency	see Figure 7									
		V_{CC} = 3.0 V to 3.6 V									
		C_L = 15 pF		80	125	-	65	-	50	-	MHz
		C_L = 50 pF		50	75	-	45	-	35	-	MHz
		V_{CC} = 4.5 V to 5.5 V									
		C_L = 15 pF		125	175	-	105	-	85	-	MHz
		C_L = 50 pF		85	115	-	75	-	65	-	MHz
t_W	pulse width	CP HIGH or LOW; see Figure 7									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	5.0	-	5.0	-	ns
t_{WL}	pulse width LOW	$\overline{MR}$; see Figure 8									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	5.0	-	5.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DSA, DSB to CP; see Figure 9									
		V_{CC} = 3.0 V to 3.6 V		5.0	-	-	6.0	-	6.0	-	ns
		V_{CC} = 4.5 V to 5.5 V		4.5	-	-	4.5	-	4.5	-	ns
t_h	hold time	DSA, DSB to CP; see Figure 9									
		V_{CC} = 3.0 V to 3.6 V		1.5	-	-	1.5	-	1.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.0	-	-	2.0	-	2.0	-	ns

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Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	Min	Max	
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8									
		V_{CC} = 3.0 V to 3.6 V		2.5	-	-	2.5	-	2.5	-	ns
		V_{CC} = 4.5 V to 5.5 V		2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	48	-	-	-	-	-	pF
74AHCT164; V_{CC} = 4.5 V to 5.5 V											
t_{pd}	propagation delay	CP to Qn; see Figure 7	[2]								
		C_L = 15 pF		-	3.4	9.0	1.0	10.5	1.0	11.5	ns
		C_L = 50 pF		-	4.9	11.0	1.0	12.5	1.0	14.0	ns
		$\overline{MR}$ to Qn; see Figure 8	[3]								
		C_L = 15 pF		-	3.5	8.6	1.0	10.0	1.0	11.0	ns
		C_L = 50 pF		-	5.0	10.6	1.0	12.0	1.0	13.5	ns
f_{max}	maximum frequency	see Figure 7									
		C_L = 15 pF		125	175	-	105	-	85	-	MHz
		C_L = 50 pF		85	115	-	75	-	65	-	MHz
t_W	pulse width	CP HIGH or LOW; see Figure 7		5.0	-	-	5.0	-	5.0	-	ns
t_{WL}	pulse width LOW	$\overline{MR}$; see Figure 8		5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	DSA, DSB to CP; see Figure 9		4.5	-	-	4.5	-	4.5	-	ns
t_h	hold time	DSA, DSB to CP; see Figure 9		2.0	-	-	2.0	-	2.0	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP; see Figure 8		2.5	-	-	2.5	-	2.5	-	ns
C_{PD}	power dissipation capacitance	f_i = 1 MHz; V_I = GND to V_{CC}	[4]	-	51	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] t_{pd} is the same as t_{PHL} only.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

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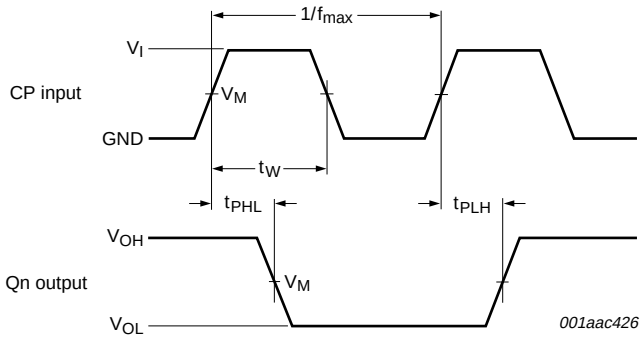
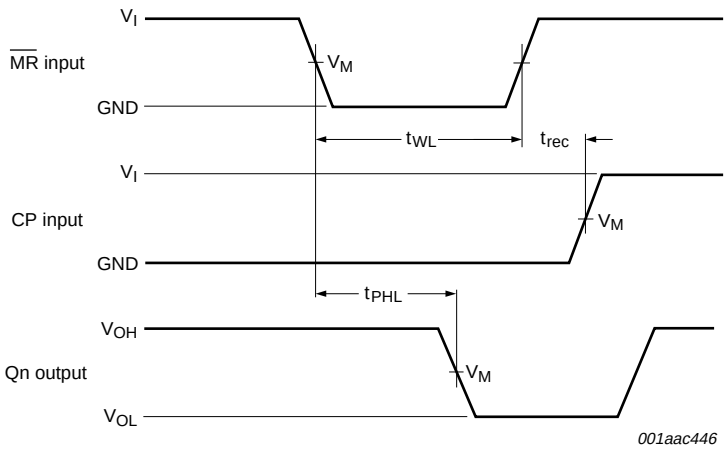
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. Clock pulse width, maximum frequency and input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 8. Master reset pulse width, recovery time and propagation delays

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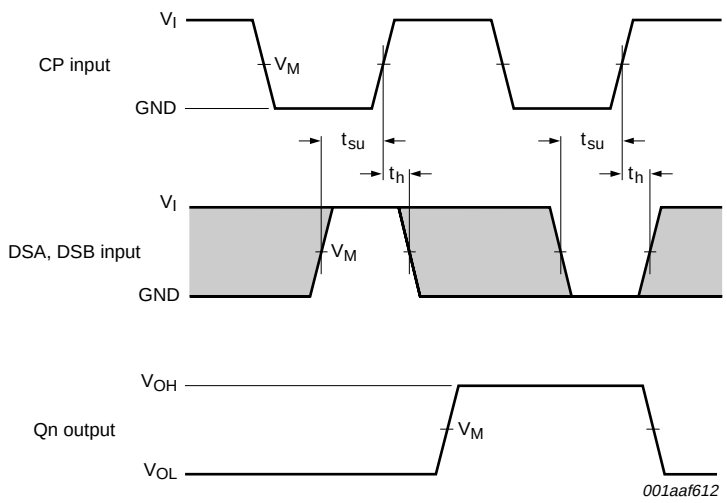

Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Data set-up and hold times

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC164	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT164	1.5 V	$0.5 \times V_{CC}$

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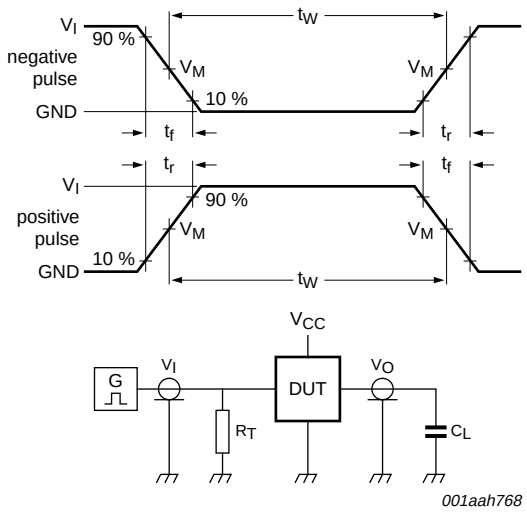

Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

Fig 10. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC164	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT164	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

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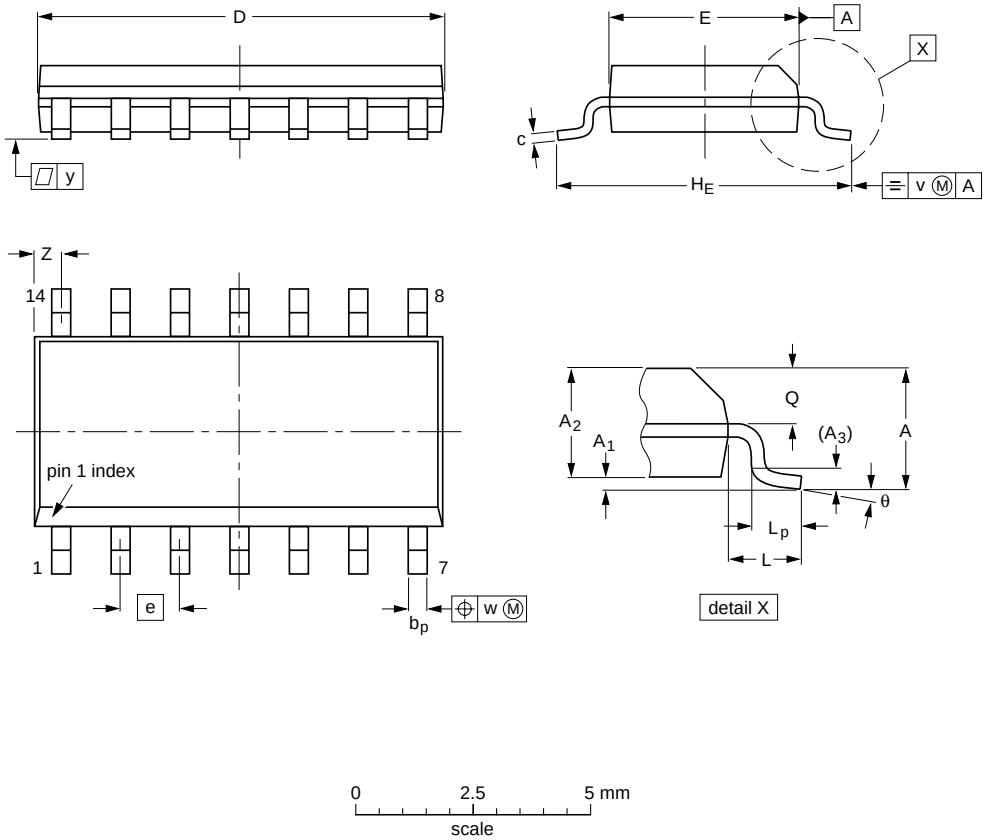
12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT108-1 (SO14)

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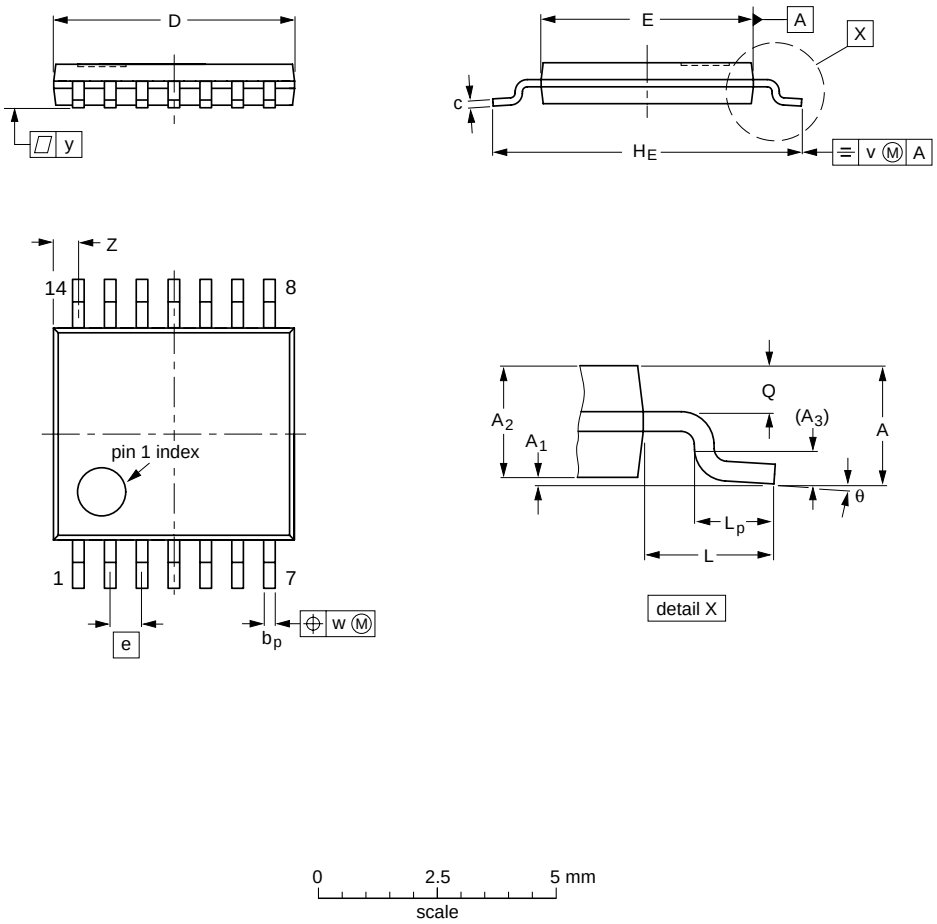
TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 12. Package outline SOT402-1 (TSSOP14)

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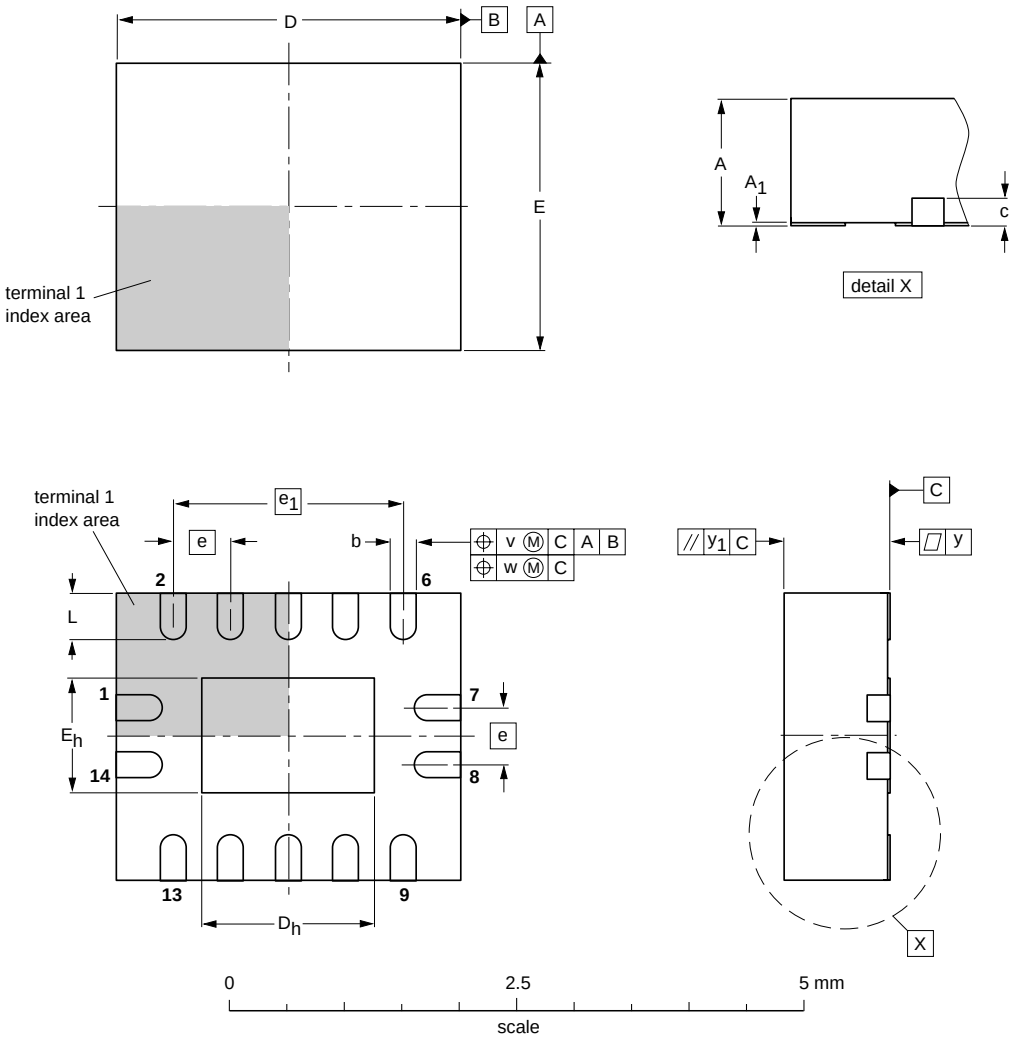
DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	- - -	MO-241	- - -			~~02-10-17~~ 03-01-27

Fig 13. Package outline SOT762-1 (DHVQFN14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT164_3	20080424	Product data sheet	-	74AHC_AHCT164_2
Modifications:	• Table 6: the conditions for input leakage current have been changed.			
74AHC_AHCT164_2	20061129	Product data sheet	-	74AHC_AHCT164_1
74AHC_AHCT164_1 (9397 750 07332)	20000815	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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