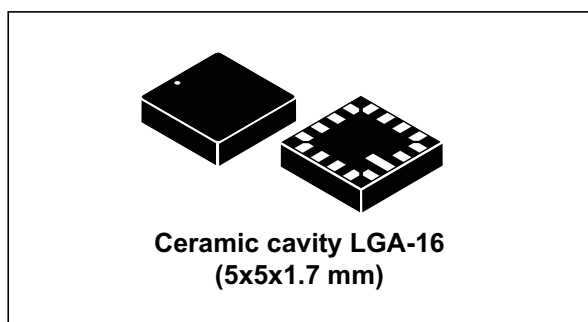


MEMS motion sensor: three-axis digital output accelerometer

Datasheet - production data



Features

- 3-axis, $\pm 2.5 g$ full-scale
- Ultra-low noise performance: $45 \mu g/\sqrt{Hz}$
- Excellent stability over temperature ($<0.4 mg/^\circ C$) and time
- 16-bit data output
- SPI 4-wire digital output interface
- Embedded temperature sensor
- 12-bit temperature data output
- Embedded FIFO (depth 32 levels)
- High shock survivability
- Extended operating temperature range ($-40^\circ C$ to $+85^\circ C$)
- ECOPACK[®], RoHS and “Green” compliant

Applications

- Precision inclinometer
- Platform and antenna stabilization
- Leveling instruments

Description

The LIS3DHH is an ultra-high-resolution and low-noise three-axis linear accelerometer.

The LIS3DHH has a full scale of $\pm 2.5 g$ and is capable of providing the measured accelerations to the application through an SPI 4-wire digital interface.

The sensing element is manufactured using a dedicated micromachining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LIS3DHH is available in a high-performance (low-stress) ceramic cavity land grid array (CC LGA) package and can operate within a temperature range of $-40^\circ C$ to $+85^\circ C$.

Table 1. Device summary

| Order codes | Temperature range [$^\circ C$] | Package | Packaging |
|-------------|----------------------------------|------------------------|---------------|
| LIS3DHHTR | -40 to $+85$ | CC LGA-16 (5x5x1.7 mm) | Tape and reel |

Contents

- 1 Pin description 6**
- 2 Mechanical and electrical specifications 7**
 - 2.1 Mechanical characteristics 7
 - 2.2 Electrical characteristics 8
 - 2.2.1 Recommended power-up sequence 9
 - 2.3 Temperature sensor characteristics 9
- 3 Absolute maximum ratings 10**
- 4 Communication interface characteristics 11**
 - 4.1 SPI - serial peripheral interface 11
 - 4.2 SPI bus interface 12
 - 4.2.1 SPI read 13
 - 4.2.2 SPI write 14
- 5 FIFO 15**
 - 5.1 Bypass mode 15
 - 5.2 FIFO mode 16
 - 5.3 Continuous mode 17
 - 5.4 Continuous-to-FIFO mode 18
 - 5.5 Bypass-to-Continuous mode 19
- 6 Register mapping 20**
- 7 Register description 21**
 - 7.1 WHO_AM_I (0Fh) 21
 - 7.2 CTRL_REG1 (20h) 21
 - 7.3 INT1_CTRL (21h) 22
 - 7.4 INT2_CTRL (22h) 22
 - 7.5 CTRL_REG4 (23h) 23
 - 7.6 CTRL_REG5 (24h) 23
 - 7.7 OUT_TEMP_L (25h), OUT_TEMP_H (26h) 24



| | | |
|----------|----------------------------------|-----------|
| 7.8 | STATUS (27h) | 24 |
| 7.9 | OUT_X (28h - 29h) | 25 |
| 7.10 | OUT_Y (2Ah - 2Bh) | 25 |
| 7.11 | OUT_Z (2Ch - 2Dh) | 25 |
| 7.12 | FIFO_CTRL (2Eh) | 25 |
| 7.13 | FIFO_SRC (2Fh) | 26 |
| 8 | Package information | 27 |
| 8.1 | LGA-16 package information | 27 |
| 9 | Revision history | 28 |

List of tables

| | | |
|-----------|--|----|
| Table 1. | Device summary | 1 |
| Table 2. | Pin description | 6 |
| Table 3. | Mechanical characteristics | 7 |
| Table 4. | Electrical characteristics | 8 |
| Table 5. | Temperature sensor characteristics | 9 |
| Table 6. | Absolute maximum ratings | 10 |
| Table 7. | SPI slave timing values | 11 |
| Table 8. | Register mapping | 20 |
| Table 9. | WHO_AM_I register | 21 |
| Table 10. | CTRL_REG1 register | 21 |
| Table 11. | CTRL_REG1 register description | 21 |
| Table 12. | INT1_CTRL register | 22 |
| Table 13. | INT1_CTRL register description | 22 |
| Table 14. | INT2_CTRL register | 22 |
| Table 15. | INT2_CTRL register description | 22 |
| Table 16. | CTRL_REG4 register | 23 |
| Table 17. | CTRL_REG4 register description | 23 |
| Table 18. | Self-test mode selection | 23 |
| Table 19. | CTRL_REG5 register | 23 |
| Table 20. | CTRL_REG5 register description | 23 |
| Table 21. | OUT_TEMP_L register | 24 |
| Table 22. | OUT_TEMP_H register | 24 |
| Table 23. | OUT_TEMP register description | 24 |
| Table 24. | Status register | 24 |
| Table 25. | Status register description | 24 |
| Table 26. | FIFO_CTRL register | 25 |
| Table 27. | FIFO_CTRL register description | 25 |
| Table 28. | FIFO mode selection | 25 |
| Table 29. | FIFO_SRC register | 26 |
| Table 30. | FIFO_SRC register description | 26 |
| Table 31. | FIFO_SRC example: OVR/FSS details | 26 |
| Table 32. | Outer dimensions | 27 |
| Table 33. | Document revision history | 28 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Pin connections | 6 |
| Figure 2. | Recommended power-up sequence | 9 |
| Figure 3. | SPI slave timing diagram | 11 |
| Figure 4. | Read and write protocol | 12 |
| Figure 5. | SPI read protocol | 13 |
| Figure 6. | Multiple byte SPI read protocol (2-byte example) | 13 |
| Figure 7. | SPI write protocol | 14 |
| Figure 8. | Multiple byte SPI write protocol (2-byte example) | 14 |
| Figure 9. | Bypass mode | 15 |
| Figure 10. | FIFO mode | 16 |
| Figure 11. | Continuous mode | 17 |
| Figure 12. | Continuous-to-FIFO mode | 18 |
| Figure 13. | External asynchronous trigger to FIFO for Continuous-to-FIFO mode | 18 |
| Figure 14. | Bypass-to-Continuous mode | 19 |
| Figure 15. | External asynchronous trigger to FIFO for Bypass-to-Continuous mode | 19 |
| Figure 16. | Continuous mode: FTH/FSS details | 26 |
| Figure 17. | Ceramic cavity LGA-16: package outline and mechanical data | 27 |

1 Pin description

Figure 1. Pin connections

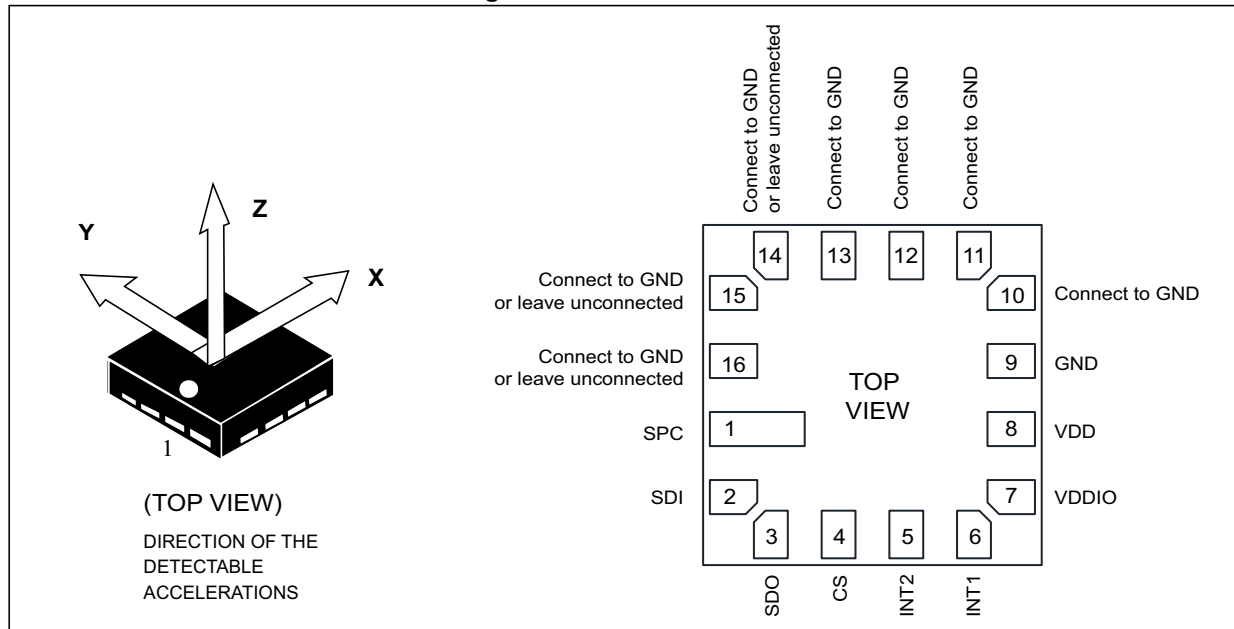


Table 2. Pin description

| Pin# | Name | Function |
|------|----------|---|
| 1 | SPC | Clock line for SPI 4-wire interface (SPC) |
| 2 | SDI | Serial data input (SDI) line for SPI 4-wire interface |
| 3 | SDO | Serial data output (SDO) line for SPI 4-wire interface |
| 4 | CS | SPI chip-select line (CS) |
| 5 | INT2 | Programmable interrupt 2 generated according to a configurable FIFO threshold in a dedicated register |
| 6 | INT1 | Programmable interrupt 1 generated according to a configurable FIFO threshold in a dedicated register |
| 7 | Vdd_IO | Power supply for I/O pins Recommended power supply decoupling capacitor (100 nF) |
| 8 | Vdd | Power supply Recommended power supply decoupling capacitors (100 nF ceramic in parallel with 10 µF aluminum) |
| 9 | GND | 0 V power supply |
| 10 | Reserved | Connect to GND |
| 11 | Reserved | Connect to GND |
| 12 | Reserved | Connect to GND |
| 13 | Reserved | Connect to GND |
| 14 | Reserved | Connect to GND or leave unconnected |
| 15 | Reserved | Connect to GND or leave unconnected |
| 16 | Reserved | Connect to GND or leave unconnected |

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 2.8 V, T = 25 °C unless otherwise noted.

Table 3. Mechanical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--------|--|---|----------|---------------------|-------------|----------|
| FS | Measurement range ⁽²⁾ | | | ±2.5 | | g |
| So | Sensitivity ⁽³⁾ | | | 0.076 | | mg/digit |
| TCSO | Sensitivity change vs. temperature | From -40 °C to +85 °C, delta from 25°C | | 0.7 | | % |
| Off | Zero-g level offset accuracy ⁽⁴⁾ | | | ±20 | | mg |
| TCOff | Zero-g level change vs. temperature ⁽⁵⁾ | From -40 °C to +85 °C, delta from 25 °C | -0.4 | | 0.4 | mg/°C |
| NL | Non linearity | Best-fit straight line | | | 2 | % FS |
| Zgn | Zero-g noise density | FS = ±2.5 g | | 45 | 65 | ug/(√Hz) |
| ODR | Digital output data rate | | | 1.1 | | kHz |
| Bw | Bandwidth | For both FIR and IIR filters | | 235 or 440 | | Hz |
| StartT | Startup time | For cold start condition | | | 150 | ms |
| ST | Self-test positive difference ⁽⁶⁾ | X, Y-axis Z-axis | 75 75 | | 650 1400 | mg |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. Sensor is designed with larger dynamic to avoid variation of FS limits in the operative bandwidth. Consequently to trim operations at factory final test.
3. Sensitivity range after MSL3 preconditioning.
4. Typical zero-g level offset value after MSL3 preconditioning.
5. Min/max at 3 sigma. Based on characterization data for a limited number of samples, not measured during final test for production.
6. Self-test positive difference is defined as:

$$\text{OUTPUT}[\text{mg}](\text{CTRL_REG4 (23h)}_{\text{ST2, ST1 bits} = 01}) - \text{OUTPUT}[\text{mg}](\text{CTRL_REG4 (23h)}_{\text{ST2, ST1 bits} = 00})$$
 in steady state.

2.2 Electrical characteristics

@ Vdd = 2.8 V, T = 25 °C unless otherwise noted.

Table 4. Electrical characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|-----------------|--|---------------------------------------|--------------|---------------------|------------|------|
| Vdd | Supply voltage | | 1.71 | 2.8 | 3.6 | V |
| Vdd_IO | I/O pins supply voltage | | 1.71 | | Vdd+0.1 | V |
| Idd | Supply current | | | 2.5 | 5 | mA |
| V _{IH} | Digital high-level input voltage | | 0.7*Vdd_IO | | | V |
| V _{IL} | Digital low-level input voltage | | | | 0.3*Vdd_IO | V |
| V _{OH} | High-level output voltage | I _{OH} = 4 mA ⁽²⁾ | Vdd_IO - 0.2 | | | V |
| V _{OL} | Low-level output voltage | I _{OL} = 4 mA ⁽²⁾ | | | 0.2 | V |
| Top | Operating temperature range | | -40 | | +85 | °C |
| SPI_Fr | SPI frequency | 4-wire interface | | 5 | 10 | MHz |
| Trise | Time for power supply rising ⁽³⁾ | | 0.01 | | 100 | ms |
| Twait | Time delay between Vdd_IO and Vdd ⁽³⁾ | | 0 | | 10 | ms |

1. Typical specifications are not guaranteed.
2. 4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.
3. Please refer to [Section 2.2.1: Recommended power-up sequence](#) for more details.

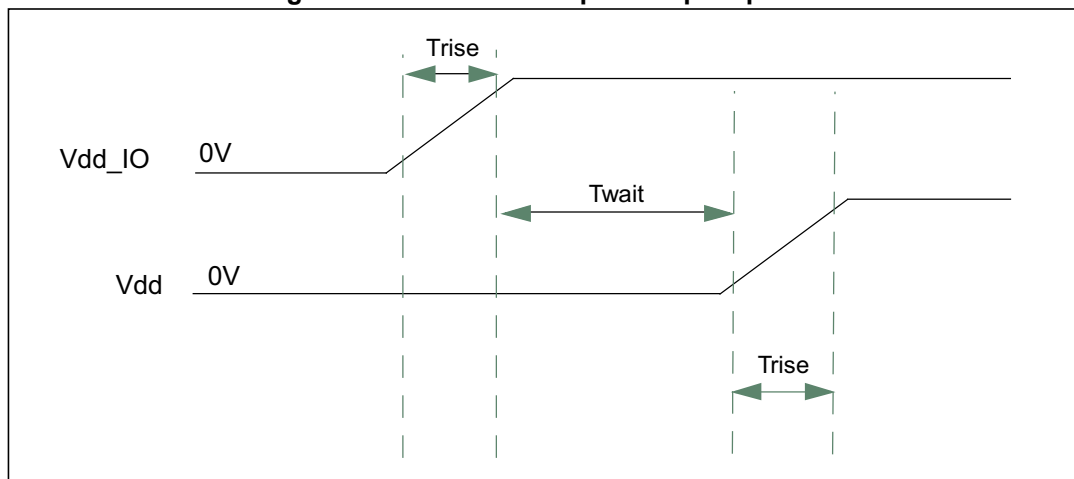
2.2.1 Recommended power-up sequence

For the power-up sequence please refer to the following figure, where:

- Trise is the time for the power supply to rise from 10% to 90% of its final value
- Twait is the time delay between the end of the Vdd_IO ramp (90% of its final value) and the start of the Vdd ramp

In the power-down sequence Vdd and Vdd_IO can come down in any order.

Figure 2. Recommended power-up sequence



2.3 Temperature sensor characteristics

@ Vdd = 2.8 V, T = 25 °C unless otherwise noted.

Table 5. Temperature sensor characteristics

| Symbol | Parameter | Test condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|--------|--|------------------------|------|---------------------|------|----------|
| TSDr | Temperature sensor output change vs. temperature | | | 16 | | digit/°C |
| Tn | Temperature sensor noise (RMS) | | | | 0.1 | °C |
| Ta | Temperature accuracy | | -15 | | +15 | °C |
| TODR | Temperature refresh rate | equal to ODR/16 | 62.5 | | | Hz |
| TNL | Temperature nonlinearity | Best-fit straight line | | 5 | | % Top |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.

3 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute maximum ratings

| Symbol | Ratings | Maximum value | Unit |
|------------------|--|---------------------|------|
| Vdd and Vdd_IO | Supply voltage | -0.3 to 4.8 | V |
| T _{STG} | Storage temperature range | -40 to +85 | °C |
| Sg | Acceleration g for 0.2 ms | 10,000 | g |
| ESD | Electrostatic discharge protection (HBM) | 2 | kV |
| V _{in} | Input voltage on any control pin (including CS, SPC, SDI, SDO) | -0.3 to Vdd_IO +0.3 | V |

Note: Supply voltage on any pin should never exceed 4.8 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4 Communication interface characteristics

4.1 SPI - serial peripheral interface

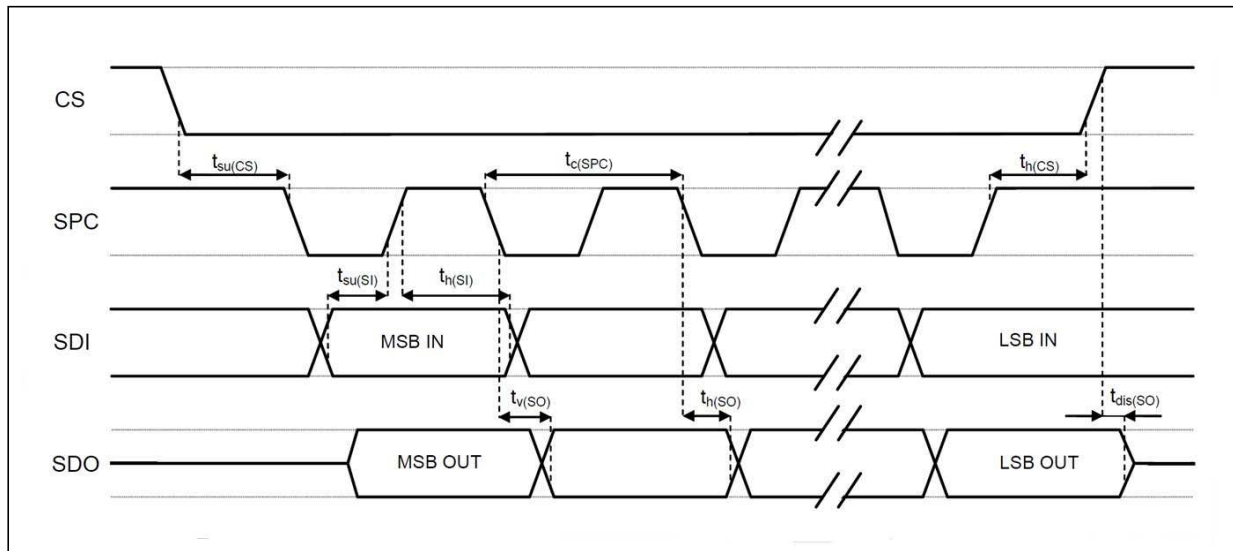
Subject to general operating conditions for Vdd and Top.

Table 7. SPI slave timing values

| Symbol | Parameter | Value ⁽¹⁾ | | Unit |
|---------------|-------------------------|----------------------|-----|------|
| | | Min | Max | |
| $t_{c(SPC)}$ | SPI clock cycle | 100 | | ns |
| $f_{c(SPC)}$ | SPI clock frequency | | 10 | MHz |
| $t_{su(CS)}$ | CS setup time | 5 | | ns |
| $t_{h(CS)}$ | CS hold time | 20 | | |
| $t_{su(SI)}$ | SDI input setup time | 5 | | |
| $t_{h(SI)}$ | SDI input hold time | 15 | | |
| $t_{v(SO)}$ | SDO valid output time | | 50 | |
| $t_{h(SO)}$ | SDO output hold time | 5 | | |
| $t_{dis(SO)}$ | SDO output disable time | | 50 | |

1. Values are guaranteed at 10 MHz clock frequency for SPI 4 wires, based on characterization results, not tested in production

Figure 3. SPI slave timing diagram



Note: Measurement points are done at $0.2 \cdot V_{dd_IO}$ and $0.8 \cdot V_{dd_IO}$, for both input and output ports.

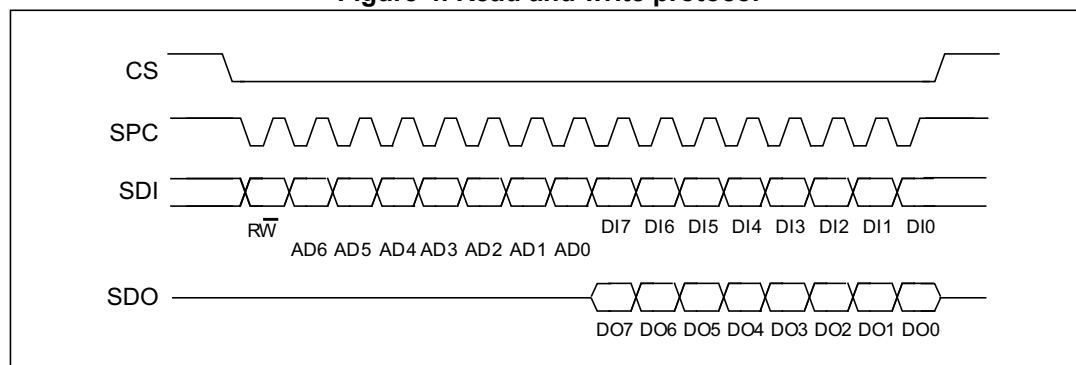
Note: The SPI state machine is reset each time the CS signal is de-asserted.

4.2 SPI bus interface

The LIS3DHH SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 4. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: \overline{RW} bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

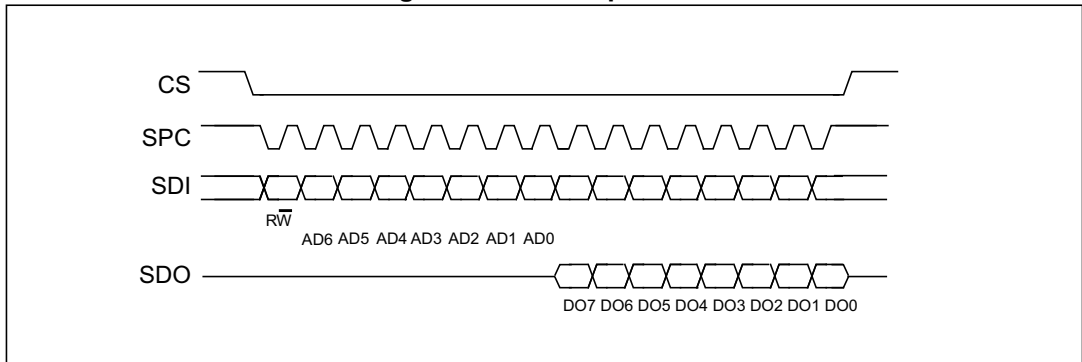
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When the [CTRL_REG1 \(20h\)](#) (IF_ADD_INC) bit is '0' the address used to read/write data remains the same for every block. When [CTRL_REG1 \(20h\)](#)(IF_ADD_INC) bit is '1' the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

4.2.1 SPI read

Figure 5. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

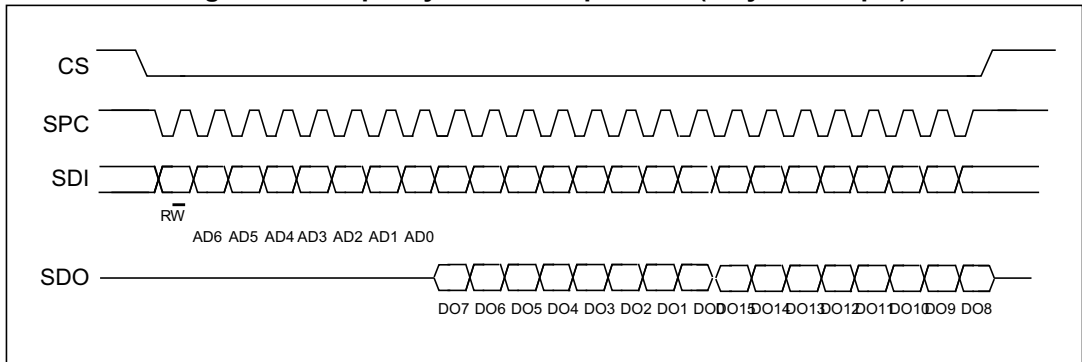
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

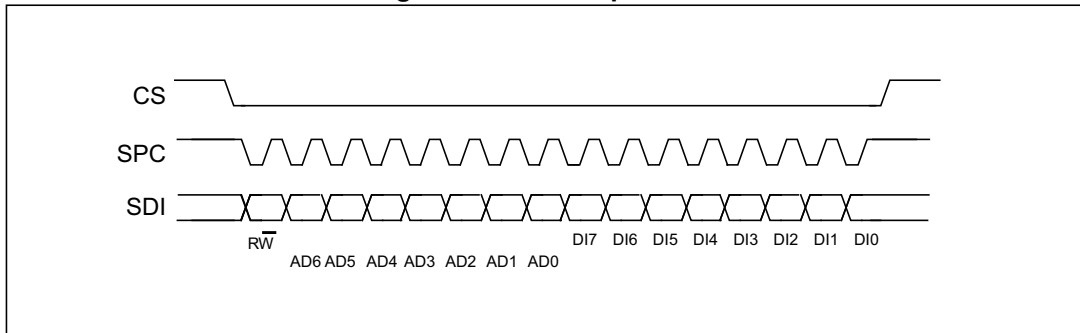
bit 16-... : data DO(...-8). Further data in multiple byte reads.

Figure 6. Multiple byte SPI read protocol (2-byte example)



4.2.2 SPI write

Figure 7. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

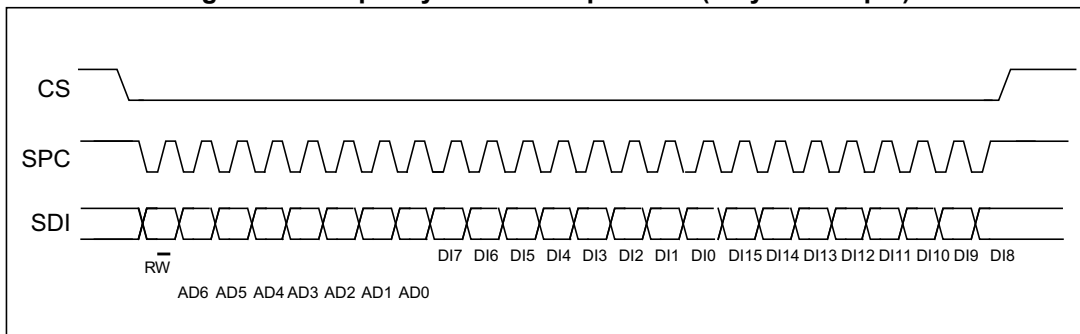
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 8. Multiple byte SPI write protocol (2-byte example)



5 FIFO

The LIS3DHH embeds 32 slots of 16-bit data FIFO for each of the accelerometer's three output channels, X, Y and Z. This allows consistent power saving for the system since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to five different modes: Bypass mode, FIFO mode, Continuous mode, Continuous-to-FIFO mode and Bypass-to-Continuous mode. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL (2Eh)* register. Programmable FIFO threshold status, FIFO overrun events and the number of unread samples stored are available in the *FIFO_SRC (2Fh)* register and can be set to generate dedicated interrupts on the INT1 and INT2 pins using the *INT1_CTRL (21h)* and *INT2_CTRL (22h)* registers.

FIFO_SRC (2Fh)(FTH) goes to '1' when the number of unread samples (*FIFO_SRC (2Fh)* (FSS5:0)) is greater than or equal to FTH [4:0] in *FIFO_CTRL (2Eh)*. If *FIFO_CTRL (2Eh)* (FTH[4:0]) is equal to 0, *FIFO_SRC (2Fh)*(FTH) goes to '0'.

FIFO_SRC (2Fh)(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO_SRC (2Fh)(FSS [5:0]) contains stored data levels of unread samples. When FSS [5:0] is equal to '000000', FIFO is empty. When FSS [5:0] is equal to '100000', FIFO is full and the unread samples are 32.

The FIFO feature is enabled by writing '1' in *CTRL_REG4 (23h)* (FIFO_EN).

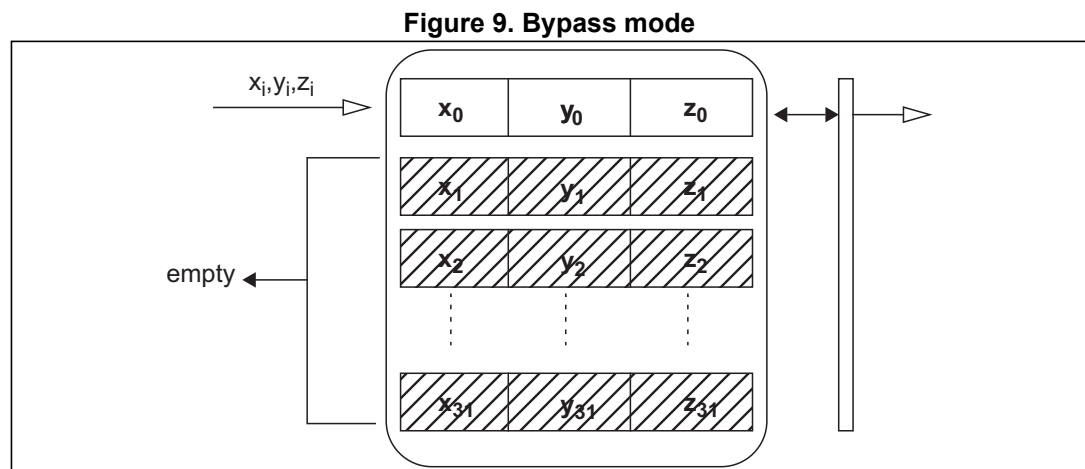
To guarantee the correct acquisition of data during the switching into and out of FIFO mode, the first sample acquired must be discarded.

5.1 Bypass mode

In Bypass mode (*FIFO_CTRL (2Eh)*(FMODE [2:0]= 000), the FIFO is not operational, no data is collected in FIFO memory, and it remains empty with the only actual sample available in the output registers.

Bypass mode is also used to reset the FIFO when in FIFO mode.

As described in *Figure 9*, for each channel only the first address is used. When new data is available the old data is overwritten.



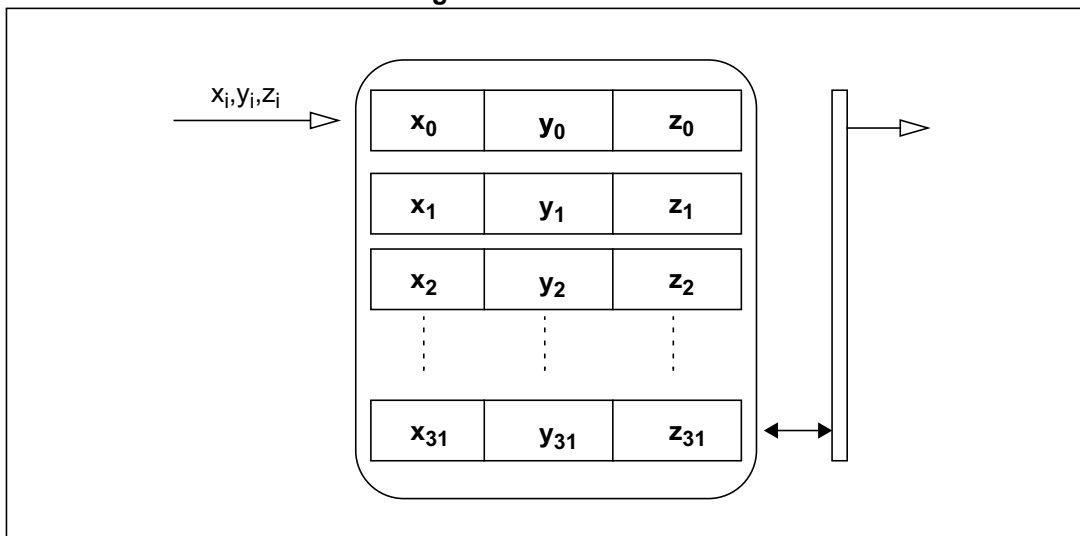
5.2 FIFO mode

In FIFO mode (*FIFO_CTRL (2Eh)* (FMODE [2:0] = 001) data from the output channels are stored in the FIFO memory until it is full, when 32 unread samples are stored in memory, data collecting is stopped.

To reset FIFO content, Bypass mode should be selected by writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '000'. After this reset command, it is possible to restart FIFO mode, writing *FIFO_CTRL (2Eh)* (FMODE [2:0]) to '001'.

A FIFO threshold interrupt can be enabled (INT1_OVR bit in *INT1_CTRL (21h)* or INT2_OVR bit in *INT2_CTRL (22h)*) in order to be raised when the FIFO is filled to the level specified by the FTH[4:0] bits of *FIFO_CTRL (2Eh)*.

Figure 10. FIFO mode



5.3 Continuous mode

Continuous mode (*FIFO_CTRL (2Eh)* (FMODE[2:0] = 110) provides a continuous FIFO update: when 32 unread samples are stored in memory, as new data arrives the oldest data is discarded and overwritten by the newer.

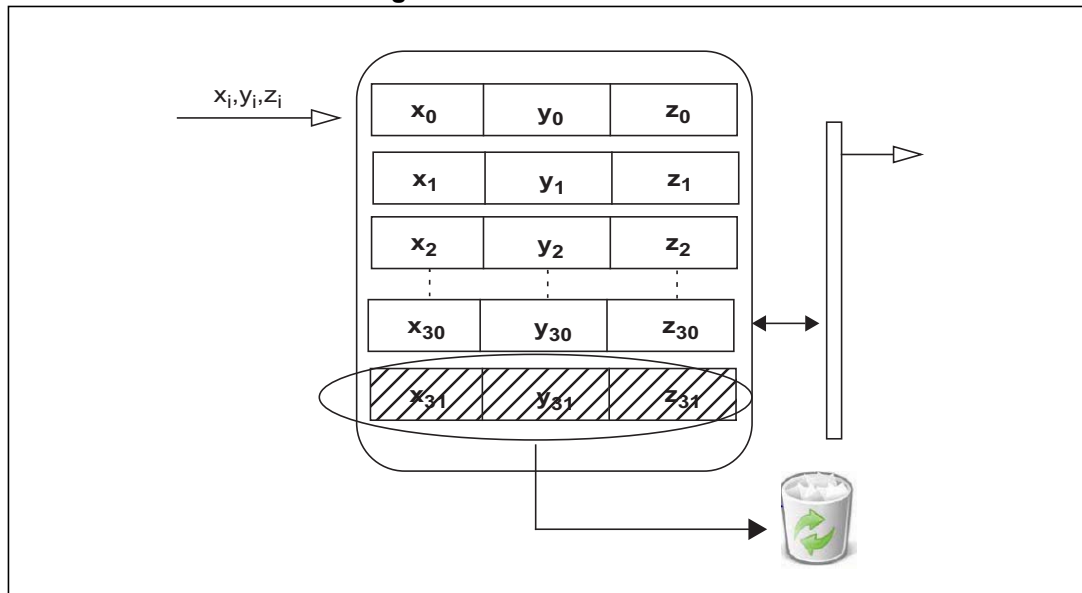
A FIFO threshold flag *FIFO_SRC (2Fh)*(FTH) is asserted when the number of unread samples in FIFO is greater than or equal to *FIFO_CTRL (2Eh)*(FTH4:0).

It is possible to route *FIFO_SRC (2Fh)*(FTH) to the INT1 pin by writing the INT1_FTH bit to '1' in register *INT1_CTRL (21h)* or to the INT2 pin by writing the INT2_FTH bit to '1' in register *INT2_CTRL (22h)*.

A full-flag interrupt can be enabled (*INT1_CTRL (21h)* (INT_FSS5)= '1' or *INT2_CTRL (22h)* (INT_FSS5)= '1') when the FIFO becomes saturated and in order to read the contents all at once. If an overrun occurs, the oldest sample in FIFO is overwritten and the OVRN flag in *FIFO_SRC (2Fh)* is asserted.

In order to empty the FIFO before it is full, it is also possible to pull from FIFO the number of unread samples available in *FIFO_SRC (2Fh)* (FSS[5:0]).

Figure 11. Continuous mode



5.4 Continuous-to-FIFO mode

In Continuous-to-FIFO mode (*FIFO_CTRL (2Eh)*(FMODE [2:0] = 011), FIFO operates in Continuous mode and FIFO mode starts on the INT1 edge trigger event. When the FIFO is full, data collecting is stopped.

Figure 12. Continuous-to-FIFO mode

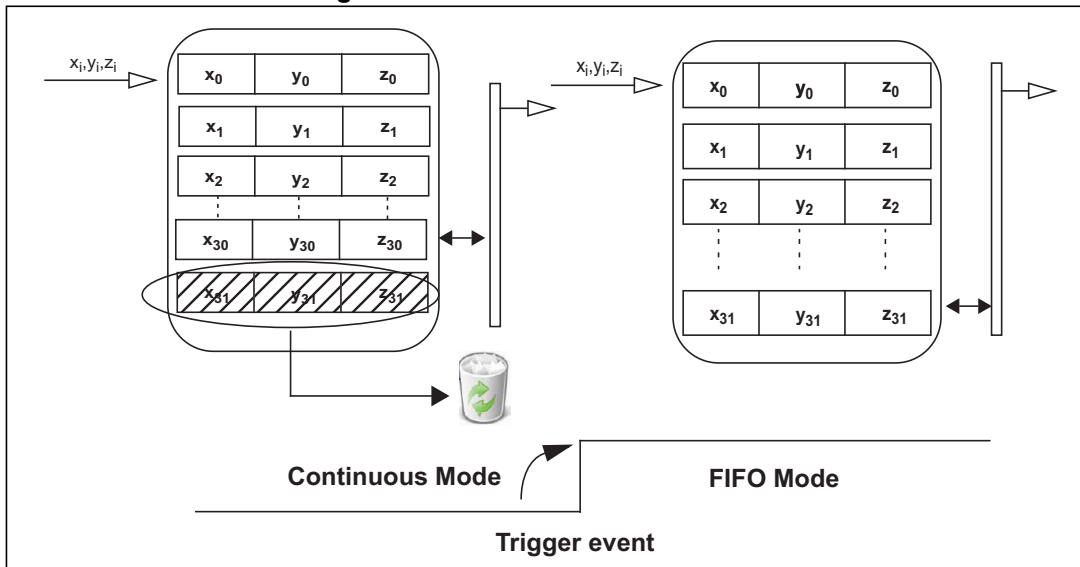
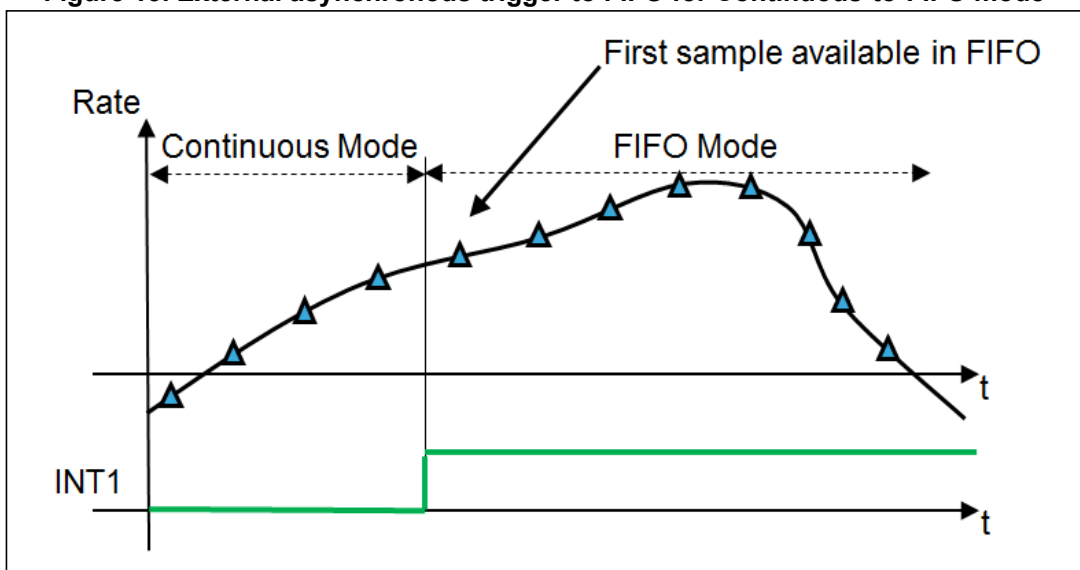


Figure 13. External asynchronous trigger to FIFO for Continuous-to-FIFO mode



5.5 Bypass-to-Continuous mode

In Bypass-to-Continuous mode (*FIFO_CTRL (2Eh)*(FMODE[2:0] = '100'), data measurement storage inside FIFO starts in Continuous mode on the INT1 edge trigger event, then the sample that follows the trigger is available in FIFO.

Figure 14. Bypass-to-Continuous mode

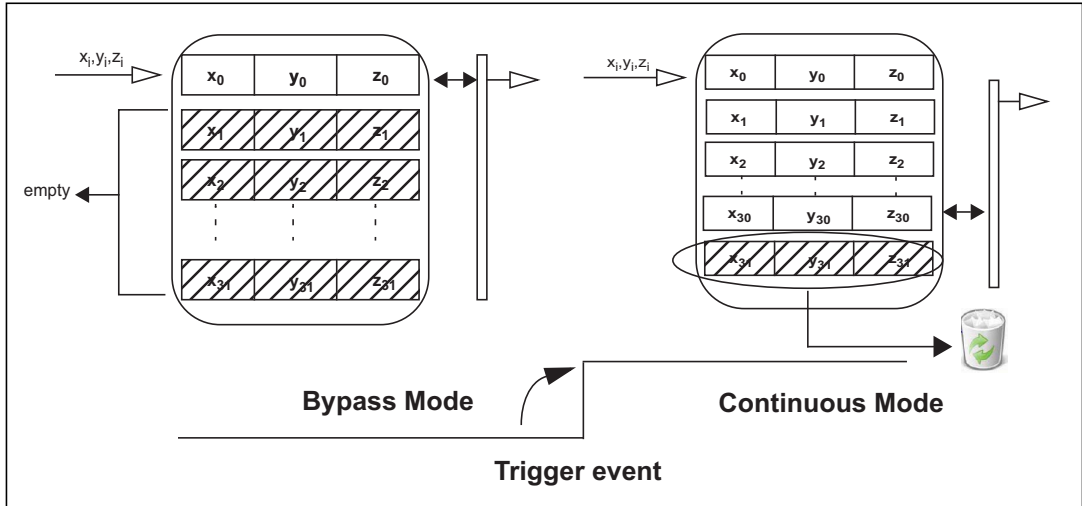
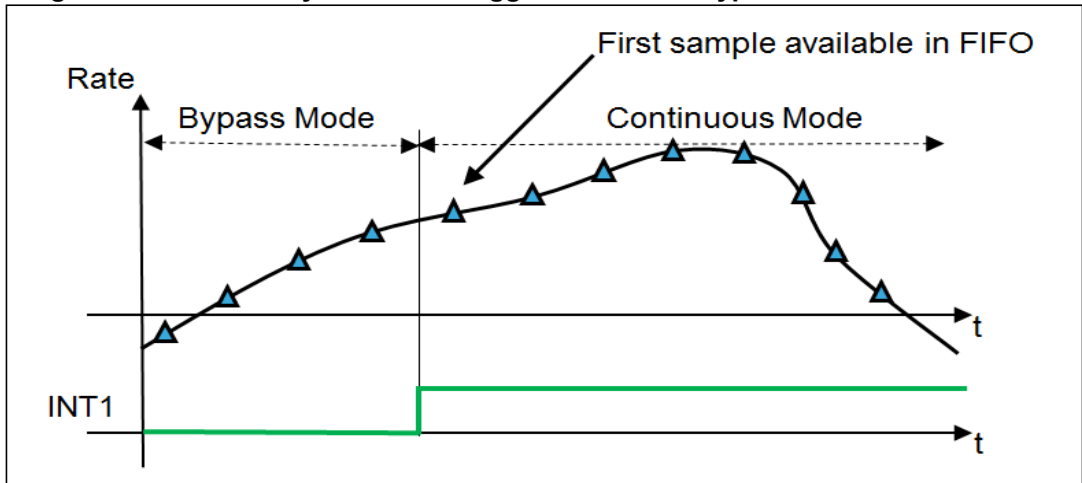


Figure 15. External asynchronous trigger to FIFO for Bypass-to-Continuous mode



6 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

Table 8. Register mapping

| Name | Type | Register address | | Default | Note |
|------------|------|------------------|----------|----------|----------|
| | | Hex | Binary | | |
| Reserved | -- | 00-0E | -- | -- | Reserved |
| WHO_AM_I | r | 0F | 00001111 | 00010001 | |
| Reserved | -- | 10-1F | -- | -- | Reserved |
| CTRL_REG1 | r/w | 20 | 00100000 | 00000000 | |
| INT1_CTRL | r/w | 21 | 00100001 | 00000000 | |
| INT2_CTRL | r/w | 22 | 00100010 | 00000000 | |
| CTRL_REG4 | r/w | 23 | 00100011 | 00000000 | |
| CTRL_REG5 | r/w | 24 | 00100100 | 00000000 | |
| OUT_TEMP_L | r | 25 | 00100101 | output | |
| OUT_TEMP_H | r | 26 | 00100110 | output | |
| STATUS | r | 27 | 00100111 | output | |
| OUT_X_L_XL | r | 28 | 00101000 | output | |
| OUT_X_H_XL | r | 29 | 00101001 | output | |
| OUT_Y_L_XL | r | 2A | 00101010 | output | |
| OUT_Y_H_XL | r | 2B | 00101011 | output | |
| OUT_Z_L_XL | r | 2C | 00101100 | output | |
| OUT_Z_H_XL | r | 2D | 00101101 | output | |
| FIFO_CTRL | r/w | 2E | 00101110 | 00000000 | |
| FIFO_SRC | r | 2F | 00101111 | output | |
| Reserved | -- | 30-32 | -- | -- | Reserved |

Registers marked as *Reserved* must not be changed. Writing to those registers may affect the correct behavior of the device.

Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration and temperature data. The register addresses, consisting of 7 bits, are used to identify them and to write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Device identification register.

Table 9. WHO_AM_I register

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
|---|---|---|---|---|---|---|---|

7.2 CTRL_REG1 (20h)

Control register 1.

Table 10. CTRL_REG1 register

| | | | | | | | |
|-----------------|----------------|------------------|------------------|------|----------|----------------|-----|
| NORM_ MOD_EN | IF_ADD_ INC | 0 ⁽¹⁾ | 0 ⁽¹⁾ | BOOT | SW_RESET | DRDY_ PULSE | BDU |
|-----------------|----------------|------------------|------------------|------|----------|----------------|-----|

1. These bits must be set to '0' for the correct operation of the device.

Table 11. CTRL_REG1 register description

| | |
|-----------------|---|
| NORM_ MOD_EN | Normal mode enable. Default value: 0 (0: power down; 1: enabled) |
| IF_ADD_ INC | Register address automatically incremented during a multiple byte access with SPI serial interface. Default value: 1 (0: disabled; 1: enabled) |
| BOOT | Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content ⁽¹⁾) |
| SW_RESET | Software reset. Default value: 0 With SW_RESET the values in the writable CTRL registers are changed to the default values. (0: normal mode; 1: reset device) This bit is cleared by hardware at the end of the operation. |
| DRDY_ PULSE | Data ready on INT1 pin. Default value: 0 (0: DRDY latched; 1: DRDY pulsed, pulse duration is 1/4 ODR) |
| BDU | Block Data Update. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB read) |

1. Boot request is executed as soon as the internal oscillator is turned on. It is possible to set the bit while in power-down mode, in this case it will be served at the next normal mode.

7.3 INT1_CTRL (21h)

INT1 pin control register.

Table 12. INT1_CTRL register

| | | | | | | | |
|-----------|-----------|----------|-----------|----------|----------|------------------|------------------|
| INT1_DRDY | INT1_BOOT | INT1_OVR | INT1_FSS5 | INT1_FTH | INT1_EXT | 0 ⁽¹⁾ | 0 ⁽¹⁾ |
|-----------|-----------|----------|-----------|----------|----------|------------------|------------------|

1. These bits must be set to '0' for the correct operation of the device.

Table 13. INT1_CTRL register description

| | |
|-----------|---|
| INT1_DRDY | Accelerometer data ready on INT1 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT1_BOOT | Boot status available on INT1 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT1_OVR | Overrun flag on INT1 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT1_FSS5 | FSS5 full FIFO flag on INT1 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT1_FTH | FIFO threshold flag on INT1 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT1_EXT | INT1 pin configuration. Default value: 0 It configures the INT1 pad as output for FIFO flags or as external asynchronous input trigger to FIFO. INT2 pad is always available as output for FIFO flags. (0: INT1 as output interrupt; 1: INT1 as input channel) |

7.4 INT2_CTRL (22h)

INT2 pin control register.

Table 14. INT2_CTRL register

| | | | | | | | |
|-----------|-----------|----------|-----------|----------|------------------|------------------|------------------|
| INT2_DRDY | INT2_BOOT | INT2_OVR | INT2_FSS5 | INT2_FTH | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ |
|-----------|-----------|----------|-----------|----------|------------------|------------------|------------------|

1. These bits must be set to '0' for the correct operation of the device.

Table 15. INT2_CTRL register description

| | |
|-----------|---|
| INT2_DRDY | Accelerometer data ready on INT2 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT2_BOOT | Boot status available on INT2 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT2_OVR | Overrun flag on INT2 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT2_FSS5 | FSS5 full FIFO flag on INT2 pin. Default value: 0 (0: disabled; 1: enabled) |
| INT2_FTH | FIFO threshold flag on INT2 pin. Default value: 0 (0: disabled; 1: enabled) |

7.5 CTRL_REG4 (23h)

Control register 4.

Table 16. CTRL_REG4 register

| | | | | | | | |
|-------------|------------|-----|-----|------------|------------|---------|------------------|
| DSP_LP_TYPE | DSP_BW_SEL | ST2 | ST1 | PP_OD_INT2 | PP_OD_INT1 | FIFO_EN | 1 ⁽¹⁾ |
|-------------|------------|-----|-----|------------|------------|---------|------------------|

1. This bit must be set to '1' for correct operation of the device.

Table 17. CTRL_REG4 register description

| | |
|-------------|---|
| DSP_LP_TYPE | Digital filtering selection. Default value: 0 (0: FIR Linear Phase; 1: IIR Nonlinear Phase) |
| DSP_BW_SEL | User-selectable bandwidth. Default value: 0 (0: 440 Hz typ.; 1: 235 Hz typ.) |
| ST [2:1] | Self-test enable. Default value: 00 (00: Self-test disabled; Other: See Table 18) |
| PP_OD_INT2 | Push-pull/open drain selection on INT2 pin. Default value: 0 (0: push-pull mode; 1: open drain mode) |
| PP_OD_INT1 | Push-pull/open drain selection on INT1 pin. Default value: 0 (0: push-pull mode; 1: open drain mode) |
| FIFO_EN | FIFO memory enable. Default value: 0 (0: disabled; 1: enabled) |

Table 18. Self-test mode selection

| ST2 | ST1 | Self-test mode |
|-----|-----|-------------------------|
| 0 | 0 | Normal mode |
| 0 | 1 | Positive sign self-test |
| 1 | 0 | Negative sign self-test |
| 1 | 1 | Not allowed |

7.6 CTRL_REG5 (24h)

Control register 5.

Table 19. CTRL_REG5 register

| | | | | | | | |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------|
| 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | 0 ⁽¹⁾ | FIFO_SPI_HS_ON |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------|

1. These bits must be set to '0' for correct operation of the device.

Table 20. CTRL_REG5 register description

| | |
|----------------|--|
| FIFO_SPI_HS_ON | Enables the SPI high speed configuration for the FIFO block that is used to guarantee a minimum duration of the window in which writing operation of RAM output is blocked. This bit is recommended for SPI clock frequencies higher than 6 MHz. Default value: 0. (0: not enabled; 1: enabled) |
|----------------|--|

7.7 OUT_TEMP_L (25h), OUT_TEMP_H (26h)

Temperature data output register. L and H registers together express a 16-bit word in two's complement left-justified.

Table 21. OUT_TEMP_L register

| | | | | | | | |
|-------|-------|-------|-------|---|---|---|---|
| Temp3 | Temp2 | Temp1 | Temp0 | 0 | 0 | 0 | 0 |
|-------|-------|-------|-------|---|---|---|---|

Table 22. OUT_TEMP_H register

| | | | | | | | |
|--------|--------|-------|-------|-------|-------|-------|-------|
| Temp11 | Temp10 | Temp9 | Temp8 | Temp7 | Temp6 | Temp5 | Temp4 |
|--------|--------|-------|-------|-------|-------|-------|-------|

Table 23. OUT_TEMP register description

| | |
|-------------|--|
| Temp [11:0] | Temperature sensor output data. The value is expressed as two's complement sign. 0 LSB represents T=25 °C ambient. |
|-------------|--|

7.8 STATUS (27h)

Status register (r)

Table 24. Status register

| | | | | | | | |
|-------|-----|-----|-----|-------|-----|-----|-----|
| ZYXOR | ZOR | YOR | XOR | ZYXDA | ZDA | YDA | XDA |
|-------|-----|-----|-----|-------|-----|-----|-----|

Table 25. Status register description

| | |
|-------|--|
| ZYXOR | Logic OR of the single X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set) |
| ZOR | Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data) |
| YOR | Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data) |
| XOR | X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data) |
| ZYXDA | Logic AND of the single X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available) |
| ZDA | Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available) |
| YDA | Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available) |
| XDA | X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available) |

7.9 OUT_X (28h - 29h)

Linear acceleration sensor X-axis output register. The value is expressed as a 16-bit word in two's complement.

7.10 OUT_Y (2Ah - 2Bh)

Linear acceleration sensor Y-axis output register. The value is expressed as a 16-bit word in two's complement.

7.11 OUT_Z (2Ch - 2Dh)

Linear acceleration sensor Z-axis output register. The value is expressed as a 16-bit word in two's complement.

7.12 FIFO_CTRL (2Eh)

FIFO control register.

Table 26. FIFO_CTRL register

| | | | | | | | |
|--------|--------|--------|------|------|------|------|------|
| FMODE2 | FMODE1 | FMODE0 | FTH4 | FTH3 | FTH2 | FTH1 | FTH0 |
|--------|--------|--------|------|------|------|------|------|

Table 27. FIFO_CTRL register description

| | |
|-------------|---|
| FMODE [2:0] | FIFO mode selection bits. Default value: 000 For further details refer to Table 28 . |
| FTH [4:0] | FIFO threshold level setting. Default value: 0 0000 |

Table 28. FIFO mode selection

| FMODE2 | FMODE1 | FMODE0 | Mode |
|--------|--------|--------|---|
| 0 | 0 | 0 | Bypass mode. FIFO turned off |
| 0 | 0 | 1 | FIFO mode. Stops collecting data when FIFO is full. |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Continuous mode until trigger is asserted, then FIFO mode. |
| 1 | 0 | 0 | Bypass mode until trigger is asserted, then Continuous mode. |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Continuous mode. If the FIFO is full, the new sample overwrites the older sample. |
| 1 | 1 | 1 | Reserved |

7.13 FIFO_SRC (2Fh)

FIFO status register.

Table 29. FIFO_SRC register

| | | | | | | | |
|-----|------|------|------|------|------|------|------|
| FTH | OVRN | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 |
|-----|------|------|------|------|------|------|------|

Table 30. FIFO_SRC register description

| | |
|-----------|---|
| FTH | FIFO threshold status. (0: FIFO filling is lower than threshold level; 1: FIFO filling is equal to or higher than the threshold level) |
| OVRN | FIFO overrun status. (0: FIFO is not completely filled; 1: FIFO is completely filled and at least one sample has been overwritten) For further details refer to Table 31 . |
| FSS [5:0] | Number of unread samples stored in FIFO. (000000: FIFO empty; 100000: FIFO full, 32 unread samples) For further details refer to Table 31 . |

Table 31. FIFO_SRC example: OVR/FSS details

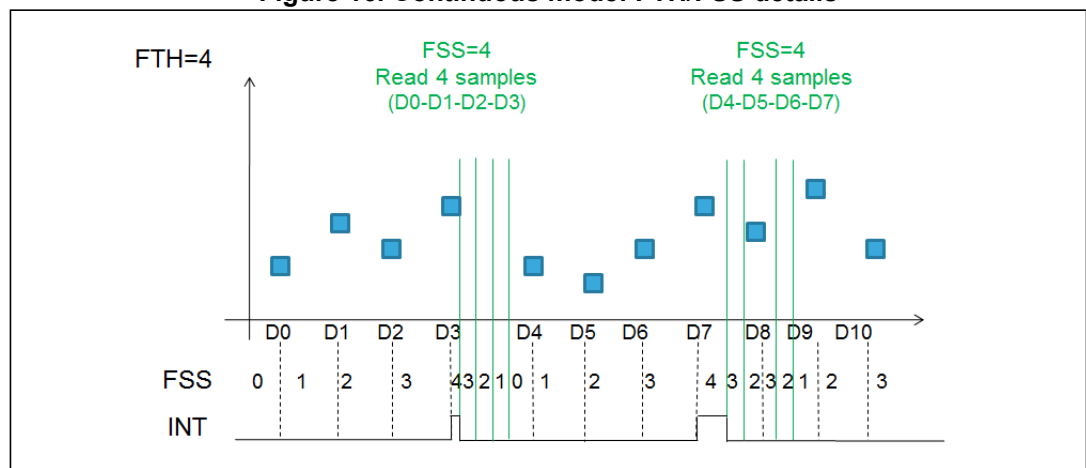
| FTH | OVRN | FSS5 | FSS4 | FSS3 | FSS2 | FSS1 | FSS0 | Description |
|-------|------|------|------|------|------|------|------|--|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO empty |
| ..(1) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 unread sample |
| ... | | | | | | | | |
| ..(1) | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 32 unread samples |
| 0(1) | 1 | 1 | 0 | 0 | 0 | 0 | 0 | At least one sample has been overwritten |

1. When the number of unread samples in FIFO is equal to or greater than the threshold level set in register *FIFO_CTRL (2Eh)*, the FTH value is '1'.

The FSS is the FIFO stored data level of the unread samples. When it is equal to FTH, all data available in FIFO are read without additional read operations.

The INT output is high when the number of samples to read is equal to or greater than FTH.

Figure 16. Continuous mode: FTH/FSS details

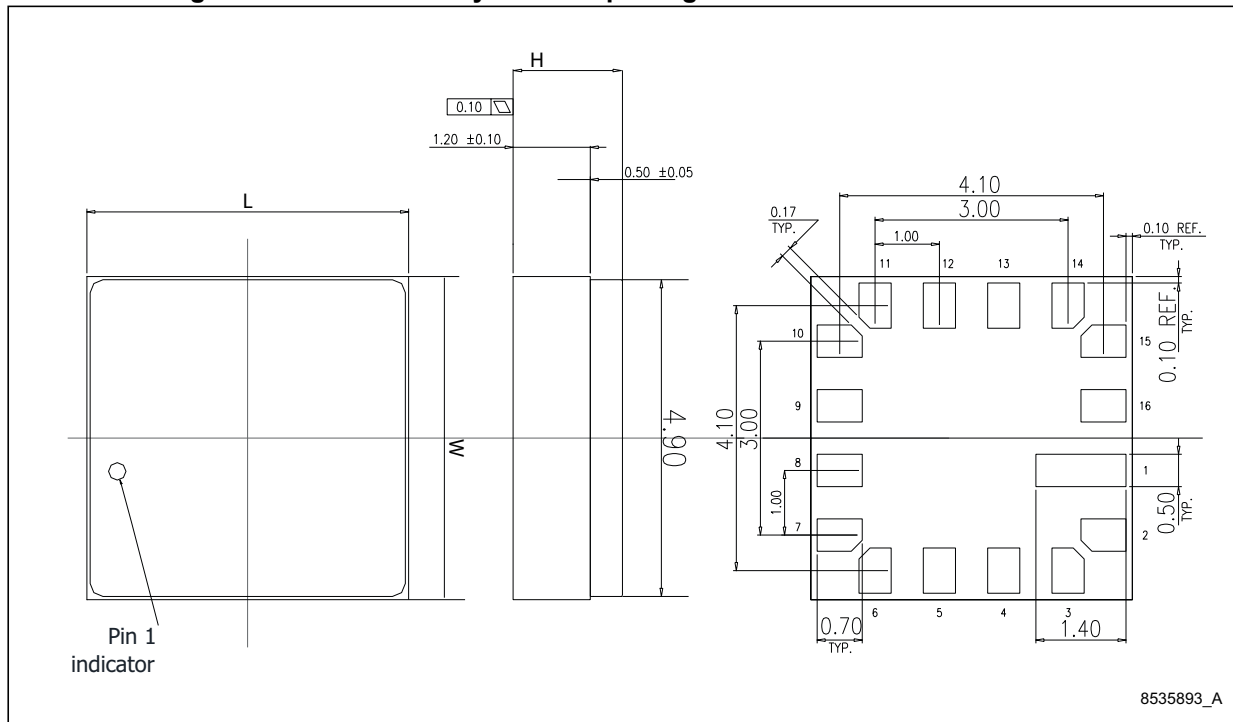


8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 LGA-16 package information

Figure 17. Ceramic cavity LGA-16: package outline and mechanical data



Note: Top and bottom view: dimensions are expressed in mm

Table 32. Outer dimensions

| ITEM | Dimension [mm] | Tolerance [mm] |
|------------|----------------|----------------|
| Length [L] | 5 | ±0.15 |
| Width [W] | 5 | ±0.15 |
| Height [H] | 1.7 typ | ±0.15 |
| Pad size | 0.7 x 0.5 | ±0.15 |

Note: General tolerance is ±0.1 mm unless otherwise specified

9 Revision history

Table 33. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 23-Mar-2017 | 1 | Initial release |
| 09-May-2017 | 2 | Updated V_{IH} , V_{IL} and added V_{OH} , V_{OL} to Table 4: Electrical characteristics |
| 11-Oct-2017 | 3 | Updated Table 3: Mechanical characteristics Updated Table 4: Electrical characteristics Updated Figure 2: Recommended power-up sequence Updated Table 7: SPI slave timing values Updated Figure 6: Multiple byte SPI read protocol (2-byte example) and Figure 8: Multiple byte SPI write protocol (2-byte example) Added WHO_AM_I (0Fh) Updated bit 0 in CTRL_REG4 (23h) |

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.