



LB1863M, ~~1869M~~

Two-Phase Unipolar Brushless Motor Driver
Automatic Recovery Type Circuit in a Miniature Flat Package

An ON Semiconductor Company

Overview

The LB1863M and ~~LB1869M~~ are 2-phase unipolar brushless motor drivers that are provided in a miniature flat package that contributes to end product miniaturization and supports automatic mounting. These products support the implementation of motor drive lock protection and automatic recovery circuits, and alarm specifications with a minimal number of external components.

Features and Functions

- Hall elements can be connected directly to the IC itself.
- 1.5-A output current output transistors built in
- Rotation detection function that provides a low-level output during motor drive and a high-level output when the motor is stopped
- Motor lock protection and automatic recovery functions built in
- Thermal shutdown circuit
- Switching noise can be reduced with an external ceramic capacitor.

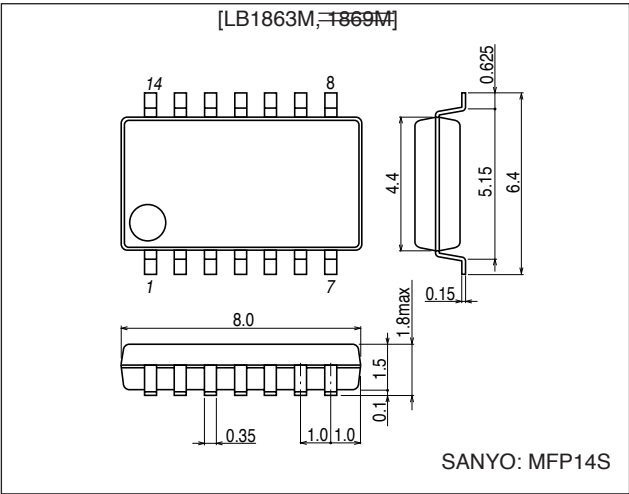
Classification

| Package | MFP-14S |
|-----------------|--------------------|
| System voltage | |
| 12 V | LB1869M |
| 24 V | LB1863M |

Note: The LB1869M and LB1863M are pin compatible so that the same printed circuit board can be used for both ~~12 V~~ and 24 V products.

Package Dimensions

unit: mm
3111-MFP14S



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Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|-----------------------------|---------------------|---|------------------------|------------------|
| Maximum input current | $I_{CC\text{ max}}$ | $t \leq 20\text{ ms}$ | 200 | mA |
| Output voltage | V_{OUT} | LB1863M | -0.3 to +85 | V |
| | | LB1869M | -0.3 to +60 | V |
| Output current | I_{OUT} | | 1.5 | A |
| RD influx current | I_{RD} | | 10 | mA |
| RD voltage | V_{RD} | | 30 | V |
| Allowable power dissipation | $P_d\text{ max}$ | When mounted (on a $20 \times 15 \times 1.5\text{-mm}^3$ glass-epoxy printed circuit board) | 800 | mW |
| Operating temperature | T_{opr} | | -30 to +80 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -55 to +150 | $^\circ\text{C}$ |

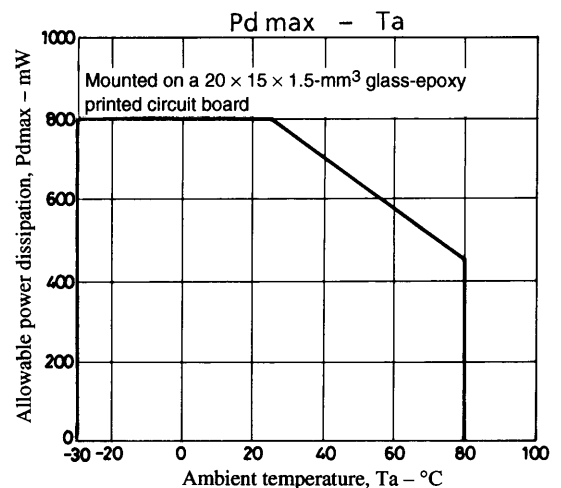
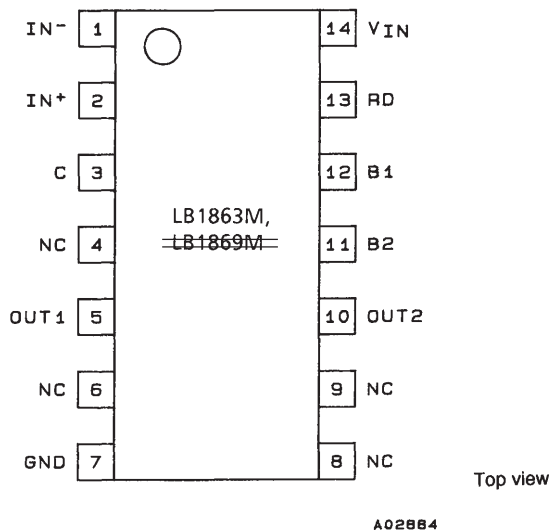
Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|---------------------------------|-----------|------------|---------------------|------|
| Input current range | I_{CC} | | 6.0 to 50 | mA |
| Common-mode input voltage range | V_{ICM} | | 0 to $V_{IN} - 1.5$ | V |

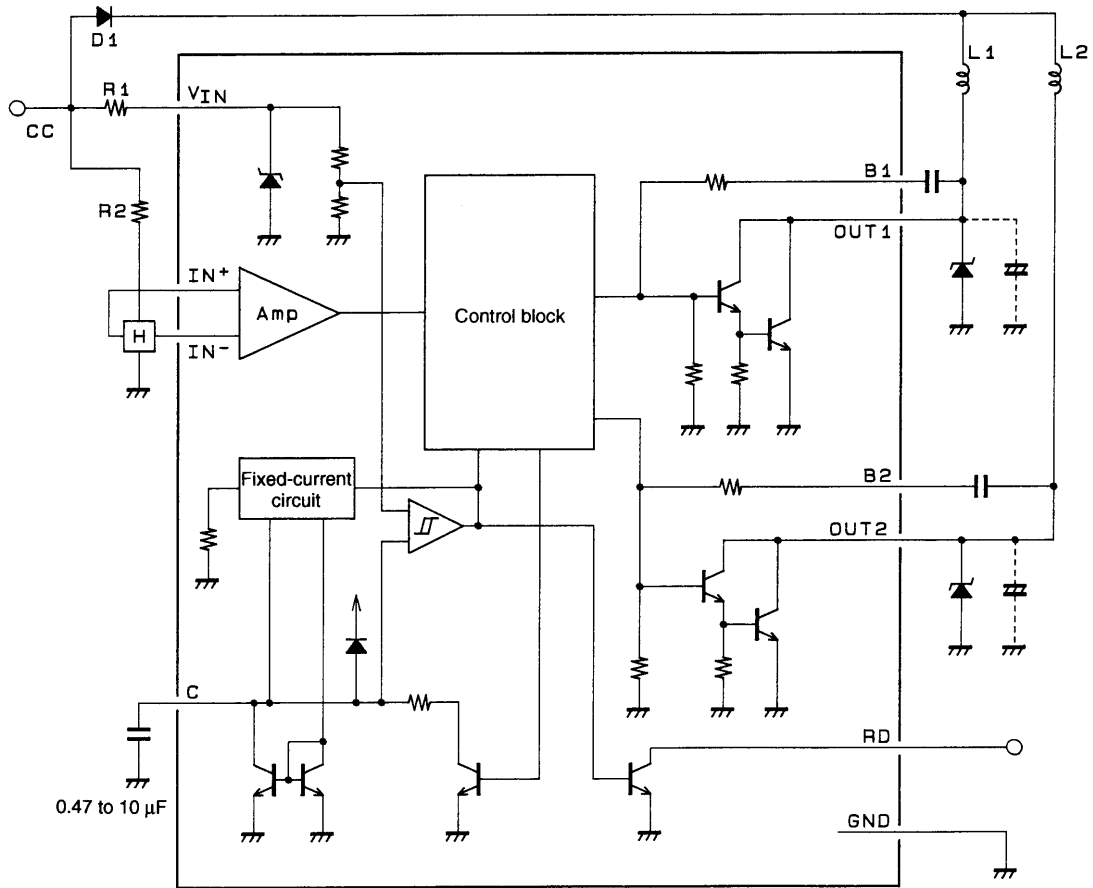
Electrical Characteristics at $T_a = 25^\circ\text{C}$, $I_{CC} = 10\text{ mA}$

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|------------------------------------|---------------|--|---------------|--------------|------|---------------|
| | | | min | typ | max | |
| Output voltage 1 | V_{OR} | LB1863M | 80 | | | V |
| | | LB1869M | 60 | | | V |
| Output voltage 2 | $V_{O(SUS)}$ | LB1863M : $I_O = 0.1\text{ A}$ | 65 | | | V |
| | | LB1869M : $I_O = 0.1\text{ A}$ | 40 | | | V |
| Output saturation voltage | $V_{O(sat)1}$ | $I_O = 0.5\text{ A}$ | | 0.95 | 1.2 | V |
| | $V_{O(sat)2}$ | $I_O = 1.0\text{ A}$ | | 1.15 | 1.5 | V |
| Input voltage | V_{IN} | $I_{CC} = 7.0\text{ mA}$ | 6.4 | 6.7 | 7.0 | V |
| Amplifier input offset voltage | V_{OFF} | | -7 | 0 | +7.0 | mV |
| Amplifier input bias current | I_{BA} | | -250 | | | nA |
| RD output saturation voltage | $V_{RD(sat)}$ | $I_{RD} = 5\text{ mA}$ | | 0.1 | 0.3 | V |
| Capacitor discharge current | I_{C1} | | 2.1 | 3 | 3.9 | μA |
| | I_{C2} | | 0.31 | 0.44 | 0.59 | μA |
| Comparator input threshold voltage | V_{TH1} | | 0.77 | $0.8V_{IN}$ | 0.83 | V |
| | V_{TH2} | | 0.42 | $0.45V_{IN}$ | 0.48 | V |

Pin Assignment

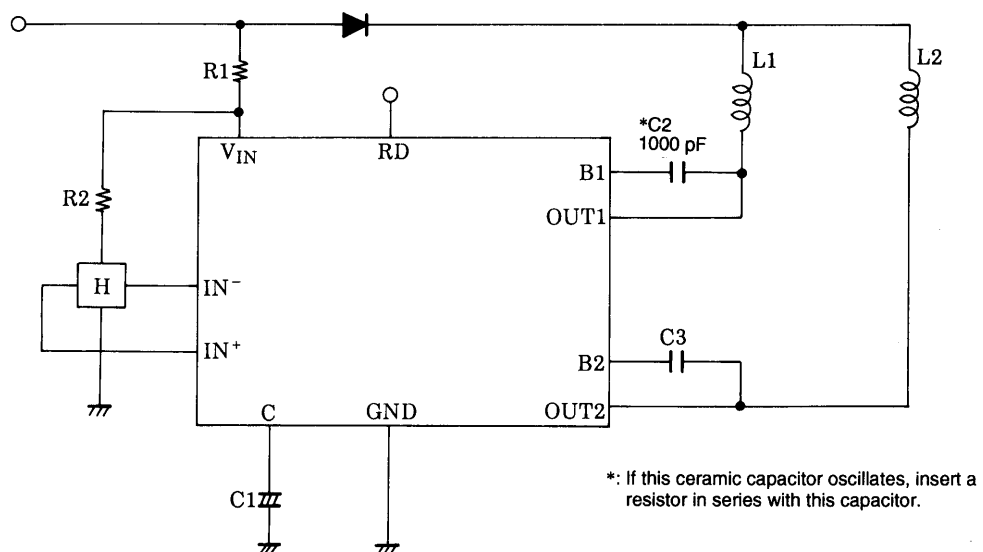


Equivalent Circuit, Block Diagram, and Sample Application

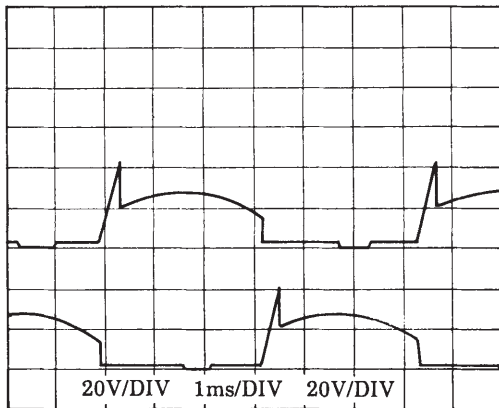


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Sample Application Circuit



Sample Application Circuit Output Waveforms



Truth Table

| IN ⁺ | IN ⁻ | C | OUT1 | OUT2 | RD |
|-----------------|-----------------|---|------|------|----|
| H | L | L | H | L | L |
| L | H | L | L | H | L |
| H | L | H | H | H | H |
| L | H | H | H | H | H |

Design Documentation (See the application circuit diagram.)

1. Power-supply voltage (V_{IN} pin)

Since these miniature flat package products supply power to the Hall amplifier block and the control block from an internal parallel regulator, they operate with good stability with respect to kickback currents from the motor and variations in the power-supply voltage. They also provide an adequate ability to withstand surges. The resistor R1 between the V_{CC} and V_{IN} pins should be set up so that a current in the range I_{CC} = 6 to 50 mA flows into the V_{IN} pin in the fan motor power-supply voltage range.

V_{IN} has a typical value of 6.7 volts when I_{CC} is 7 mA. The current flowing into V_{IN} can be calculated with the following formula.

$$I_{CC} = \frac{V_{CC} - V_{IN}}{R1} \dots\dots\dots(1)$$

• Abnormal voltage considerations

The maximum allowable current for the V_{IN} pin is 200 mA. Therefore, the IC design allows it to withstand voltages up to the plus side abnormal voltage V_{surge} give by formula (2).

$$V_{surge} = V_{IN} + R1 \times 200 \text{ mA} \dots\dots(2)$$

2. Hall input pin voltages (IN⁻ and IN⁺ pins)

The Hall element output voltages to the Hall element input pins must be in the range 0 to (V_{IN} - 1.5 V). The gain from the Hall input pins to the output pin is over 100 dB. The Hall input amplifier offset voltage is ±7 mV. This means that the Hall element output must be set up taking this ±7 mV offset into account.

3. Output transistors (OUT1 and OUT2 pins)

Output current: I_O = 1.5 A maximum

Output saturation voltage: V_{Osat} = 1.15V/1.0 A (typical)

Applications should adopt one of the following three output protection techniques.

- ① If a capacitor is inserted between OUT and ground, use a capacitor with a value up to C = 10 μF, and design that value so that the kickback and reverse voltages do not exceed V_{OR}.
- ② If a Zener diode is added, determine a value for the Zener voltage that is lower than V_{O(SUS)}. If radio-frequency noise is a problem, insert a capacitor between B1 and B2.
- ③ If a capacitor is inserted between OUT and B1, set the capacitor value so that the kickback voltage is lower than V_{O(SUS)}. If oscillation occurs, insert a resistor in series with the capacitor.

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