

## Evaluation Board for Dual, High Speed Op Amps Offered in 8-Lead SOIC Packages

### FEATURES

**Enables quick breadboarding/prototyping**  
**User-defined circuit configuration**  
**Edge-mounted SMA connector provisions**  
**Easy connection to test equipment and other circuits**  
**RoHS compliant**

### GENERAL DESCRIPTION

The Analog Devices, Inc., 8-lead SOIC package, dual, high speed evaluation board is designed to help customers quickly prototype new dual op amp circuits and reduce design time. The evaluation board can be used with almost any Analog Devices dual op amp in various configurations and applications. The evaluation board is a bare board (that is, there are no components or amplifier soldered to the board; these must be ordered separately). Figure 1 shows the component side of the evaluation board, and Figure 2 shows the circuit side of the evaluation board.

This evaluation board is a 6-layer PCB, designed to provide internal, wideband, power supply bypassing without the use of

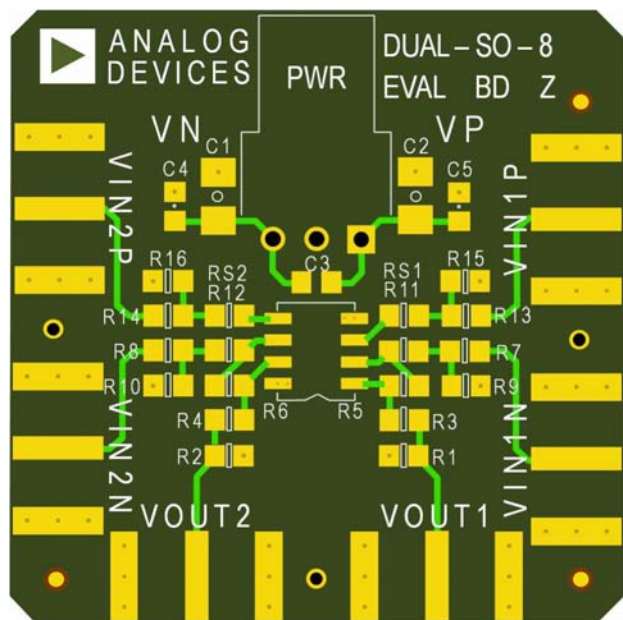
external capacitors. The close spacing between the VCC supply plane (Layer 3) and the inner ground plane (Layer 4) provides the necessary capacitance to bypass the VCC supply. Similarly, the close spacing between the inner ground layer (Layer 4) and the VEE supply plane (Layer 5) provides the necessary capacitance to bypass the VEE supply.

The evaluation board components are primarily SMT 0603 case size, with the exception of the electrolytic bypass capacitors (C1, C2), which are 1206 case size.

Two options are available for supply bypassing. The first option is to use the internal interplanar capacitance. No external bypass capacitors are required. Capacitors C1 to C5 can be left off the board. If additional supply bypassing is required, C1 and C2 can accommodate 1206 tantalum or nonpolarized capacitors. C3, C4, and C5 accommodate 0603 capacitors.

Figure 3 shows the evaluation board schematic. Figure 4 and Figure 5 show the evaluation board assembly drawings.

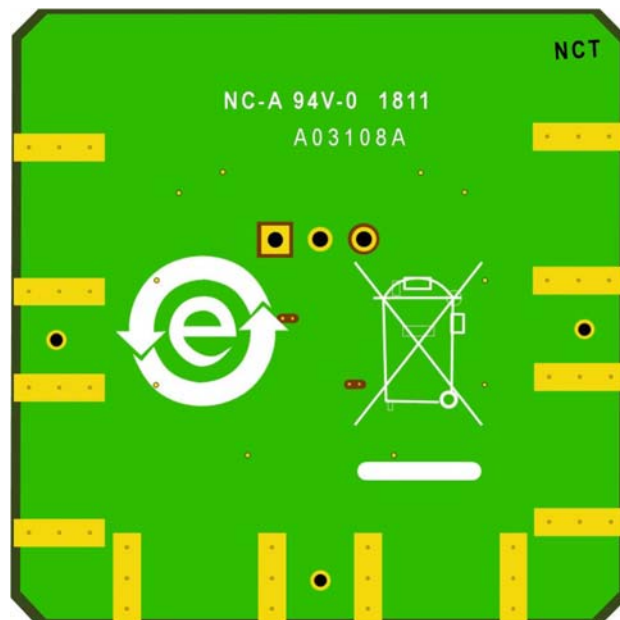
### EVALUATION BOARD COMPONENT AND CIRCUIT SIDES



#### NOTES

1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 1. Component Side of Evaluation Board



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Figure 2. Circuit Side of Evaluation Board

## TABLE OF CONTENTS

|                                                    |   |                                                       |   |
|----------------------------------------------------|---|-------------------------------------------------------|---|
| Features .....                                     | 1 | Evaluation Board Schematic and Assembly Drawings..... | 3 |
| General Description .....                          | 1 | Evaluation Board Layer Stackup.....                   | 4 |
| Evaluation Board Component and Circuit Sides ..... | 1 | Ordering Information.....                             | 5 |
| Revision History .....                             | 2 | Bill of Materials.....                                | 5 |

## REVISION HISTORY

### 8/11—Rev. A to Rev. B

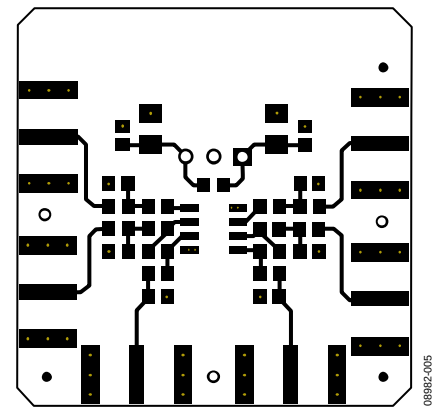
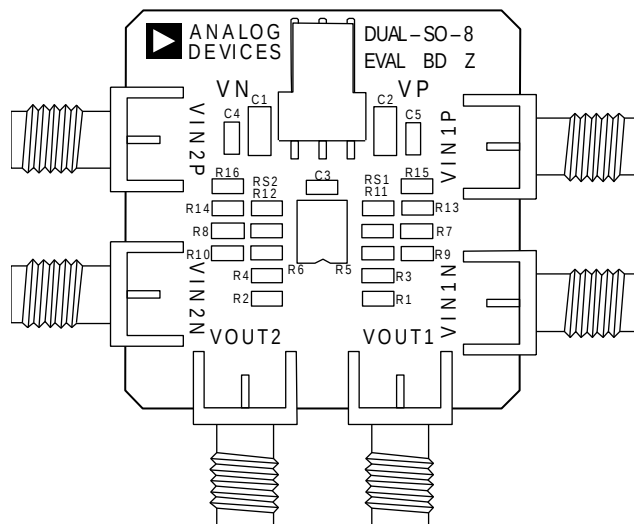
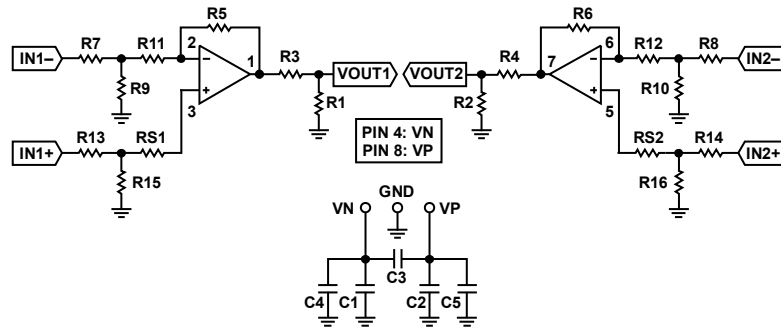
|                                                                                                             |   |
|-------------------------------------------------------------------------------------------------------------|---|
| Changes to General Description Section, Figure 1, and Figure 2 .....                                        | 1 |
| Changed Evaluation Board Schematic Section to Evaluation Board Schematic and Assembly Drawings Section..... | 3 |
| Changes to Figure 3, Figure 4, and Figure 5.....                                                            | 3 |
| Deleted Figure 6 and Figure 7; Renumbered Sequentially.....                                                 | 4 |
| Added Evaluation Board Layer Stackup Section .....                                                          | 4 |
| Added Figure 6; Renumbered Sequentially .....                                                               | 4 |
| Changes to Table 1 .....                                                                                    | 5 |

### 4/11—Rev. 0 to Rev. A

|                                                                                                    |   |
|----------------------------------------------------------------------------------------------------|---|
| Changes to Product Title, General Description Section, Figure 1 and Figure 2 .....                 | 1 |
| Changed Evaluation Board Schematic and Artwork Section to Evaluation Board Schematic Section ..... | 3 |
| Added Evaluation Board Assembly Drawings and Layout Patterns Section .....                         | 4 |
| Changes to Figure 4 through Figure 7 .....                                                         | 4 |

### 4/10—Revision 0: Initial Version

## EVALUATION BOARD SCHEMATIC AND ASSEMBLY DRAWINGS



EVALUATION BOARD LAYER STACKUP

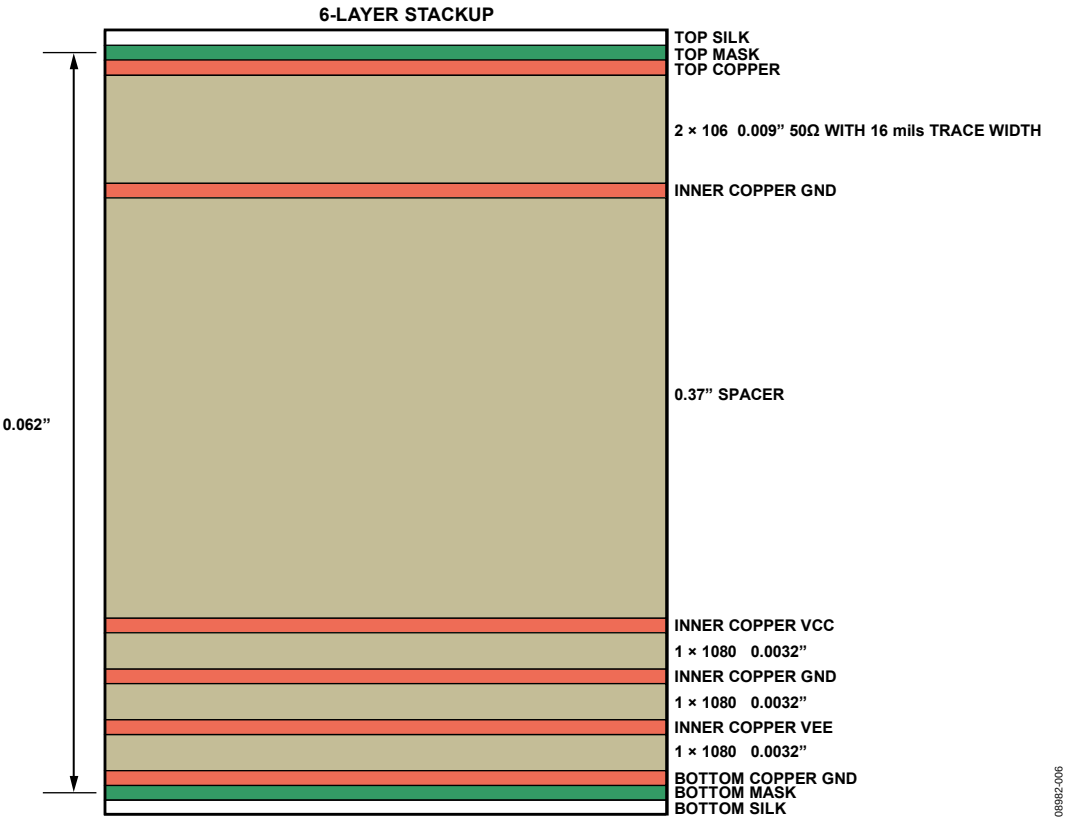


Figure 6. Evaluation Board Stackup

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 1.

| Quantity | Reference Designator                     | Description            | Package          |
|----------|------------------------------------------|------------------------|------------------|
| 1        | PWR                                      | Power connector        | 0.1 inch spacing |
| 2        | C1, C2                                   | 10 $\mu$ F capacitor   | C1206            |
| 3        | C3, C4, C5                               | User-defined capacitor | C0603            |
| 1        | DUT                                      | Device                 | 8-lead SOIC      |
| 6        | VIN1P, VIN2P, VIN1N, VIN2N, VOUT1, VOUT2 | SMA/SMT                | SMA/SMT          |
| 18       | R1 to R16, RS1, RS2                      | User-defined resistor  | R0603            |

**NOTES**

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**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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