Dual Programmable Filters and VGAs for 2 GHz Channel Spacing for µW Radios

Data Sheet **ADRF6520**

FEATURES

- Matched VGAs and programmable filters
- Maximum gain: 53 dB
- Continuous gain control range: 60 dB
- Filter bypass mode I/Q bandwidth
  - ±1 dB gain flatness: >1250 MHz
- 4-pole Butterworth filter I/Q bandwidth: 36 MHz to 720 MHz
- RMS detector
- IMD3: <−55 dBc for 1.5 V p-p composite output
- HD2, HD3: <−55 dBc for 1.5 V p-p output
- Noise figure: 10.5 dB at maximum gain
  - NF < 11 dB over 12 dB of VGA2 gain backoff
- 100 Ω differential input, low impedance output
- Optional dc output offset correction
- SPI-programmable filter corners
- Single 3.3 V supply operation with power-down feature

APPLICATIONS

- Point-to-point and point-to-multipoint radios
- Baseband IQ receivers
- Diversity receivers
- ADC drivers
- Instrumentation
- Medical

FUNCTIONAL BLOCK DIAGRAM

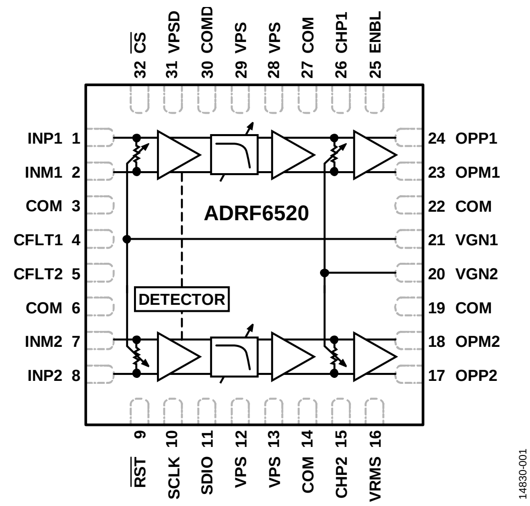

Figure 1

GENERAL DESCRIPTION

The ADRF6520 is a matched pair of fully differential low noise and low distortion programmable filters and variable gain amplifiers (VGAs). Each channel is capable of rejecting large, out of band interferers while reliably boosting the wanted signal, thus reducing the bandwidth and resolution requirements on the analog-to-digital converters (ADCs). The excellent matching between channels and their high spurious-free dynamic range over all gain and bandwidth settings make the ADRF6520 ideal for quadrature-based (IQ) communication systems with dense constellations, multiple carriers, and nearby interferers. The filter corners, enable, and dc offset correction loop enable are all programmable via a serial peripheral interface (SPI).

The first VGA that precedes the filters offers 30 dB of continuous gain control with a maximum gain of 18 dB and sets a differential input impedance of 100 Ω. The filters provide a four-pole Butterworth response with −1 dB corner frequencies: 36 MHz, 72 MHz, 144 MHz, 288 MHz, 432 MHz, 576 MHz, and 720 MHz. For operation beyond 720 MHz, the filter can be disabled and completely bypassed, thereby extending the −1 dB bandwidth up to 1.25 GHz. A wideband rms detector is available to monitor the signal at the filter inputs. A fixed gain amplifier of 6 dB immediately follows the filter. The postfilter VGA provides 30 dB of continuous gain control with a maximum gain of 12 dB. The output buffers offer an additional 18 dB of gain and provide a differential output impedance of 20 Ω. The output buffers are capable of driving 1.5 V p-p into 100 Ω loads at better than 55 dBc nominal for the third-order intermodulation distortion (IMD3). Independent, built in, dc offset correction loops for each channel can be disabled via the SPI if fully dc-coupled operation is desired. The high-pass corner frequency is determined by external capacitors on the CHP1 and CHP2 pins and the postfilter VGA gain.

The ADRF6520 operates from a 3.15 V to 3.45 V supply and consumes a maximum supply current of 425 mA. When fully disabled, it consumes ≤10 mA. The ADRF6520 is fabricated in an advanced silicon-germanium BiCMOS process and is available in a 32-lead, exposed pad LFCSP. Performance is specified over the −40°C to +85°C temperature range.

Rev. 0 Document Feedback

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REVISION HISTORY

4/2017—Revision 0: Initial Version

SPECIFICATIONS

VPS, VPSD = 3.3 V, T_A = 25°C, Z_{LOAD} = 100 Ω.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RESPONSE, FILTER BYPASS MODE					
±1 dB Gain Flatness Bandwidth	I or Q channel		1.25		GHz
FREQUENCY RESPONSE					
Low-Pass Corner Frequency, f_C					
Corner Frequencies	Four-pole Butterworth filter, −1 dB bandwidth		36		MHz
			72		MHz
			144		MHz
			288		MHz
			432		MHz
			576		MHz
			720		MHz
Corner Frequency Absolute Accuracy	Over operating temperature range		±8		% f_C
Corner Frequency Matching	Channel A and Channel B at same gain and bandwidth settings		±0.5		% f_C
Pass-Band Flatness	Defined as difference between value at 100 kHz and f_C				
Corner Frequency = 72 MHz			0.2		dB
Bypass Mode			1.5		dB
Gain Matching	Channel A and Channel B at same gain and bandwidth settings; 1 kHz to f_C		±0.1		dB
Group Delay Variation	From midband to peak				
Corner Frequency = 36 MHz			4		ns
Corner Frequency = 144 MHz			0.8		ns
Corner Frequency = 720 MHz			0.25		ns
Bypass Mode			0.15		ns
Group Delay Matching	At f_C/2; Channel A and Channel B at same gain				
Corner Frequency = 36 MHz			±60		ps
Corner Frequency = 144 MHz			±50		ps
Corner Frequency = 720 MHz			±15		ps
Bypass Mode			±10		ps
Stop-Band Rejection	Gain = 53 dB				
Relative to Pass Band	2 × f_C		−20		dB
	5 × f_C		−50		dB
	10 × f_C		−80		dB
INPUT STAGE	INP1, INM1, INP2, INM2				
Maximum Input Swing	At minimum gain, VGN1 = 0 V		4.0		V p-p
Differential Input Impedance			100		Ω
Input Common Mode	AC coupling recommended		1.375		V
RMS DETECTOR	VRMS, CFLT1, CFLT2				
Output Scaling	Relative to the summation of the differential voltage at filter input of both channels		1		V/V rms
Output Current	Source available			3	mA
Output Load	To reach full scale	1			kΩ
GAIN CONTROL	VGN1, VGN2				
Gain Range	Maximum gain		53		dB
	Minimum gain		−7		
Attenuation Range	Each attenuator; VGN1 or VGN2 = 1.5 V	−30	0		dB
	Each attenuator; VGN1 or VGN2 = 0 V		30		dB
Gain Slope			30		mV/dB
Gain Error	V_{GAIN} from 500 mV to 1000 mV		0.2		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT STAGE	OPP1, OPM1, OPP2, OPM2				
Maximum Output Swing	At maximum gain, R_{LOAD} = 100 Ω	3.5	4.5		V p-p
	HD2 > 55 dBc, HD3 > 55 dBc, R_{LOAD} = 100 Ω		1.5		V p-p
Output 1 dB Compression Point (OP1dB)	Gain = 53 dB	12	14		dBm re:100 Ω
Differential Output Impedance			<20		Ω
Output DC Offset	Inputs shorted, dc offset correction loop enabled		<20		mV
Output Common-Mode	AC coupling recommended		1.65		V
NOISE/DISTORTION					
Corner Frequency = 36 MHz					
Output Noise Density	At f_C/2, VGA1 gain = 18 dB, VGA2 gain = 0 dB		−137.25		dBV/Hz
	At f_C/2, VGA1 gain = 18 dB, VGA2 gain = 30 dB		−119.5		dBV/Hz
Noise Figure	Gain = 53 dB		11		dB
Second Harmonic, HD2	10 MHz fundamental, 1.5 V p-p output level				
	VGA1 gain = 6 dB, VGA2 = 0 dB		−71.7		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−71.7		dBc
	VGA1 gain = 18 dB, VGA2 = 24 dB		−72.9		dBc
Third Harmonic, HD3	10 MHz fundamental, 1.5 V p-p output level				
	VGA1 gain = 6 dB, VGA2 = 0 dB		−74.3		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−74.7		dBc
	VGA1 gain = 18 dB, VGA2 = 24 dB		−81.2		dBc
IMD3	18 MHz and 19 MHz tones, 1.5 V p-p composite output				
	Gain = 0 dB		−70		dBc
	Gain = 24 dB		−71.2		dBc
	Gain = 48 dB		−85		dBc
Corner Frequency = 720 MHz					
Output Noise Density	At f_C/2, VGA1 gain = 18 dB, VGA2 gain = 0 dB		−137		dBV/Hz
	At f_C/2, VGA1 gain = 18 dB, VGA2 gain = 30 dB		−119.9		dBV/Hz
Noise Figure	Gain = 53 dB		11		dB
Second Harmonic, HD2	100 MHz fundamental, 1.5 V p-p output level				
	VGA1 gain = 6 dB, VGA2 = 0 dB		−72		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−75.6		dBc
	VGA1 gain = 18 dB, VGA2 = 24 dB		−80.6		dBc
Third Harmonic, HD3	100 MHz fundamental, 1.5 V p-p output level				
	VGA1 gain = 6 dB, VGA2 = 0 dB		−71.3		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−71.6		dBc
	VGA1 gain = 18 dB, VGA2 = 24 dB		−79.8		dBc
IMD3	356.5 MHz and 363.5 MHz tones, 1.5 V p-p composite output				
	VGA1 gain = −6 dB, VGA2 = 0 dB		−65		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−66.5		dBc
	VGA1 gain = 18 dB, VGA2 = 24 dB		−81.1		dBc
Bypass Mode					
Output Noise Density	At 500 MHz, VGA1 gain = 18 dB, VGA2 gain = 0 dB		−136.8		dBV/Hz
	At 500 MHz, VGA1 gain = 18 dB, VGA2 gain = 30 dB		−119.8		dBV/Hz
Noise Figure	Gain = 53 dB		10.5		dB
Second Harmonic, HD2	330 MHz fundamental, 1.5 V p-p output level				
	VGA1 gain = −6 dB, VGA2 = 0 dB		−64.5		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−65		
	VGA1 gain = 18 dB, VGA2 = 24 dB		−78.4		dBc

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Third Harmonic, HD3	330 MHz fundamental, 1.5 V p-p output level				
	VGA1 gain = −6 dB, VGA2 = 0 dB		−60.5		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−62.5		
	VGA1 gain = 18 dB, VGA2 = 24 dB		−70.4		dBc
IMD3	496.5 MHz and 503.5 MHz tones, 1.5 V p-p composite output				
	VGA1 gain = −6 dB, VGA2 = 0 dB		−68.8		dBc
	VGA1 gain = 18 dB, VGA2 = 0 dB		−70		dBc
	VGA1 gain = 18 dB, VGA2 = 24 dB		−77		dBc
DIGITAL LOGIC	LE, CLK, DATA, SDO				
Input High Voltage, V_{HIGH}			>2		V
Input Low Voltage, V_{LOW}			<0.8		V
Input Current, I_{HIGH}/I_{LOW}			<1		µA
Input Capacitance, C_{IN}			2		pF
SPI TIMING	LE, CLK, DATA, SDO				
f_{CLK}	$1/t_{CLK}$		20		MHz
t_{DH}	DATA hold time		5		ns
t_{DS}	DATA setup time		5		ns
t_{LH}	LE hold time		5		ns
t_{LS}	LE setup time		5		ns
t_{PW}	CLK high pulse width		5		ns
t_{D}	CLK to SDO delay		5		ns
POWER AND ENABLE	VPS, VPSD, COM, COMD, ENBL				
Supply Voltage Range		3.15	3.3	3.45	V
Total Supply Current	ENBL = 3.3 V				
	Maximum bandwidth setting		425		mA
	Filter bypassed		390		mA
Disable Current	ENBL = 0 V		10		mA
Disable Threshold			1.6		V
Enable Response Time	Delay following ENBL low to high transition		20		µs
Disable Response Time	Delay following ENBL high to low transition		300		ns

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltages, VPS, VPSD	3.6 V
ENBL, LE, CLK, DATA, SDIO	VPSD + 0.5 V
INP1, INM1, INP2, INM2,	VPS + 0.5 V
OPP1, OPM1, OPP2, OPM2	VPS + 0.5 V
OFS1, OFS2, VRMS	VPS + 0.5 V
VGN1, VGN2	VPS + 0.5 V
Internal Power Dissipation	1.53 W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

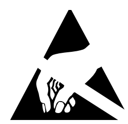
Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-32-12	29.4	2.0	°C/W

[1] Based on simulation with JEDEC standard JESD51, using a 2S2P board.
[2] Based on simulation with JEDEC standard JESD51, using a 1S0P board.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

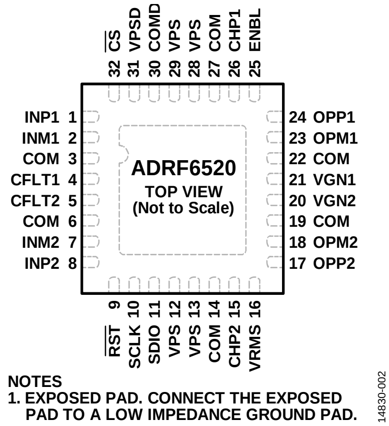


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	INP1, INM1	Channel 1 Differential Inputs, 100 Ω Differential Input Impedance.
3, 6, 19, 22	COM	Analog Common. Connect COM to an external circuit common using the lowest possible impedance.
4, 5	CFLT1, CFLT2	Averaging Capacitors for RMS Detectors. The user can leave these pins open for the fastest response time and the least amount of rms averaging.
7, 8	INM2, INP2	Channel 2 Differential Inputs, 100 Ω Differential Input Impedance.
9	$\overline{\text{RST}}$	SPI Reset to Default Bit Values. This pin is active low. Pull the pin high under nonactive conditions. The transistor-transistor logic (TTL) levels are V_{LOW} < 0.8 V and V_{HIGH} > 2 V.
10	SCLK	SPI Port Clock. The TTL levels are V_{LOW} < 0.8 V and V_{HIGH} > 2 V.
11	SDIO	SPI Data Input and Output. The TTL levels are V_{LOW} < 0.8 V and V_{HIGH} > 2 V.
12, 13, 28, 29	VPS	Analog Positive Supply Voltage: 3.15 V to 3.45 V.
15, 26	CHP2, CHP1	DC Offset Correction Loop Capacitors. Connect the capacitors to a circuit common.
16	VRMS	RMS Detector Output. The output transfer function is 1 V/V rms × (CH1_RMS + CH2_RMS), where CH1_RMS is the differential rms voltage of the input of the Channel 1 filter, and CH2_RMS is the differential rms voltage of the input of the Channel 2 filter. The user can leave the pin open if not using the rms detector; there is no need to terminate this pin. Load this pin with at least 1 kΩ to ground; values lower than this prevent the detector output from reaching its full-scale value.
17, 18	OPP2, OPM2	Channel 2 Differential Outputs. These outputs have a 20 Ω differential output impedance.
20, 21	VGN2, VGN1	VGA2 and VGA1 Analog Gain Control. These pins operate from 0 V to 1.5 V with 30 mV/dB gain scaling.
23, 24	OPM1, OPP1	Channel 2 Differential Outputs. These outputs have a 20 Ω differential output impedance.
25	ENBL	Chip Enable. Pull this pin high to enable the chip. Voltages on ENBL of less than 1.6 V disable the device.
30	COMD	Digital Common. Connect this pin to an external circuit common using the lowest possible impedance.
31	VPSD	Digital Positive Supply Voltage: 3.15 V to 3.45 V.
32	$\overline{\text{CS}}$	Chip Select Bar to Enable SPI Programming. $\overline{\text{CS}}$ is an SPI programming pin and is active low. The TTL levels are V_{LOW} < 0.8 V and V_{HIGH} > 2 V.
	EP	Exposed Ground Pad. Connect the exposed pad to a low impedance ground pad.

TYPICAL PERFORMANCE CHARACTERISTICS

VPS, VPSD = 3.3 V, T_A = 25°C, Z_{LOAD} = 100 Ω, dc offset correction loop disable bit (B5) = 1 (enabled), noise spectral density (NSD) measured at $f_C/2$ and at 500 MHz in bypass mode, unless otherwise noted. Noise figure measured with 100 Ω differential input termination. Worst case IMD3 tone is reported for all IMD3/IP3 plots.

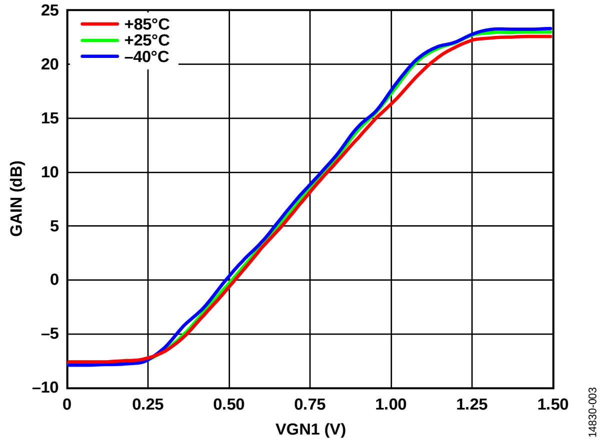


Figure 3. Gain at 500 MHz vs. VGN1 over Temperature; Bypass Mode, VGN2 = 0 V

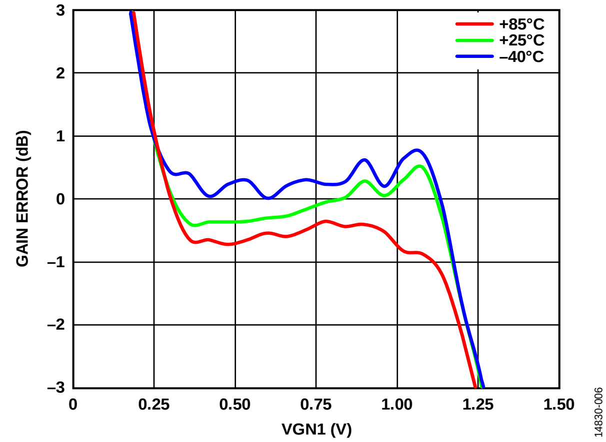


Figure 6. Gain Error at 500 MHz vs. VGN1 over Temperature; Bypass Mode, VGN2 = 0 V

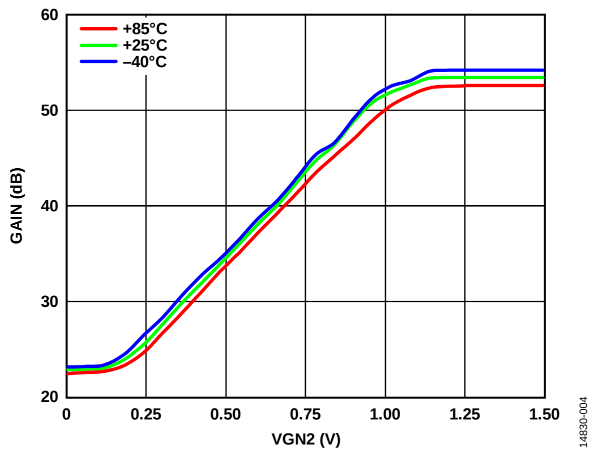


Figure 4. Gain at 500 MHz vs. VGN2 over Supply; Bypass Mode, VGN1 = 1.5 V

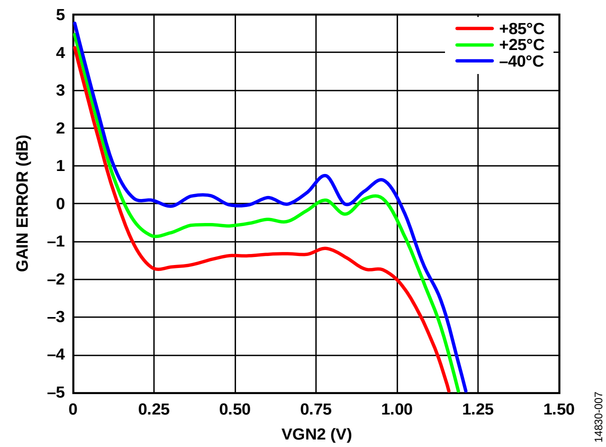


Figure 7. Gain Error at 500 MHz vs. VGN2 over Temperature; Bypass Mode, VGN1 = 1.5 V

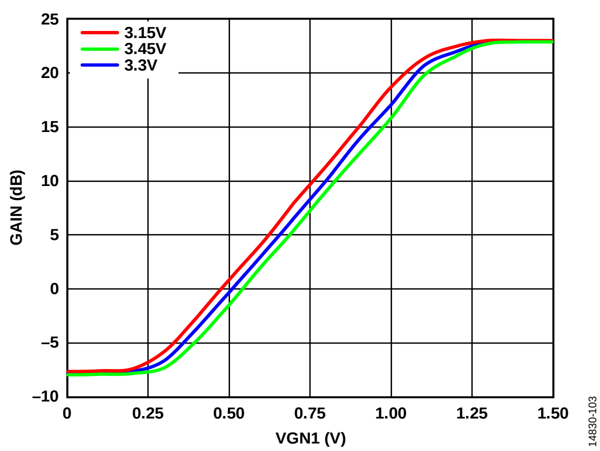


Figure 5. Gain at 500 MHz vs. VGN1 over Supply; Bypass Mode, VGN2 = 0 V

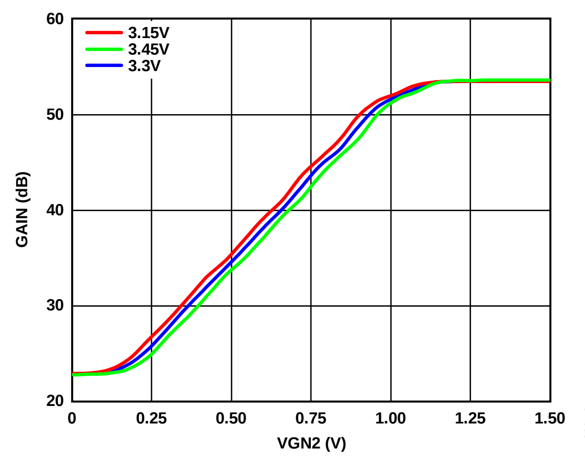


Figure 8. Gain at 500 MHz vs. VGN2 over Supply; Bypass Mode, VGN1 = 1.5 V

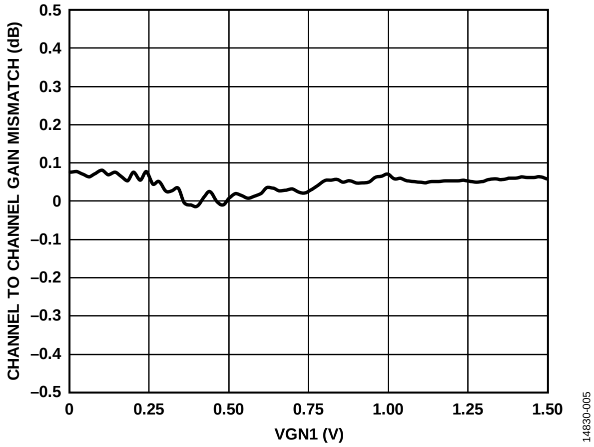


Figure 9. Channel to Chanel Gain Mismatch vs. VGN1; VGN2 = 0 V, Bypass Mode at 500 MHz

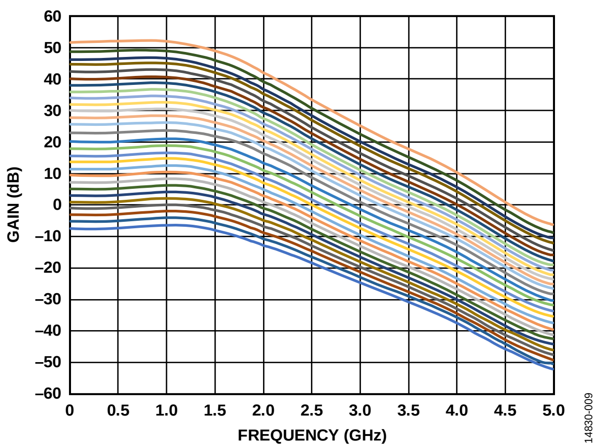


Figure 10. Gain vs. Frequency over VGN1/VGN2, 3 dB Gain Steps

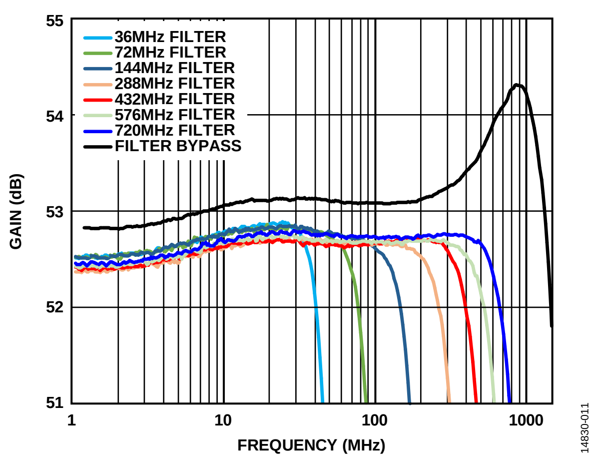


Figure 11. Gain vs. Frequency over all Bandwidth Settings; VGN1 = VGN2 = 1.5 V (Logarithmic)

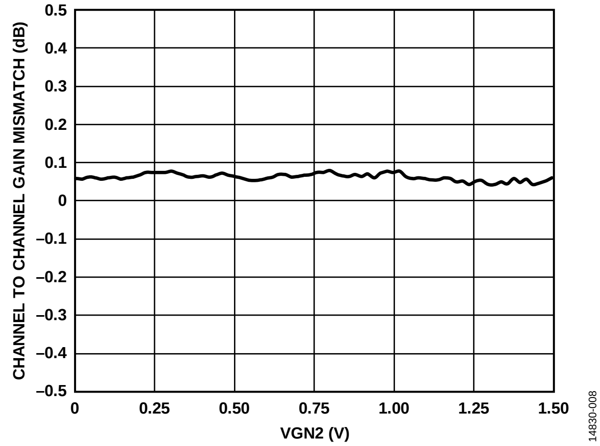


Figure 12. Channel to Chanel Gain Mismatch vs. VGN2; VGN1 = 1.5 V, Bypass Mode at 500 MHz

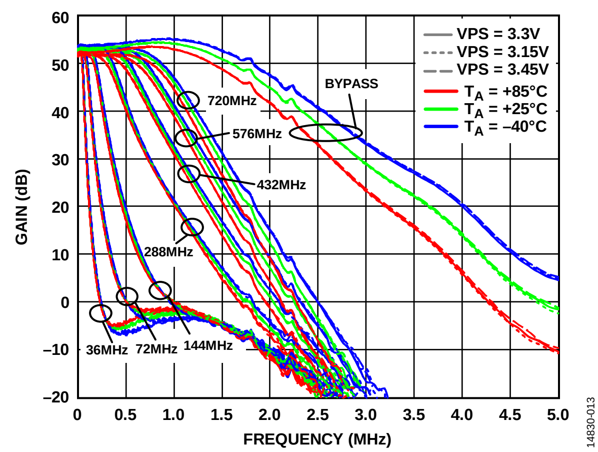


Figure 13. Frequency Response over Supply and Temperature for 36 MHz, 144 MHz, 288 MHz, 432 MHz, 576 MHz, and 720 MHz Filter Corners and Bypass

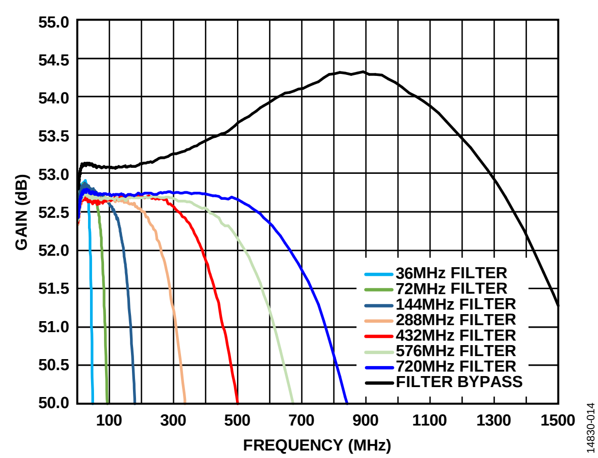


Figure 14. Gain vs. Frequency over all Bandwidth Settings; VGN1 = VGN2 = 1.5 V (Linear)

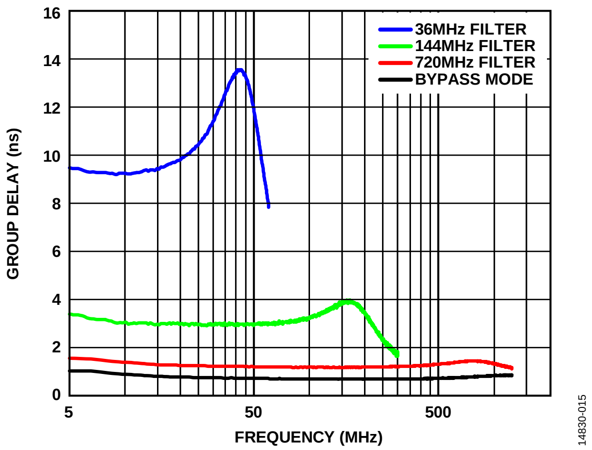


Figure 15. Group Delay vs. Frequency for 36 MHz, 144 MHz, 720 MHz, and Bypass Mode

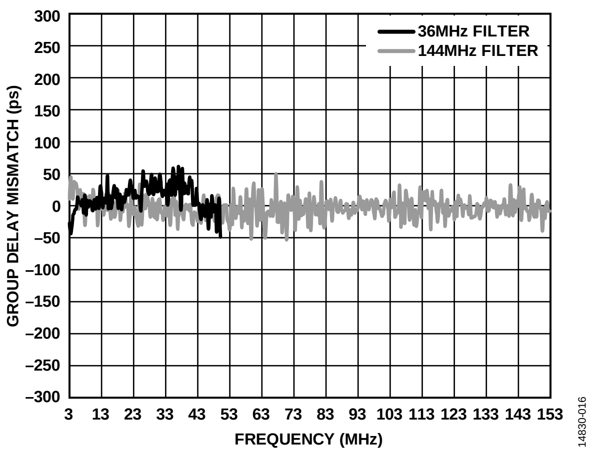


Figure 16. IQ Group Delay Mismatch vs. Frequency for 36 MHz and 144 MHz

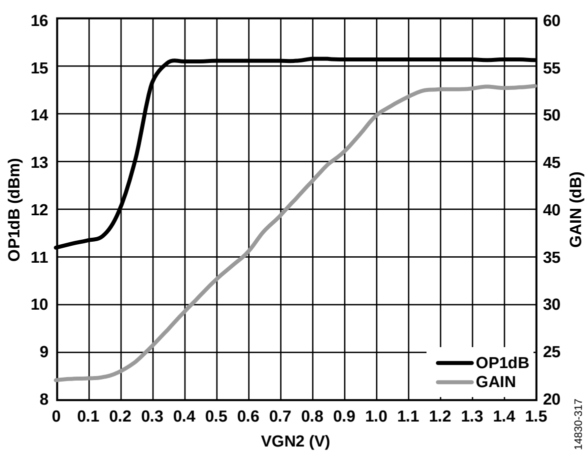


Figure 17. OP1dB vs. Gain at a Fundamental of 500 MHz

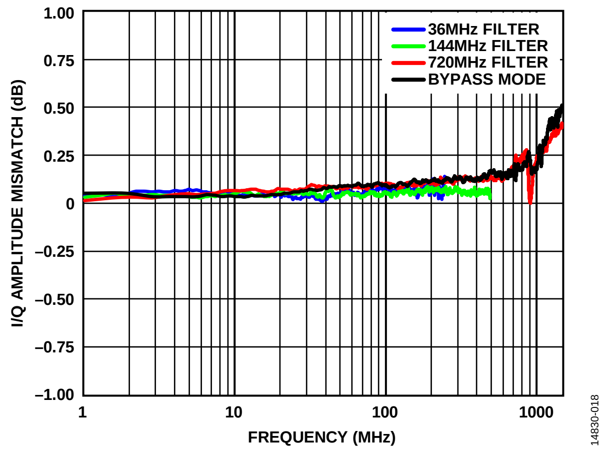


Figure 18. IQ Amplitude Mismatch vs. Frequency for 36 MHz, 144 MHz, 720 MHz, and Bypass Mode

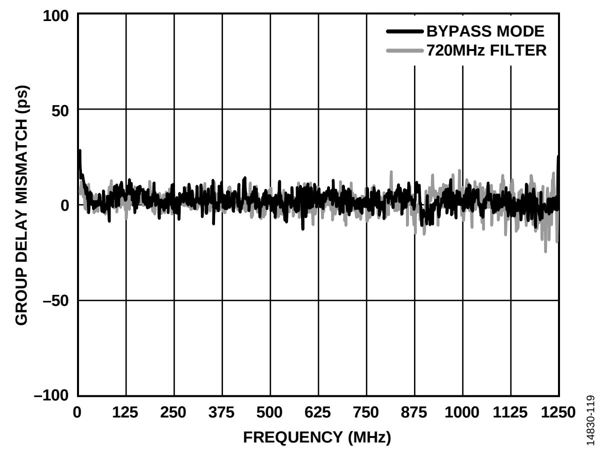


Figure 19. IQ Group Delay Mismatch vs. Frequency for 720 MHz and Bypass Mode

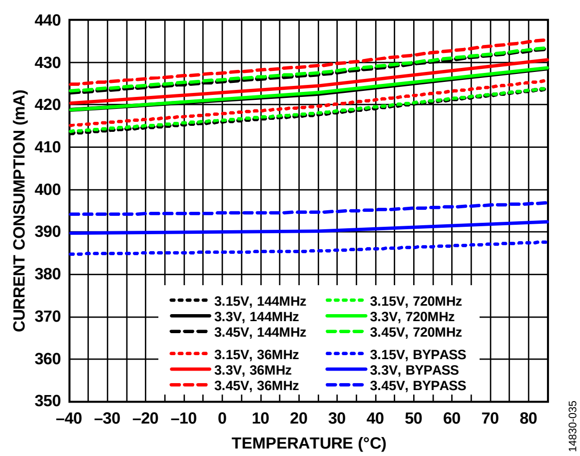


Figure 20. Current Consumption vs. Temperature for 36 MHz, 144 MHz, 720 MHz, and Bypass Mode

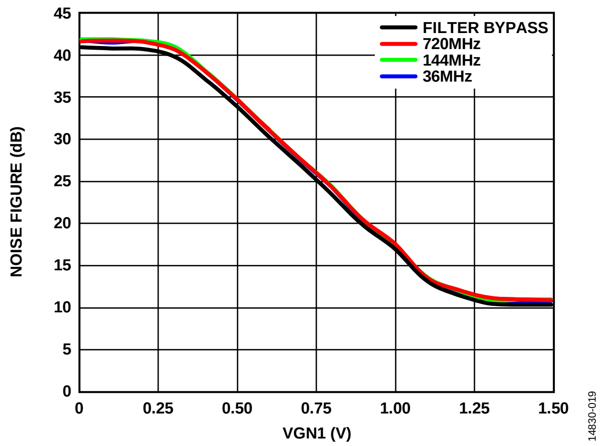


Figure 21. Noise Figure vs. VGN1 for 36 MHz, 144 MHz, 720 MHz, and Bypass; VGN2 = 1.5 V

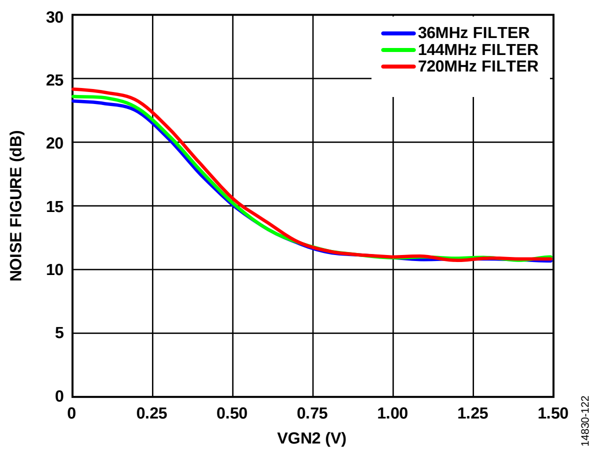


Figure 22. Noise Figure vs. VGN2 for 36 MHz, 144 MHz, 720 MHz; VGN1 = 1.5 V

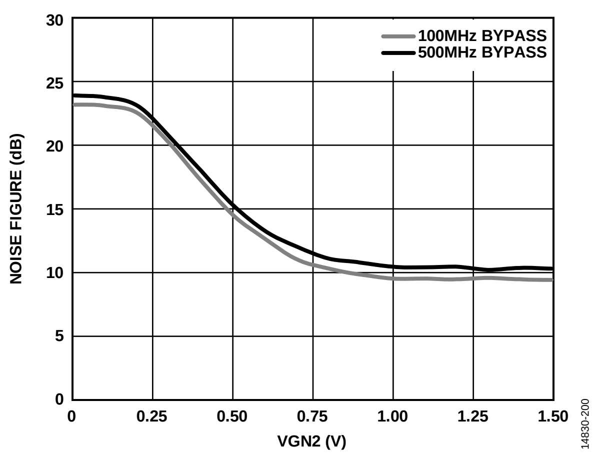


Figure 23. Noise Figure vs. VGN2 for Bypass Mode; NSD at 100 MHz and 500 MHz; VGN1 = 1.5 V

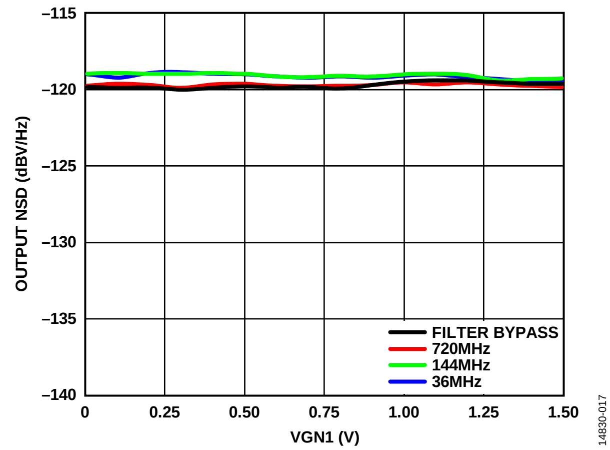


Figure 24. Output NSD vs. VGN1 for 36 MHz, 144 MHz, 720 MHz, and Bypass; VGN2 = 1.5 V

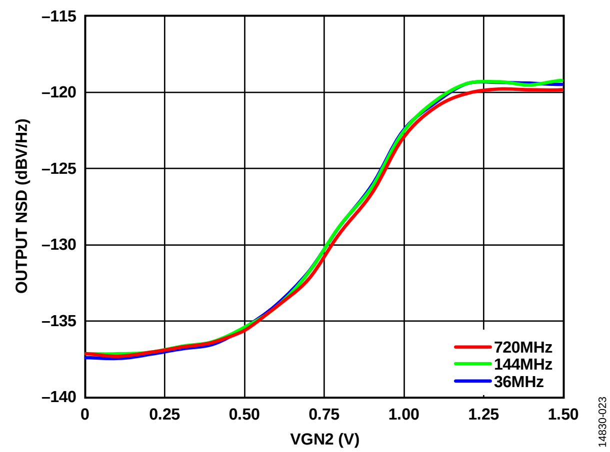


Figure 25. Output NSD vs. VGN2 for 36 MHz, 144 MHz, 720 MHz; VGN1 = 1.5 V

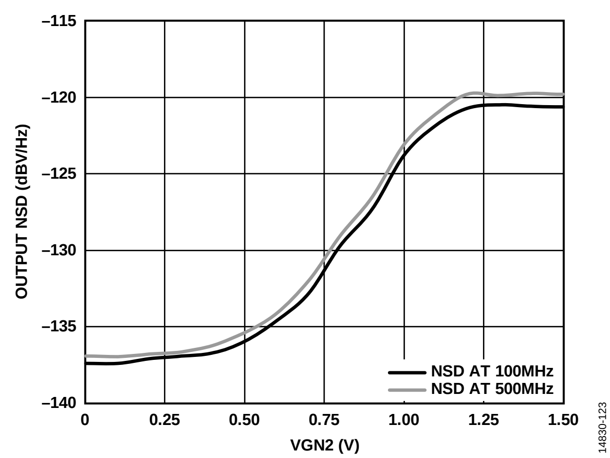


Figure 26. Output NSD vs. VGN2 for Bypass Mode; NSD at 100 MHz and 500 MHz; VGN1 = 1.5 V

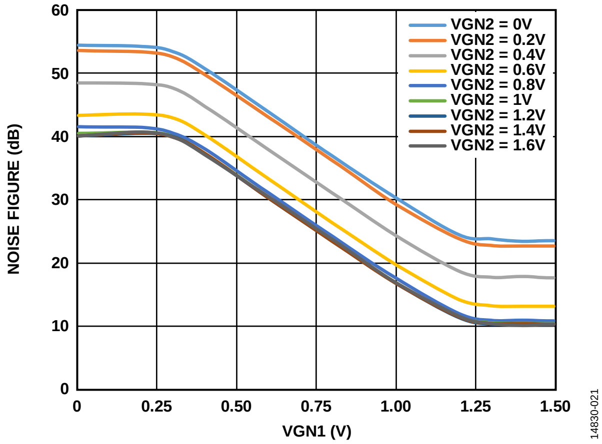


Figure 27. Noise Figure vs. VGN1 over VGN2, Bypass Mode

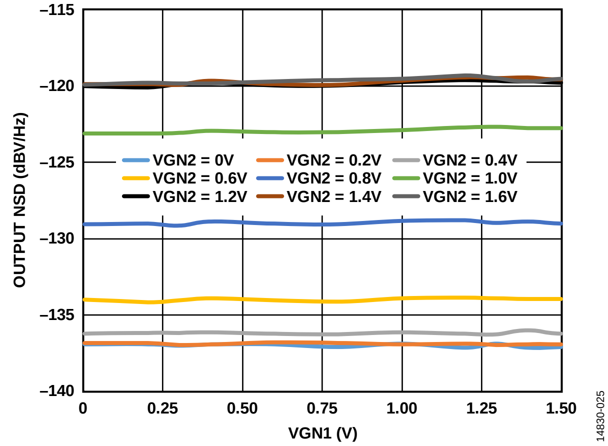


Figure 30. Output NSD vs. VGN1 over VGN2; Bypass Mode

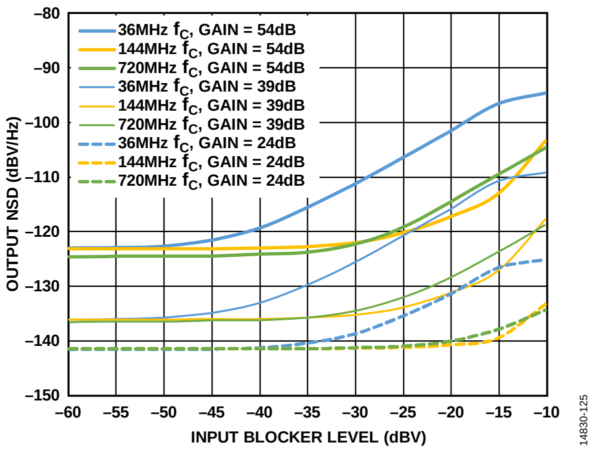


Figure 28. Output NSD vs. Input Blocker Level over VGA2 Gain and Filter Corners; VGN1 = 1.5 V

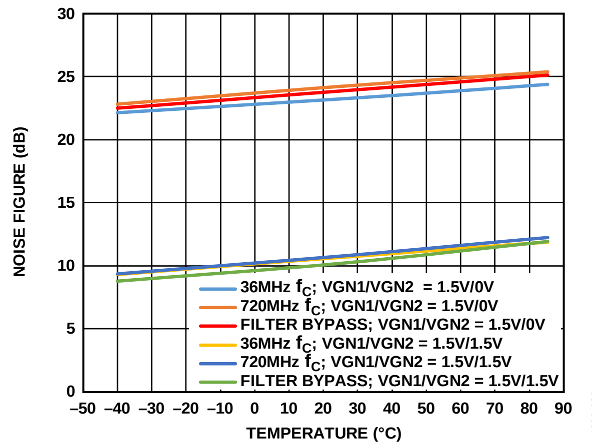


Figure 31. Noise Figure vs. Temperature over Bandwidth and Gain

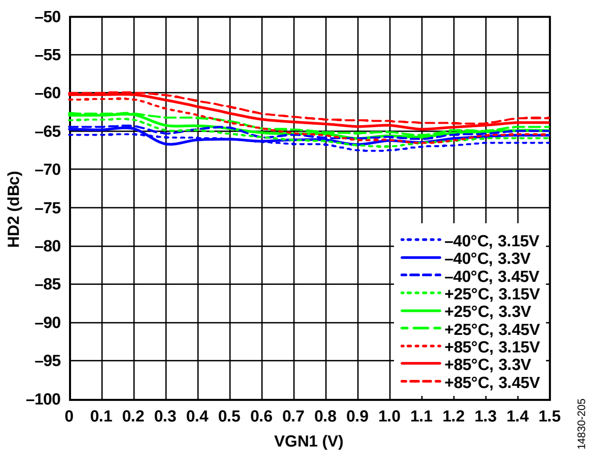


Figure 29. HD2 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p at Output, Bypass Mode

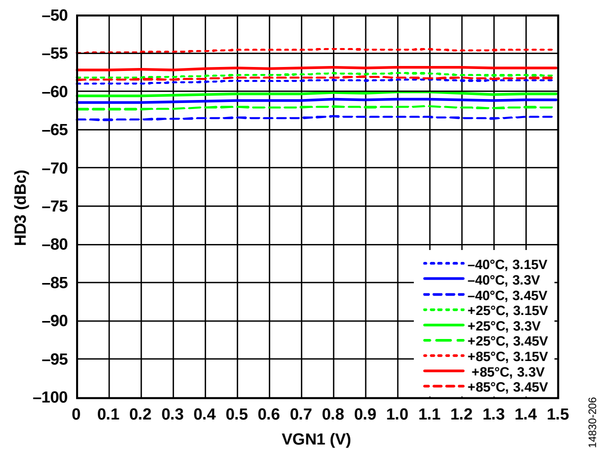


Figure 32. HD3 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p at Output, Bypass Mode

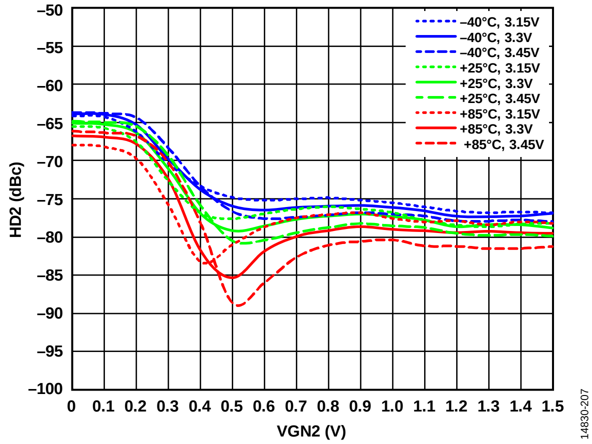


Figure 33. HD2 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p at Output, Bypass Mode

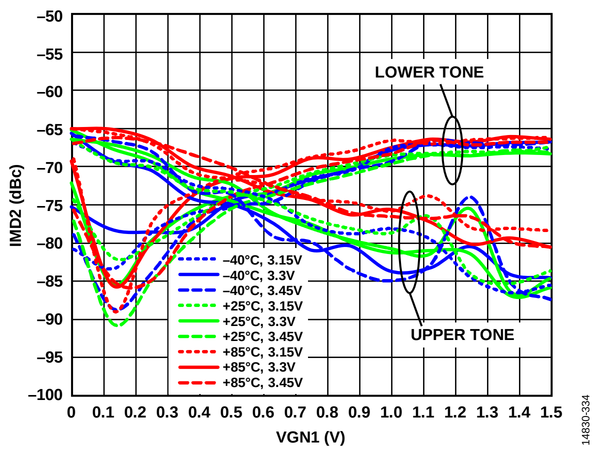


Figure 34. IMD2 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, 36 MHz Filter Corner

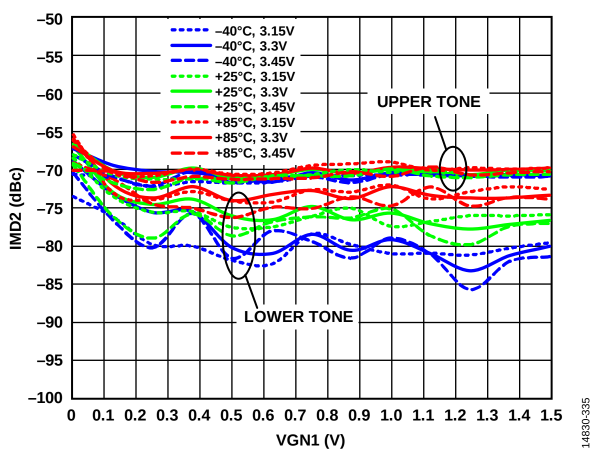


Figure 35. IMD2 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, 144 MHz Filter Corner

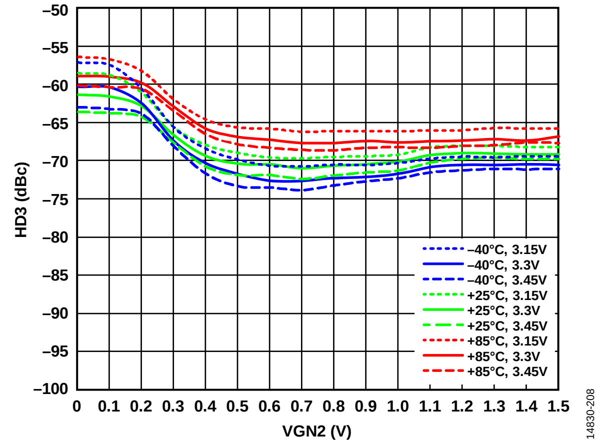


Figure 36. HD3 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p at Output, Bypass Mode

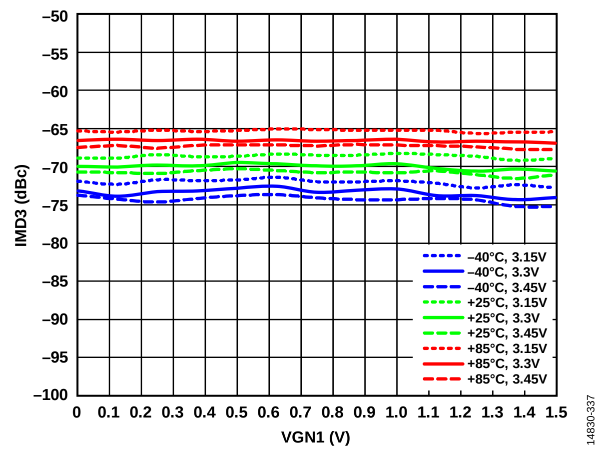


Figure 37. IMD3 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, 36 MHz Filter Corner

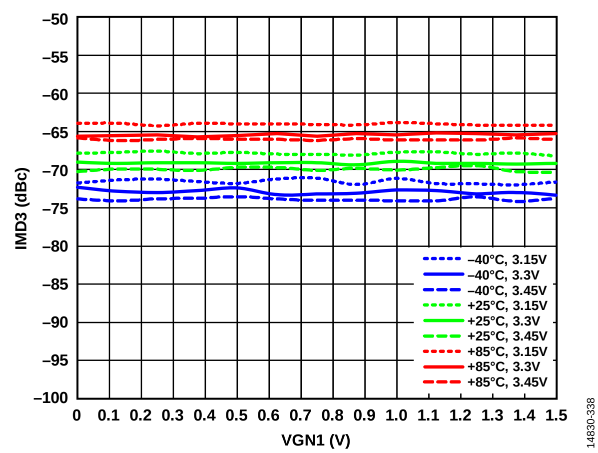


Figure 38. IMD3 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, 144 MHz Filter Corner

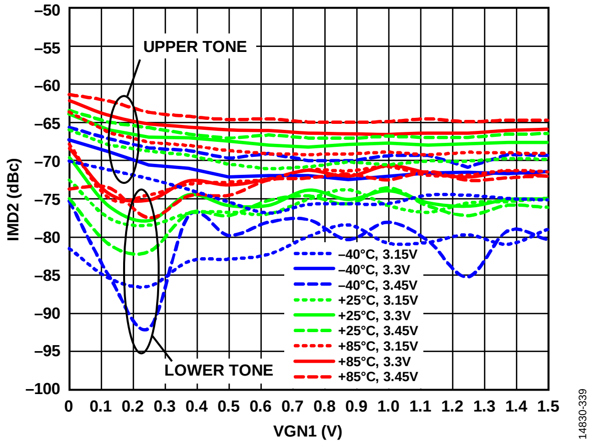


Figure 39. IMD2 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, 720 MHz Filter Corner

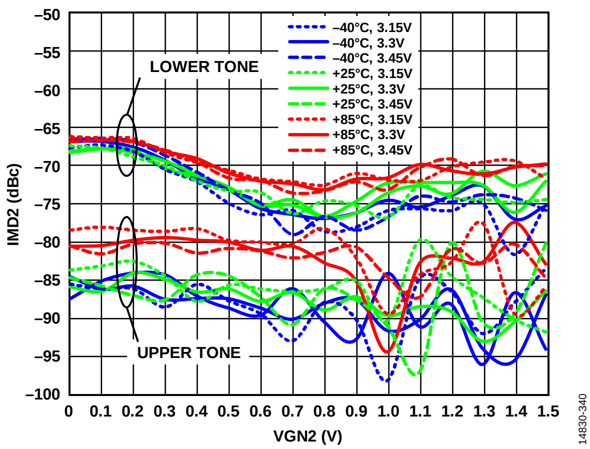


Figure 40. IMD2 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, 36 MHz Filter Corner

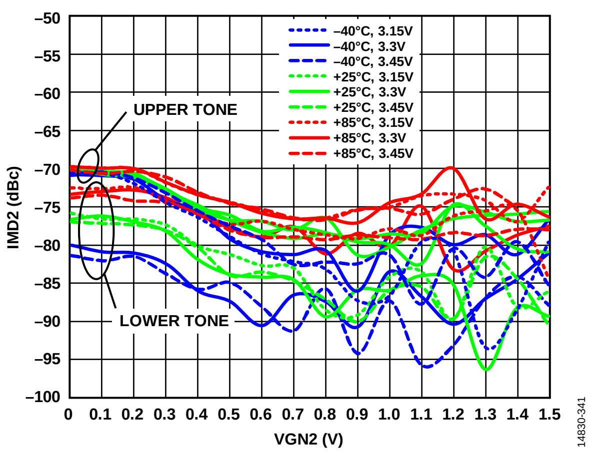


Figure 41. IMD2 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, 144 MHz Filter Corner

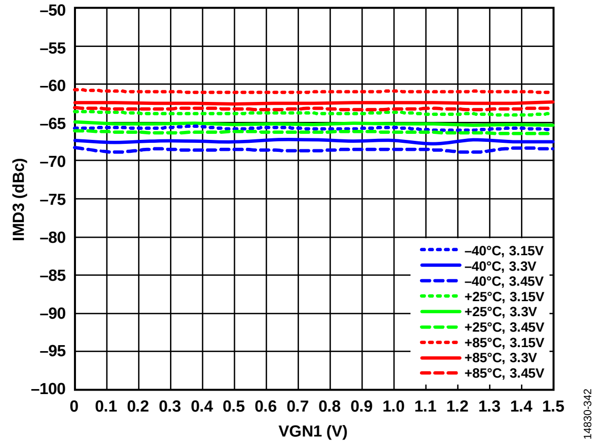


Figure 42. IMD3 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, 720 MHz Filter Corner

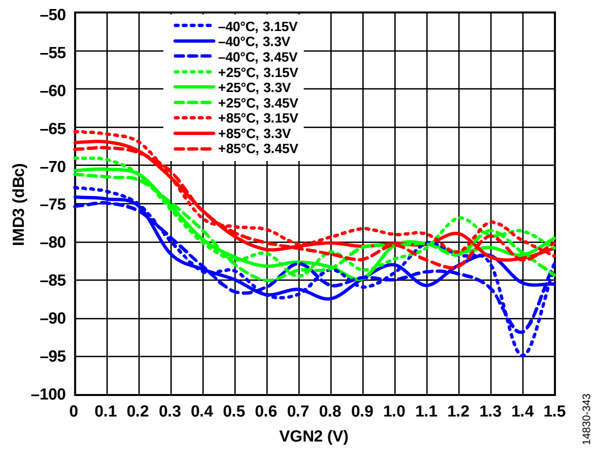


Figure 43. IMD3 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, 36 MHz Filter Corner

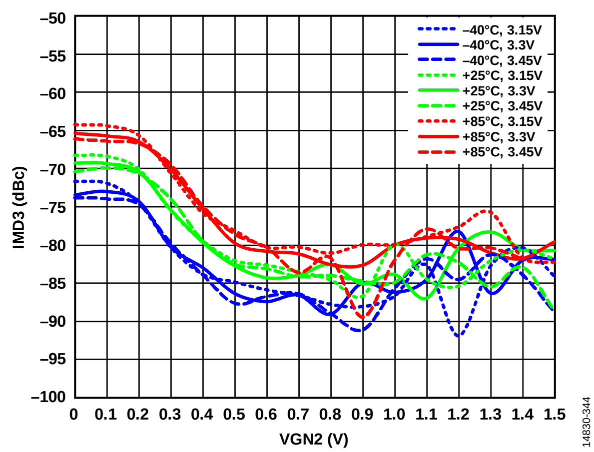


Figure 44. IMD3 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, 144 MHz Filter Corner

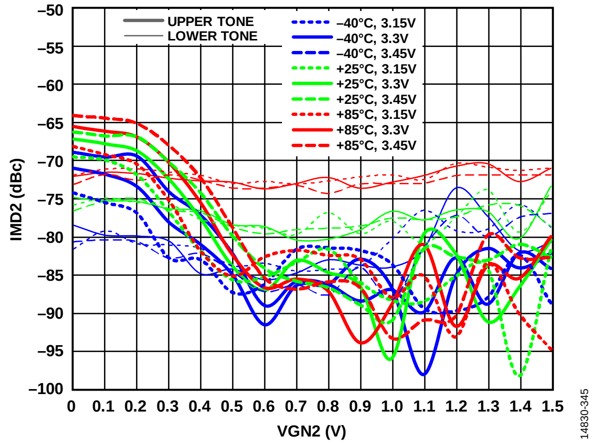


Figure 45. IMD2 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, 720 MHz Filter Corner

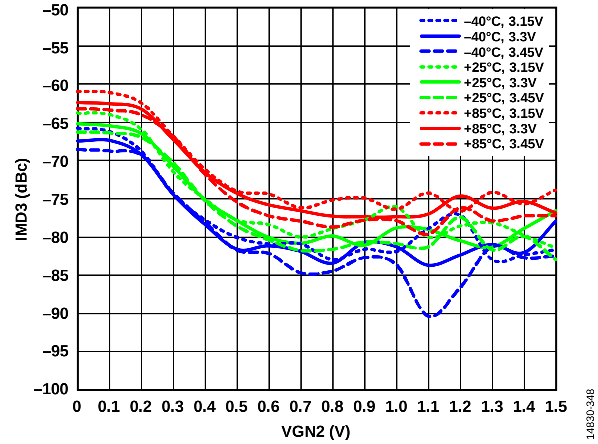


Figure 48. IMD3 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, 720 MHz Filter Corner

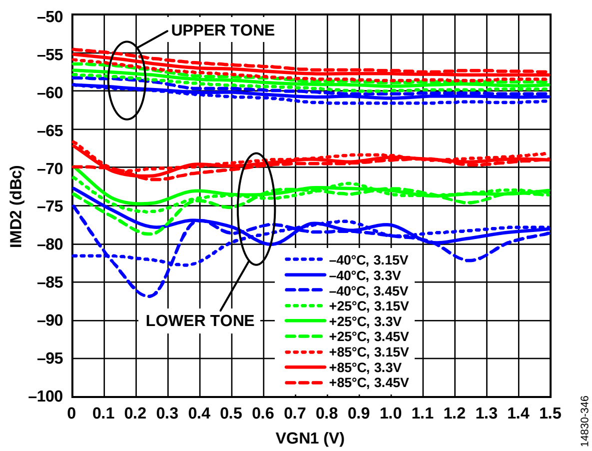


Figure 46. IMD2 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, Bypass Mode, 500 MHz Tones

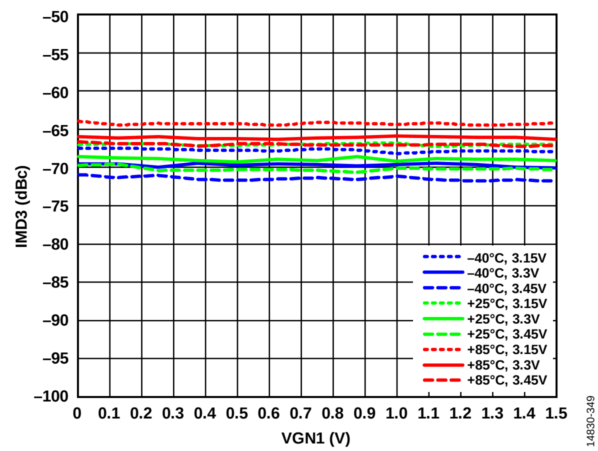


Figure 49. IMD3 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, Bypass Mode, 500 MHz Tones

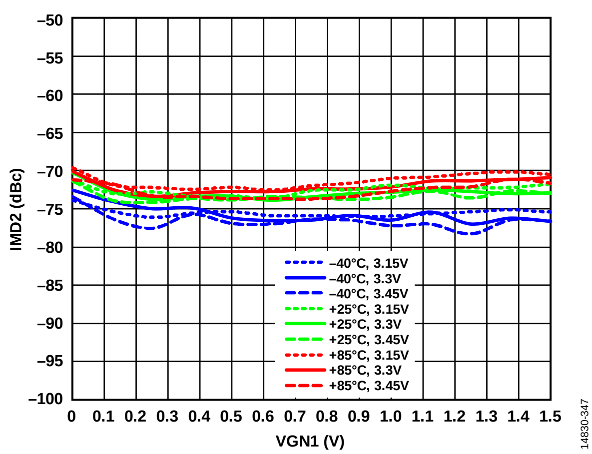


Figure 47. IMD2 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, Bypass Mode, 1 GHz Tones, Low Tone Measured

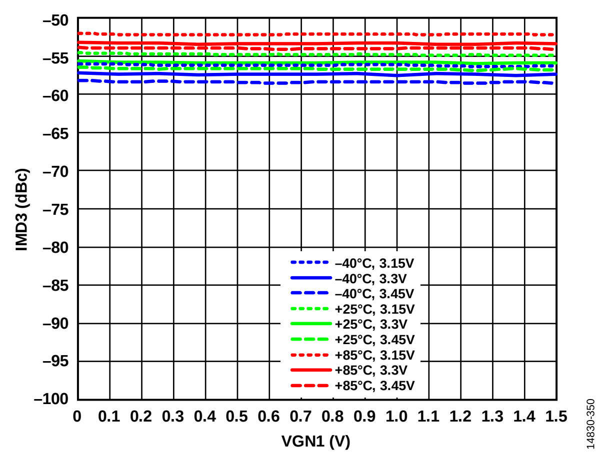


Figure 50. IMD3 vs. VGN1 over Supply and Temperature, VGN2 = 0 V, 1.5 V p-p Composite at Output, Bypass Mode, 1 GHz Tones

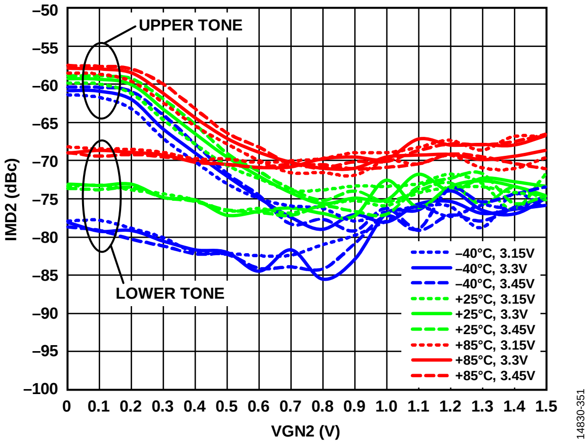


Figure 51. IMD2 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, Bypass Mode, 500 MHz Tones

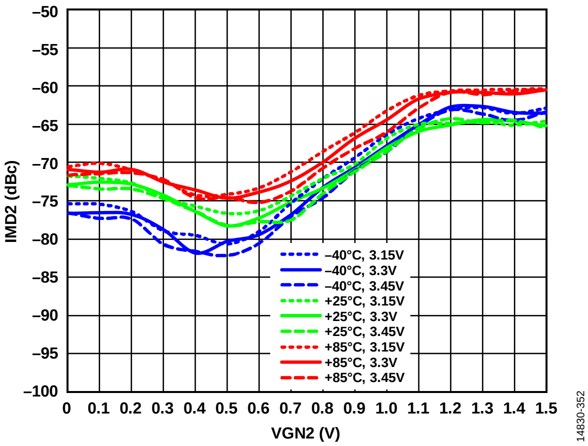


Figure 52. IMD2 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, Bypass Mode, 1 GHz Tones, Low Tone Measured

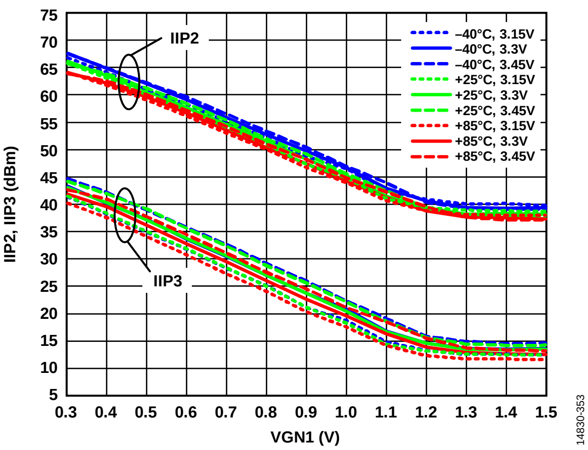


Figure 53. Input IP2 (IIP2), Input IP3 (IIP3) vs. VGN1, VGN2 = 0 V, Bypass Mode, 500 MHz Tones

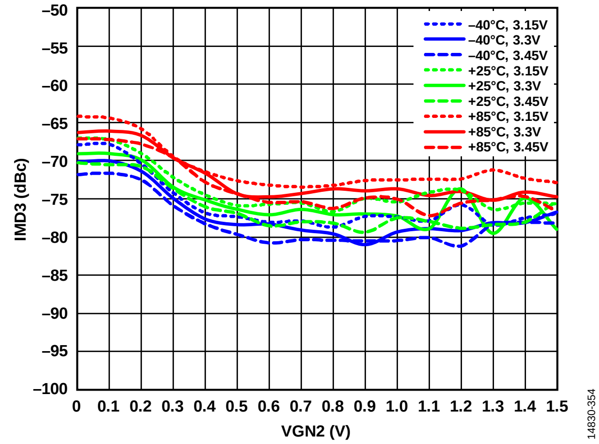


Figure 54. IMD3 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, Bypass Mode, 500 MHz Tones

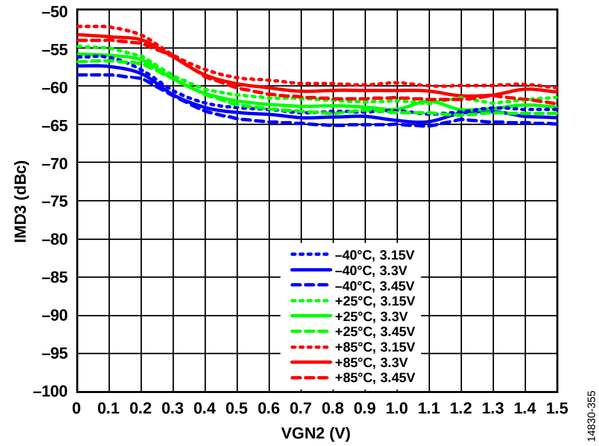


Figure 55. IMD3 vs. VGN2 over Supply and Temperature, VGN1 = 1.5 V, 1.5 V p-p Composite at Output, Bypass Mode, 1 GHz Tones

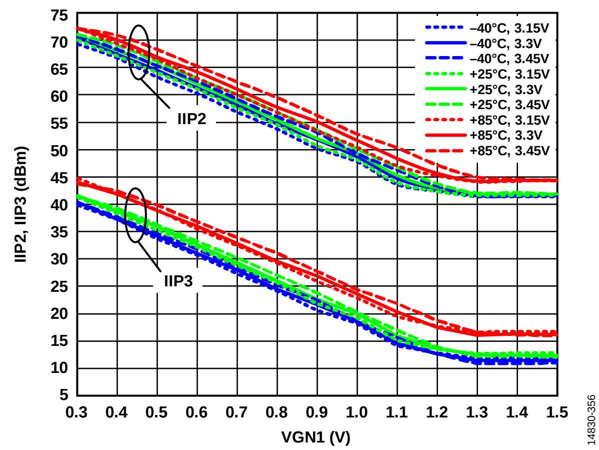


Figure 56. IIP2, IIP3 vs. VGN1, VGN2 = 0 V, Bypass Mode, 1 GHz Tones

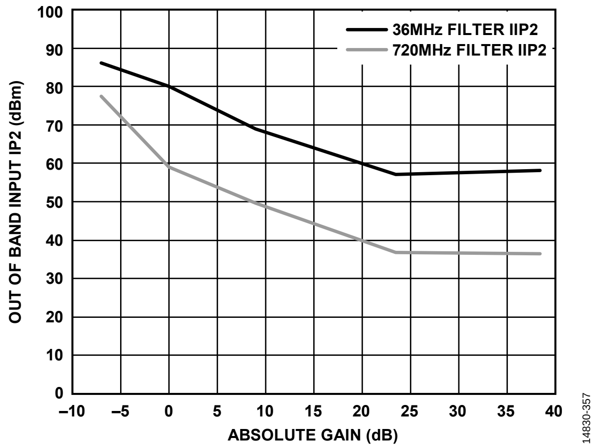


Figure 57. Out of Band IIP2, IMD2 for 36 MHz and 720 MHz

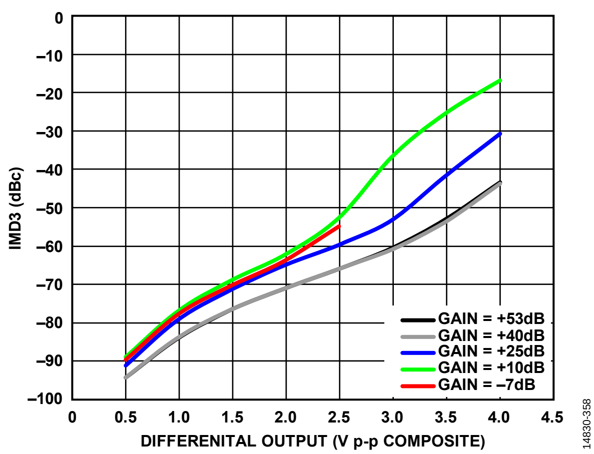


Figure 58. In Band IMD3 vs. Differential Output Voltage (V p-p Composite) over Gain, Bypass Mode at 500 MHz

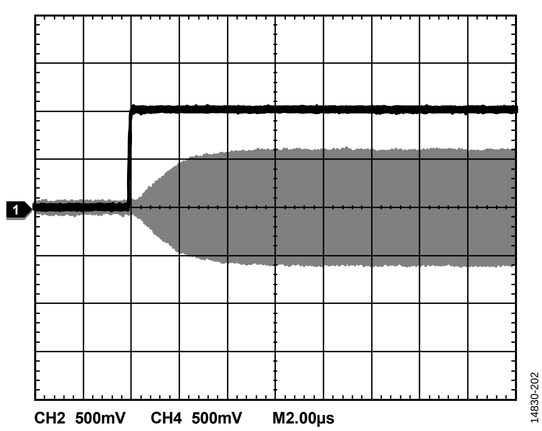


Figure 59. VGA1 Gain Step Response

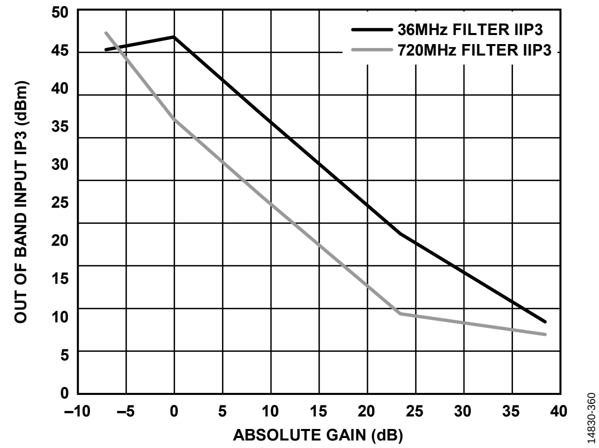


Figure 60. Out of Band IIP3, IMD3 for 36 MHz and 720 MHz

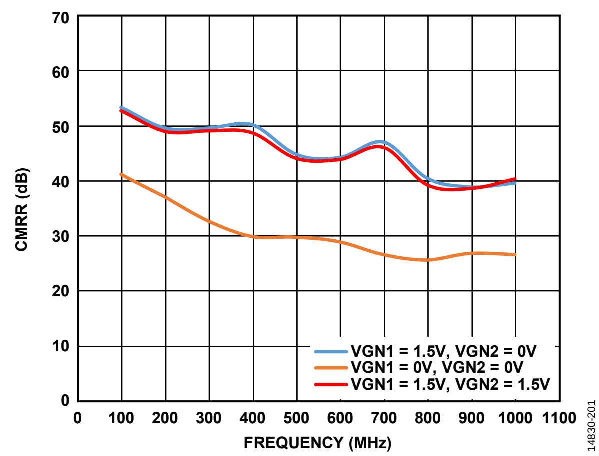


Figure 61. Common-Mode Rejection Ratio (CMRR) vs. Frequency, Bypass Mode

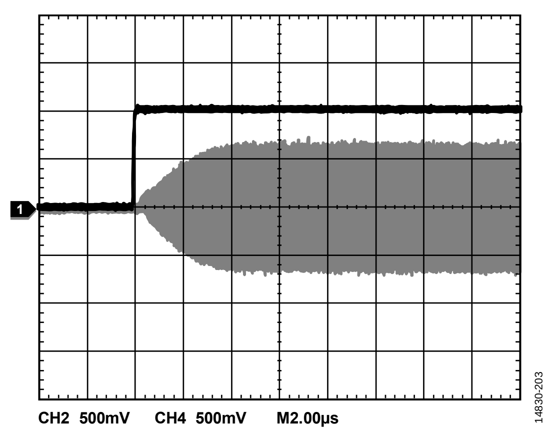


Figure 62. VGA2 Gain Step Response; C9 and C16 = Open

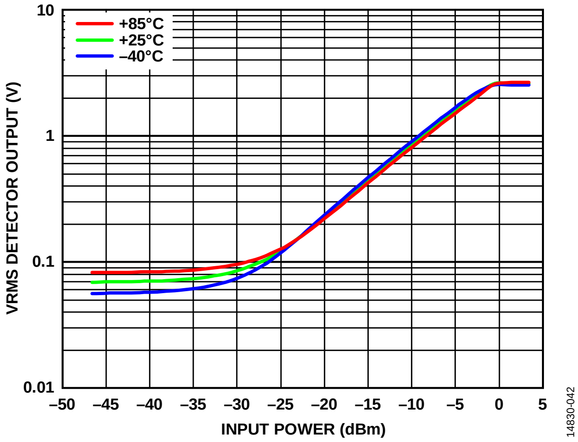


Figure 63. Detector Output vs. Input Power (P_{IN}) over Temperature, VGN1 = 1.5 V, VGN2 = 0 V, Both Inputs Driven to Same Amplitude

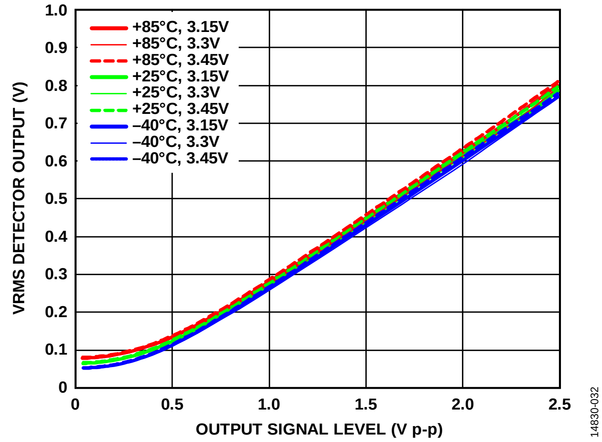


Figure 64. Detector Output Voltage vs. Output Signal Level (V p-p) over Supply and Temperature, VGN1 = 1.5 V, VGN2 = 0 V, Both Inputs Driven to Same Amplitude

THEORY OF OPERATION

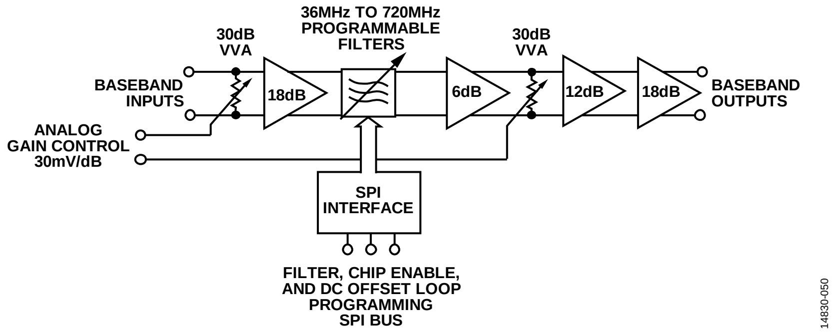


Figure 65. Signal Path Block Diagram for a Single Channel of the ADRF6520

The ADRF6520 consists of a matched pair of input VGAs followed by programmable filters, 6 dB fixed gain amplifiers, and finally another matched pair of variable gain amplifiers and output ADC drivers. The filters can be bypassed and powered down through the SPI interface for operation beyond the maximum filter bandwidth. The block diagram of a single channel is shown in Figure 65.

The programmability of the filter bandwidth through the SPI offers great flexibility when coping with signals in the presence of noise and large, undesired signals near the desired band. The entire differential signal chain is dc-coupled. The bandwidth and gain setting controls for the two channels are shared, ensuring close matching of their magnitude and phase responses. The ADRF6520 can be fully disabled through the ENBL pin or the enable bit in the SPI register.

Filtering and amplification are fundamental operations in any signal processing system. Filtering is necessary to select the intended signal while rejecting out of band noise and interferers. Amplification increases the level of the desired signal to overcome noise added by the system. When used together, filtering and amplification can extract a low level signal of interest in the presence of noise and out of band interferers. Such analog signal processing alleviates the requirements on the analog, mixed signal, and digital components that follow.

INPUT VGAs

The input VGAs are designed to have low noise and high linearity. The VGAs have a differential input impedance of 100 Ω, maximum gain of 18 dB, and minimum gain of −12 dB, providing a 30 dB gain range. They are designed to drive the filters with up to 1.5 V p-p of undesired signal or 0.75 V p-p of desired signal, or a combination of both. The input to the ADRF6520 must be ac-coupled. The topology of the input VGA is such that its noise figure (NF) degrades dB for dB as its gain is reduced, although its high linearity is maintained across its full input range. The input VGA can drive up to 3 V p-p at its output; however, it is recommended that the VGA be kept to the aforementioned limits to avoid overdriving the filter or 6 dB fixed gain amplifier.

RMS DETECTOR

To measure the signal level at the critical interface of the VGA1 output and the programmable filter input, an rms detector was implemented. The rms detector simultaneously measures both channels at the VGA1 output and reports the sum of the two at the VRMS pin. On-chip averaging capacitors set the minimum settling time for the VRMS voltage to roughly 50 ns for most of the signal measurement range. The on-chip capacitors can be augmented by placing capacitors between the CFLT1 and CFLT2 pins and VPS. Off-chip capacitors are needed in most cases to obtain an accurate rms measurement of the input signal, as well as to reduce the modulation ripple in the VRMS output voltage.

The rms detector responds in a linear in volts manner, with the VRMS voltage representing the rms value of the input signal with the following relationship at maximum VGA1 gain:

$$VRMS = k \times [\mathrm{RMS}(ch1\ input) + \mathrm{RMS}(ch2\ input)]$$

where RMS(x) is the root mean square value, and it is assumed that sufficiently large filtering capacitors are chosen to allow averaging of the modulation content.

The previous relationship applies at maximum VGA1 gain only. When VGA1 gain is reduced, the VRMS output voltage also decreases proportionately. Relating VRMS, the gain of VGA1 and the summation of the rms values of the channel inputs is

$$VRMS = 1(V/V_{RMS})(VGA1\ Linear\ Voltage\ Gain)(\mathrm{RMS}(ch1\ input) + \mathrm{RMS}(ch2\ input))$$

For example, if VGA1 is at its maximum gain of 18 dB, the equation reduces down to

$$VRMS = 8(V/V_{RMS})(\mathrm{RMS}(ch1\ input) + \mathrm{RMS}(ch2\ input))$$

And at the VGA1 minimum gain of −12 dB, the equation reduces down to

$$VRMS = 0.25(V/V_{RMS}) \times (\mathrm{RMS}(ch1\ input) + \mathrm{RMS}(ch2\ input))$$

The RC time constant that, to a first order, dictates the rise and fall times of the rms output is expressed with the following equation:

$$\tau \text{ (sec)} = 500\ \Omega \times (100 \text{ pF} + CFLTx)$$

where *CFLTx* is either the external CFLT1 value or CFLT2 value.

Therefore, for the example of CFLTx = 0 (no external capacitor), the settling time is 50 ns; and if CFLTx = 1 nF, the settling time is 550 ns. Note that this is the 90% settling time of the rms detector.

There is a slight dependency on input power level, wherein larger input signals to the rms detector cause it to settle more quickly. Also, the settling time varies with temperature. The simple equation, shown previously, is given for guidance so that the user can set the settling times within an order of magnitude of where they want it to be. If settling time is important, some experimentation by the user is necessary to optimize the CFLTx value for their system.

PROGRAMMABLE FILTERS

The integrated programmable filter is the key signal processing function in the ADRF6520. The filters follow a four-pole Butterworth type response that provides minimum in-band ripple and group delay variation, and good out of band rejection. The −1 dB bandwidth is programmed from 36 MHz to 720 MHz in six steps via the SPI, as described in the Programming the ADRF6520 section. The quoted corner frequency is the −1 dB point; the ADRF6520 has filter corners at 36 MHz, 72 MHz, 144 MHz, 288 MHz, 432 MHz, 576 MHz, and 720 MHz.

The filters are designed so that the gain and phase responses vs. frequency are retained for any bandwidth setting. Figure 66 and Figure 67 illustrate the ideal four-pole Butterworth response. The group delay, τ_G, is defined as

$$\tau_G = -\partial\varphi/\partial\omega$$

where:
φ is the phase in radians.
$\omega = 2\pi f$ is the frequency in radians per second.

Note that for a frequency scaled filter prototype, the absolute magnitude of the group delay scales inversely with the bandwidth; however, the shape is retained. For example, the peak group delay for a 36 MHz bandwidth setting is 20× more than for a 720 MHz setting.

The corner frequency of the filters is defined by the on-chip RC product, which can vary by ±20% over manufacturing variations. Therefore, all the devices are factory calibrated for corner frequency, resulting in a residual ±8% corner frequency variation over the −40°C to +85°C temperature range. Although absolute accuracy requires calibration, the matching of RC products between the pair of channels is better than 1% by observing careful design and layout practices. Calibration and excellent matching ensure that the magnitude and group delay responses of both channels track together, a critical requirement for digital IQ-based communication systems.

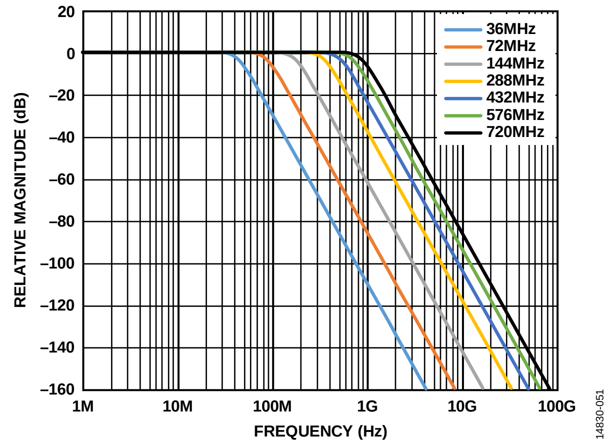


Figure 66. Ideal Fourth-Order Butterworth Magnitude Response for All 1 dB Bandwidths Programmed

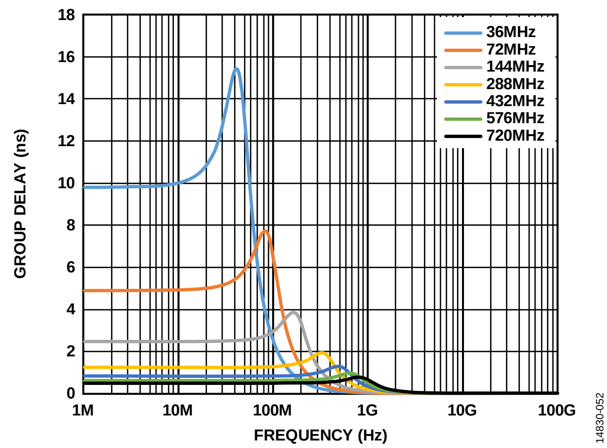


Figure 67. Ideal Fourth-Order Butterworth Group Delay Response for All 1 dB Bandwidths Programmed

Bypassing the Filters

For bandwidth applications greater than 720 MHz, the filters of the ADRF6520 can be bypassed via the SPI. In filter bypass mode, filters are disabled and power consumption is significantly reduced. The bandwidth of cascaded VGAs is fully realized in the filter bypass mode.

VARIABLE GAIN AMPLIFIERS

The second VGA, VGA2, is based on the same architecture as the input VGA, with 12 dB maximum gain and minimum gain of −18 dB, providing a 30 dB gain range controlled with a separate high impedance gain control input, the VGN2 pin. The basic VGA structure of the second VGA is identical to that of the first VGA. However, the VGA2 details vary slightly from VGA1 to produce a higher noise figure.

OUTPUT BUFFERS/ADC DRIVERS

The low impedance (<20 Ω) output buffers of the ADRF6520 have 18 dB of gain and are designed to drive either ADC inputs or subsequent amplifier stages. They are capable of delivering up to 3.5 V p-p composite two-tone signals into 100 Ω differential loads with >50 dBc IMD3. The output common-mode of the ADC driver is set internally to mid supply and cannot be adjusted. If the circuit must be dc-coupled, it must be coupled to a subsequent stage with matching common mode. However, if common-mode matching is not possible, take care to limit the dc common-mode current that is used to shift the common mode, or else poor linearity results are observed.

DC OFFSET COMPENSATION LOOP

In many signal processing applications, no information is carried in the dc level. In fact, dc voltages and other low frequency disturbances can often dominate the intended signal and consume precious dynamic range in the analog path and bits in the data converters. These dc voltages can be present with the desired input signal or can be generated inside the signal path by inherent dc offsets or other unintended signal-dependent processes such as self mixing or rectification.

It is recommended to use ac coupling capacitors at the input and output terminals of the ADRF6520. The ac coupling capacitors at the input block any dc offset from the input getting into the device. The coupling capacitors must be sufficiently large, because they form a high pass filter with the100 Ω differential input impedance plus any source impedance of the driving circuit. The high-pass corners may need to be <1 kHz in some cases.

To address the issue of dc offsets generated inside the device, the ADRF6520 provides a dc offset correction loop that nulls the output differential dc level, as shown in Figure 68. The correction loop can be disabled through the SPI port; however, when the correction loop is disabled, the dc offsets can consume nearly all of the output dynamic range, especially near maximum gain settings, because of the large gain of the ADRF6520.

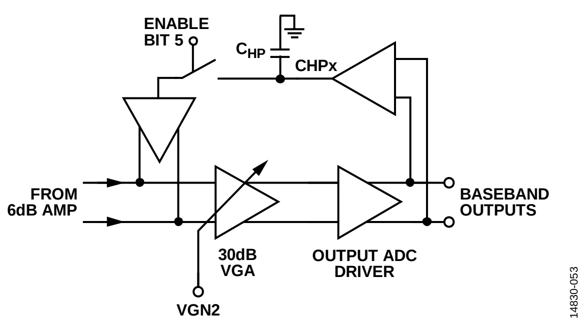


Figure 68. DC Offset Compensation Loop Operates Around the Second VGA and ADC Driver

The offset control loop creates a high-pass corner, f_{HP}, that is superimposed on the normal Butterworth filter response when filters are enabled. Typically, f_{HP} is many orders of magnitude lower than the lower programmed filter bandwidth so that there is no interaction between them. Setting f_{HP} is accomplished with capacitors, from the CHP1 and CHP2 pins to ground, as shown in Figure 68. Because the correction loop works around the VGA sections, f_{HP} is also dependent on the total gain of the cascaded VGAs.

In general, the expression for f_{HP} is given by

$$f_{HP}\ (\text{Hz}) = 16.1 \times \textit{VGA2 Linear Voltage Gain}/C_{OFS}\ (\mu\text{F})$$

where *VGA2 Linear Voltage Gain* is expressed in linear terms, not in decibels (dB), and is the gain following the offset correction amplifier, which excludes the all prior gain.

For example, the high-pass corner at maximum VGA2 gain, 30 dB, and with C_{OFS} = 1 µF, is calculated as follows:

$$f_{HP}\ (\text{Hz}) = 16.1 \frac{10^{30/20}}{1} = 509.1\ \text{Hz}$$

Note that f_{HP} increases in proportion to the gain. For this reason, choose C_{OFS} at the highest operating gain to guarantee that f_{HP} is always below the maximum limit required by the system.

PROGRAMMING THE ADRF6520

The filter frequency, filter bypass mode, chip enable, and dc offset correction loop enable are programmed simultaneously through the SPI port. A 24-bit register stores 8 data bits, 15 bits for addressing, and 1 bit for a read/write instruction (see Table 5). The SPI protocol allows these selections to be written into and read out of the SDIO pin (see the timing diagrams in Figure 69).

The chip select bar ($\overline{CS}$) pin must first go to a Logic 0 for a read or write cycle to begin. On the next rising edge of the clock (SCLK), a Logic 0 on the SDIO pin initiates a write cycle, whereas a Logic 1 on the SDIO pin initiates a read cycle. In a write cycle, the next 15 SCLK rising edges latch the desired 15-bit address, followed by the 8-bit data word. The result is a 24-bit code, including the first Logic 0 to initiate a write cycle. When $\overline{CS}$ goes high, the write cycle is completed, and different codes are presented to the filter, chip enable, and dc offset correction loop enable blocks that require programming. In a read cycle, after writing in a Logic 1 for the read/write bit and the 15 address bits, the SDIO changes from an input to an output in the ½ cycle of SCLK between the last rising edge of SCLK of the instruction (read/write bit and address bits) and the following falling edge. The next 8 SCLK rising edges present the stored 8-bit word of data, MSB first on the SDIO pin. When $\overline{CS}$ goes high, the read cycle is completed. Detailed timing diagrams are shown in Figure 69.

NOISE CHARACTERISTICS

The output noise behavior of the ADRF6520 primarily depends on the gain. Filter corner switching in ADRF6520 is achieved by changing the on-chip capacitors and keeping the resistors constant, which results in constant contribution from the filter to the total noise, irrespective of the filter corner. In filter bypass mode, noise contribution of the bypass switches is significantly lower than the active filter, which results in roughly 1 dB lower NF in the filter bypass mode than the filter mode, at maximum gain.

Each of the VGA sections used in the ADRF6520 contributes a fixed noise spectral density to its respective output, independent of the analog gain setting. When cascaded, the total noise contributed by the VGAs at the output of the ADRF6520 increases gradually with higher gain. This behavior is apparent in the noise floor variation at different VGA gain settings.

At low values of the VGA2 gain, the noise at the output is the flat spectral density contributed by VGA2. As the VGA2 gain increases, more of the filter and VGA1 noise is gained up by VGA2, and the noise of the filter and VGA1 appears at the output.

Because the noise spectral density outside the filter bandwidth is limited by the VGA output noise, it may be necessary to use an external, fixed frequency, passive filter prior to analog-to-digital conversion to prevent noise aliasing from degrading the signal-to-noise ratio (SNR). A higher sampling rate, relative to the maximum required ADRF6520 corner frequency setting, reduces the order and complexity of this external filter.

DISTORTION CHARACTERISTICS

To maintain low distortion through the cascaded VGAs and filter of the ADRF6520, consider the distortion limits of each stage. The first VGA has higher signal handling capability and slightly more bandwidth than the 6 dB amplifier and VGA2, because it must cope with out of band signals that can be larger than the in-band signals. In filter mode, these out of band signals are filtered before reaching the 6 dB amplifier and VGA2. It is important to understand the signals presented to the ADRF6520 and to match these signals with the input and output characteristics of the device. It is useful to partition the ADRF6520 into the front end (composed of VGA1 and the filter) and the back end (composed of the 6 dB amplifier and VGA2).

VGA1 can handle a 4 V p-p signal at a maximum analog attenuation setting (VGN1 = 0 V) without experiencing appreciable distortion at the input. In most applications, VGA1 gain must be adjusted such that the maximum signal presented at the filter inputs (or the input of the 6 dB amplifier in filter bypass mode) is <1.5 V p-p. At this level, the front end does not limit the distortion performance. The rms detector output, VRMS, can be used as an indicator of the signal level present at this critical interface. Choose the second VGA gain such that its output levels do not exceed 1.5 V p-p if the user wants to achieve better than 55 dBc HD2/HD3 linearity.

For these signal level considerations, it is recommended that the out of band signal, if larger than the desired in-band signal, be addressed. In filter mode, such an out of band signal only affects the VGA1 operation, because it is filtered out by the filter and does not affect the following stages. In this case, a high VGA2 gain may be needed to raise the small desired signal to a higher level at the output. In filter bypass mode, such out of band signals may need to be filtered prior to the ADRF6520.

The overall distortion introduced by the device depends on the input drive level, including the out of band signals, and the desired output signal level. To achieve best distortion performance and the desired overall gain, keep in mind the maximum signal levels indicated previously in this section when selecting different VGA gains.

To distinguish and quantify the distortion performance of the input section, two different IP2 and IP3 specifications are presented. The first is called in-band IP2/IP3 and refers to a two-tone test where the signals are inside the filter bandwidth. This specification is exactly the same figure of merit familiar to communications engineers in which the second-order and third-order intermodulation levels, IMD2 and IMD3 respectively, are measured.

To quantify the effect of out of band signals, an out of band IIP2 and IIP3 figure of merits are introduced. These tests also involve two-tone stimulus; however, the two tones are placed out of band so that the lower IMD product falls in the middle of the filter pass band. At the output, only the IMD product is visible because the original two tones are filtered out. To calculate the out of band IIP2/IIP3 at the input, the IMD2/IMD3 level is referred to the input by the overall gain. The out of band IIP2/IIP3 allows the user to predict the impact of out of band blockers or interferers at an arbitrary signal level on the in-band performance. The ratio of the desired input signal level to the input referred IMD2/IMD3 at a given blocker level represents a signal-to-distortion limit imposed by the out of band signals.

MAXIMIZING THE DYNAMIC RANGE

When used in filter mode, the role of the ADRF6520 is to increase the level of a variable in-band signal while minimizing out of band signals. Ideally, this increase is achieved without degrading the SNR of the incoming signal or introducing distortion to the incoming signal.

The first goal is to maximize the output signal swing, which can be defined by the ADC input range or the input signal capacity of the next analog stage. For the complex waveforms often encountered in communication systems, the peak to average ratio, or crest factor, must be considered when choosing the peak-to-peak output. From the chosen output signal and the maximum gain of the ADRF6520, the minimum input level can be defined.

As the input signal level increases, the VGA2 gain is reduced from its maximum gain point to maintain the desired fixed output level. VGA1 can then be adjusted as the input signal level keeps increasing. This sequencing of the gain maintains the best NF for the cascaded chain. The output noise, initially dominated by the filter and VGA1 combination, follows the gain reduction, yielding a progressively better SNR. At some point, the VGA2 gains drop sufficiently so that their noise becomes dominant, resulting in a slower reduction in SNR from that point. From the perspective of SNR alone, the maximum input level is reached when the VGA1 reaches its minimum gain.

Distortion must also be considered when maximizing the dynamic range. At low and moderate signal levels, the output distortion is constant and assumed to be adequate for the selected output level. At some point, the input signal becomes large enough that distortion at the input limits the system. This distortion can be kept in check by monitoring the rms detector voltage, VRMS.

The most challenging scenario in terms of dynamic range is the presence of a large out of band blocker accompanying a weaker in-band wanted signal. In this case, the maximum input level is dictated by the blocker and its inclination to cause distortion. After filtering, the weak wanted signal must be amplified to the desired output level, possibly requiring the maximum gain on VGA2. In such a case, both the distortion limits associated with the blocker at the input and the SNR limits created by the weaker signal and higher gains are present simultaneously. Furthermore, not only does the blocker scenario degrade the dynamic range, it also reduces the range of input signals that can be handled because a larger part of the gain range is used to extract the weak desired signal from the stronger blocker.

KEY PARAMETERS FOR QUADRATURE-BASED RECEIVERS

The majority of digital communication receivers use quadrature signaling, in which bits of information are encoded onto pairs of baseband signals that then modulate in-phase (I) and quadrature (Q) sinusoidal carriers. Both the baseband and modulated signals appear quite complex in the time domain with dramatic peaks and valleys. In a typical receiver, the goal is to recover the pair of quadrature baseband signals in the presence of noise and interfering signals after quadrature demodulation. In the process of filtering out of band noise and unwanted interferers and restoring the levels of the wanted I and Q baseband signals, it is critical to retain their gain and phase integrity over the bandwidth.

In filter mode, the ADRF6520 delivers flat, in band gain and group delay, consistent with a four-pole Butterworth prototype filter, as described in the Programmable Filters section. Furthermore, careful design ensures excellent matching of these parameters between the I and Q channels. Although absolute gain flatness and group delay can be corrected with digital equalization, mismatch introduces quadrature errors and intersymbol interference that degrade bit error rates in digital communication systems.

For signals greater than 720 MHz of bandwidth, the filters can be bypassed, and the ADRF6520 then becomes a dual cascaded chain of two VGAs, offering a large gain range while maintaining gain and group delay match between the two channels.

SPI REGISTER AND TIMING

The filter frequency, filter bypass mode and offset correction loops can be programmed using the SPI interface. Table 5 provides the bit map for the internal 24-bit register of the ADRF6520.

Table 5. Bit Map

MSB **LSB**

B24	[B23:B9]	B8	[B7:B6]	B5	B4	[B3:B1]
Read/write bit	Address bits	Enable	Don't care	DC offset disable	Don't care	Filter frequency code
0: write operation 1: read operation	Set to 000000000010000	0: disable 1: enable	Don't care	0: disable 1: enable	Don't care	1 dB corner in MHz 000: 36 MHz 001: 72 MHz 010: 144 MHz 011: 288 MHz 100: 432 MHz 101: 576 MHz 110: 720 MHz 111: bypass

Table 6. Bit Map Default on Power-Up

MSB **LSB**

B24	[B23:B9]	B8	[B7:B6]	B5	B4	[B3:B1]
Read/write bit	Address bits	Enable	Don't care	DC offset disable	Don't care	Filter frequency code
0	000000000010000	1	Don't care	1	Don't care	111

REGISTER READ/WRITE TIMING

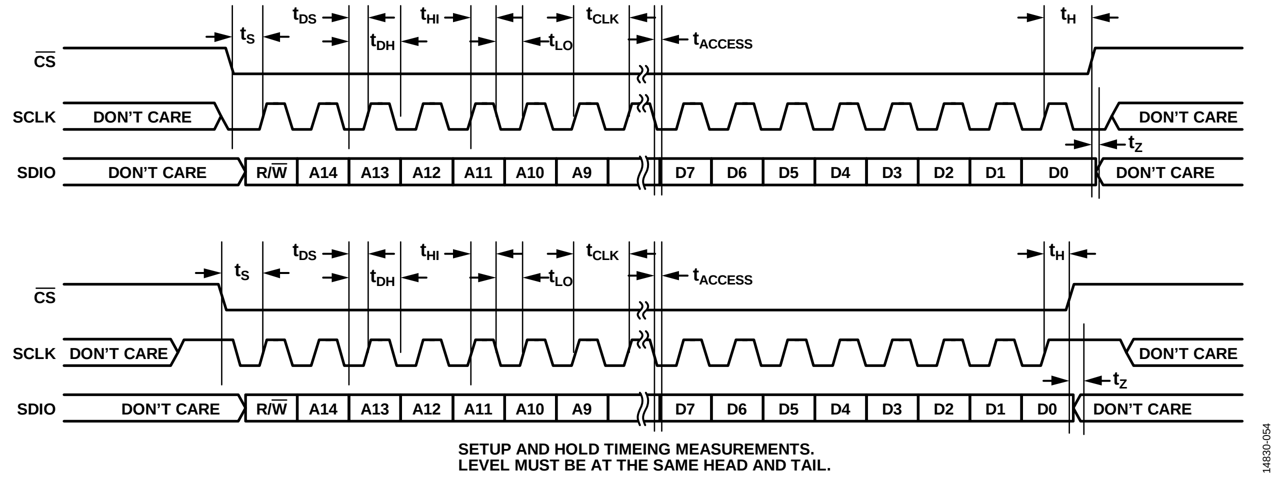


Figure 69. SPI Port Read and Write Timing Diagrams

Table 7. SPI Port Timing Specifications

Symbol	Description
t_{DS}	Setup time between data and rising edge of SCLK
t_{DH}	Hold time between data and rising edge of SCLK
t_{CLK}	Period of the clock
t_S	Setup time between $\overline{CS}$ and SCLK
t_H	Hold time between $\overline{CS}$ and SCLK
t_{HI}	Minimum period that SCLK must be in a logic high state
t_{LO}	Minimum period that SCLK must be in a logic low state
t_Z	Maximum time delay between $\overline{CS}$ deactivation and SDIO or SDO bus return to high impedance
t_{ACCESS}	Maximum time delay between falling edge of SCLK and output data valid for a read operation

B24 = 0 initiates a write, and B24 = 1 initiates a read. The instruction word (B24 followed by the 15 address bits) is written to the device, MSB first (as shown in Figure 69), followed by the data. The SDIO pin becomes an output pin after receiving the instruction header with a readback request. In read mode, the SDIO line must be changed from an input to an output in the half cycle of SCLK between the last rising edge of SCLK of the instruction and the following falling edge. When $\overline{CS}$ is deasserted, SDIO returns to high impedance until the next read transaction.

The interface is capable of reading and writing at speeds of at least 25 MHz (t_{CLK} = 40 ns). The hold time (t_{DH}) is less than 25% of the clock period. The setup time (t_{DS}) is less than 25% of the clock period. There is no minimum interface speed.

Write Cycle

The instruction word, followed by the register data, is written serially into the device through the SDIO pin on the rising edges of the interface clock, SCLK. The device is configured in MSB first mode and descending addressing.

Read Cycle

The instruction word is written to the device MSB first, followed by the data. Chip readback is sent via the SDIO. The SDIO pin becomes an output pin after receiving the instruction header with a readback request. In read mode, the SDIO line must be changed from an input to an output in the half cycle of SCLK between the last rising edge of SCLK of the instruction and the following falling edge. When $\overline{CS}$ is deasserted, SDIO returns to high impedance until the next read transaction.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 70 shows the basic connections for a typical ADRF6520 application.

SUPPLY DECOUPLING

Apply a nominal supply voltage of 3.3 V to the supply pins, VPS and VPSD. The supply voltage must not exceed 3.45 V or drop below 3.15 V for VPS and VPSD. Decouple each supply pin to ground with at least one low inductance, surface-mount ceramic capacitor of 0.1 µF placed as close as possible to the ADRF6520 device.

The ADRF6520 has two separate supplies: one analog supply and one digital supply. Take care to separate the analog and digital supplies with a large surface-mount inductor of 33 µH. Then decouple each supply separately to its respective ground through a 10 µF capacitor.

INPUT SIGNAL PATH

Each signal path has an input VGA, accessed through the INP1, INM1, INP2, and INM2 pins, which sets a differential input impedance of 100 Ω.

The inputs can be dc-coupled or ac-coupled, but ac coupling is preferred. There is no mechanism to change the common-mode voltage; therefore, if the user wants to dc-couple, the common-mode voltage of the previous stage must match the ADRF6520 input common-mode voltage of 1.375 V.

OUTPUT SIGNAL PATH

The low impedance (20 Ω) output buffers are designed to drive a 100 Ω impedance load, but can drive larger resistive loads. The output pins (OPP1, OPM1, OPP2, and OPM2) sit at a nominal output common-mode voltage of 1.65 V. The outputs can be dc-coupled or ac-coupled; however, ac coupling is preferred. There is no mechanism to change the output common-mode voltage; therefore, if the user wants to dc-couple, the common-mode voltage of the following stage must match the ADRF6520 output common-mode voltage of 1.65 V.

DC OFFSET COMPENSATION LOOP ENABLED

When the dc offset compensation loop is enabled via Bit B5 of the SPI register, the ADRF6520 can null the output differential dc level. The loop is enabled by setting Bit B5 to 1. The offset compensation loop creates a high-pass corner frequency, which is proportional to the value of the capacitors that are connected from the CHP1 and CHP2 pins to ground. For more information about setting the high-pass corner frequency, see the DC Offset Compensation Loop section.

SERIAL PORT CONNECTIONS

The ADRF6520 has a SPI port to control the filter bandwidth, chip enable, and dc offset compensation loop. Data can be written to the internal 24-bit register and read from the register. It is recommended that low-pass RC filtering be placed on the SPI lines to filter out any high frequency glitches. See the evaluation board schematic in the ADRF6520-EVALZ user guide for an example of a low-pass RC filter.

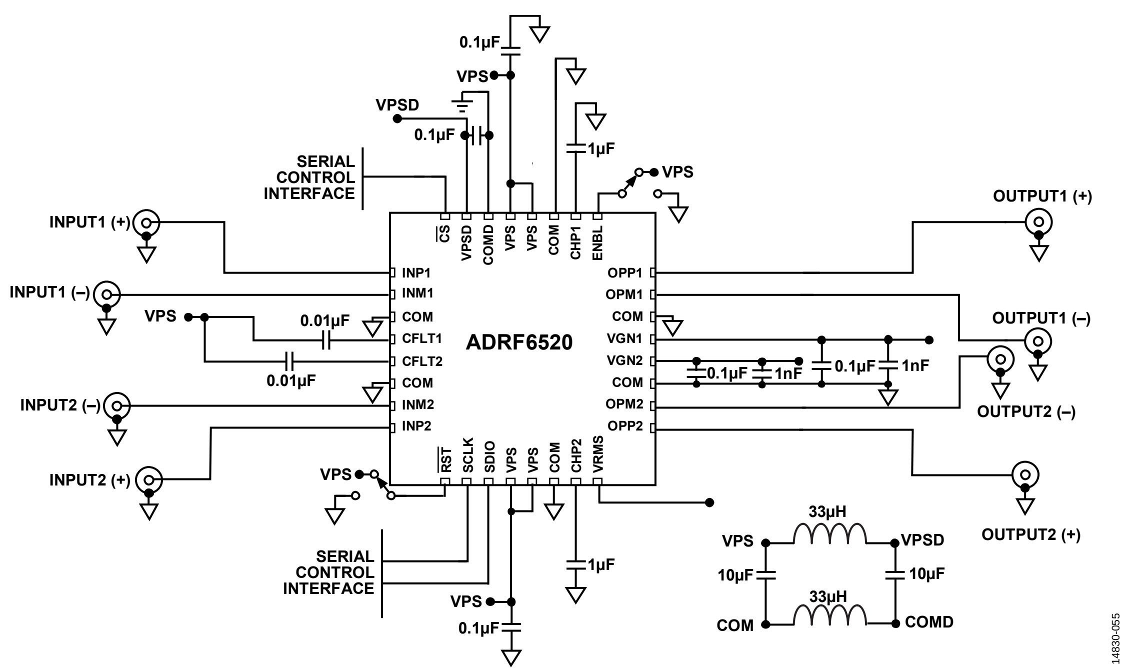


Figure 70. Basic Connections

ENABLE/DISABLE FUNCTION

To enable the ADRF6520, pull the ENBL pin high and set the enable bit in the SPI register (B8) to a logic 1 (by default, the ADRF6520 powers up with B8 = 1). Either driving the ENBL pin low or setting B8 = 0 disables the device, reducing current consumption to approximately 1 mA at room temperature.

GAIN PIN DECOUPLING

The ADRF6520 has two analog gain control pins: VGN1 and VGN2. Use at least one low inductance, surface-mount ceramic capacitor with a value of 0.1 µF and one 1000 pF in parallel to ground on each gain pin to decouple. An example of this can be seen in the evaluation board schematic in the ADRF6520-EVALZ user guide.

RMS DETECTOR CONNECTIONS

The ADRF6520 has an rms detector output on the VRMS pin, with a scaling of 1 V/V rms differential at filter inputs. VRMS output reports a scaled summation of the differential rms voltage of both channels: 1 V/V rms × (CH1_RMS + CH2_RMS).

CFLT1 and CFLT2 control the averaging of the Channel 1 and Channel 2 rms detectors, respectively. The user can leave these pins open for the fastest response time. The equation relating the VRMS output video bandwidth and the CFLT1 (or CFLT2) capacitor is given by

$$Video\ BWRMS\ (\text{Hz}) = 0.0007/(130\ \text{pF} + CFLTx)$$

where *CFLTx* is the value of either CFLT1 or CFLT2.

The VRMS pin can source up to 3 mA of current. The output structure is an NPN emitter follower type, with a 9.5 kΩ resistor placed from VRMS to ground, internally (see Figure 71). Do not to load the VRMS output with any load less than 1 kΩ.

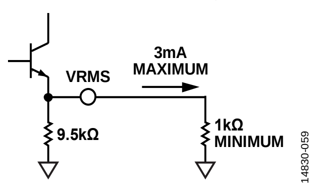


Figure 71. Simplified Schematic of VRMS Output

VGA2 GAIN STEP RESPONSE

VGA2 gain step response is affected by the dc offset correction loop. The bandwidth of the loop is set by the value of the CHP1 and CHP2 capacitors. Changing the value of the CHPx capacitors changes the signature and settling time of VGA2 gain step response. Figure 62 in the Typical Performance Characteristics section shows the VGA2 gain step response without the CHPx capacitor installed. Settling time is approximately 3 µs, and there are no transient events of any kind while the output settles. This is not the case when there is a large capacitor placed on CHPx. Figure 72 shows the VGA2 gain step response with a 1 µF capacitor placed on CHPx. Settling time is increased to approximately 750 µs, and there is a large transient shift on the output. The user wants to keep f_{HP} as low as possible to minimize the corruption of the low frequency spectral information. Care must be taken when choosing the CHPx capacitor values, to find the correct balance of the high-pass corner (f_{HP}) imposed on the signal paths vs. the VGA2 gain step response time. The larger the CHPx capacitor, the lower f_{HP} corner. The trade-off for lowering f_{HP} is longer VGA2 gain step response settling times and larger transient values on the output.

The user must determine what their needs and priorities are for their application and decide what specifications (f_{HP} vs. VGA2 step response time) to trade-off to satisfy their total system requirements.

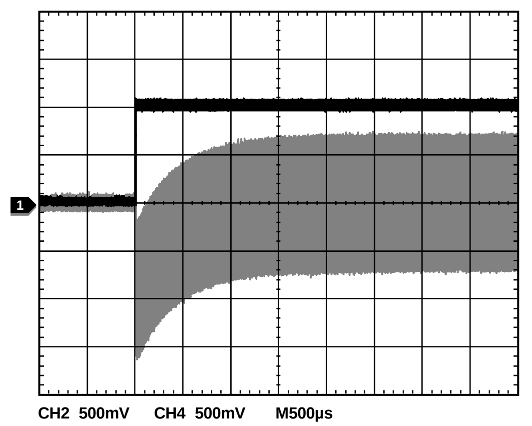


Figure 72. VGA2 Gain Step Response; C9 or C16 = 1 µF

LINEAR OPERATION OF THE ADRF6520

The ADRF6520 has multiple stages per channel. Each stage can independently be driven into compression depending on the gain settings and input signal level. There is only access to the input stages (INP1/INM1 and INP2/INM2) and the output stages (OPP1/OPM2 and OPP2/OPM2); therefore, the user must infer the signal level at the input and output of each stage from the device under test (DUT) input signal level and the analog gain settings. The maximum recommended signal levels are shown in Figure 73. Signal levels are presented in units of V p-p differential, and their equivalent power in dBm re:100 Ω.

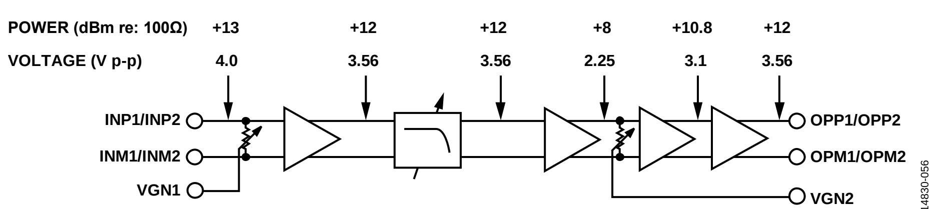


Figure 73. Maximum Signal Levels—Single Channel Shown

EVALUATION BOARD

An evaluation board is available for testing the ADRF6520. Information on control software and board setup is available in the ADRF6520-EVALZ user guide. Also available in the user guide are the schematic, bill of materials, top level layout drawing, and bottom level layout drawing.

Software, schematics, the bill of materials, and Gerber files are available to download from the ADRF6520 product page.

OUTLINE DIMENSIONS

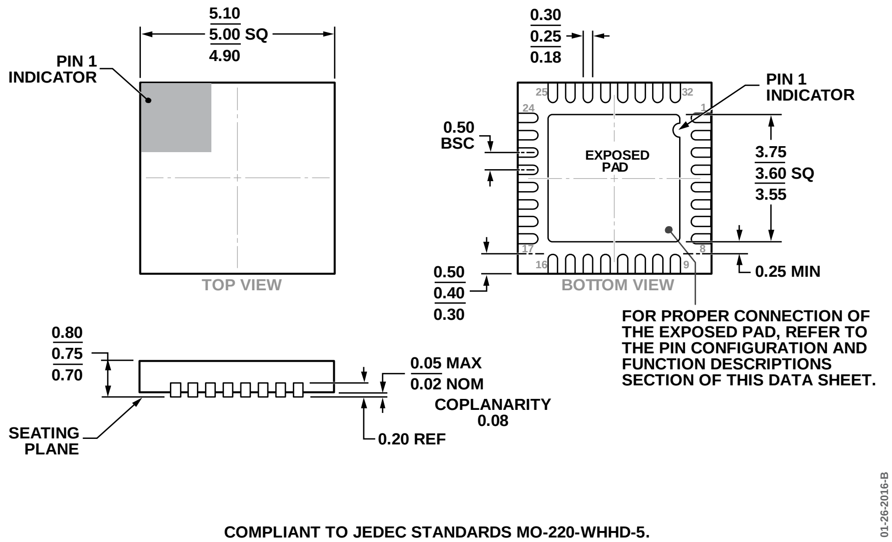


Figure 74. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADRF6520ACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-12
ADRF6520ACPZ-R7	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP], 7" Tape and Reel	CP-32-12
ADRF6520-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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D14830-0-4/17(0)

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