

# MC100LVEL16

## 3.3V ECL Differential Receiver

### Description

The MC100LVEL16 is a differential receiver. The device is functionally equivalent to the EL16 device, operating from a 3.3 V supply. The LVEL16 exhibits a wider  $V_{IHCMR}$  range than its EL16 counterpart. With output transition times and propagation delays comparable to the EL16 the LVEL16 is ideally suited for interfacing with high frequency sources at 3.3 V supplies.

Under open input conditions, the Q input will be pulled down to  $V_{EE}$  and the  $\bar{Q}$  input will be biased to  $V_{CC}/2$ . This condition will force the Q output low.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu\text{F}$  capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

### Features

- 300 ps Propagation Delay
- High Bandwidth Output Transitions
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range:  $V_{CC} = 3.0\text{ V}$  to  $3.8\text{ V}$  with  $V_{EE} = 0\text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0\text{ V}$  with  $V_{EE} = -3.0\text{ V}$  to  $-3.8\text{ V}$
- Internal Input Pulldown Resistors on D, Pullup and Pulldown Resistors on  $\bar{D}$
- Q Output will Default LOW with Inputs Open or at  $V_{EE}$
- Pb-Free Packages are Available



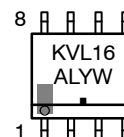
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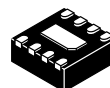
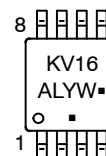
### MARKING DIAGRAMS\*



SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
M = Date Code  
▪ = Pb-Free Package

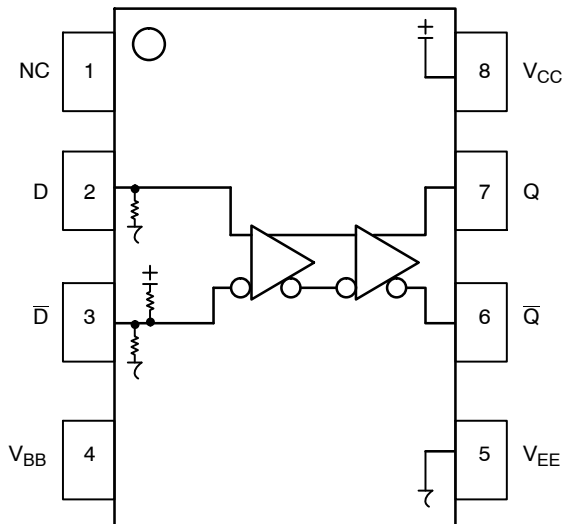
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC100LVEL16



**Table 1. PIN DESCRIPTION**

| PIN             | FUNCTION   |
|-----------------|--|
| D, $\bar{D}$    | ECL Data Inputs  |
| Q, $\bar{Q}$    | ECL Data Outputs   |
| V <sub>BB</sub> | Reference Voltage Output   |
| V <sub>CC</sub> | Positive Supply  |
| V <sub>EE</sub> | Negative Supply  |
| NC              | No Connect   |
| EP              | (DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open. |

**Figure 1. Logic Diagram and Pinout Assignment**

**Table 2. ATTRIBUTES**

| Characteristics  | Value   |
|--|---|
| Internal Input Pulldown Resistor                       | 75 k $\Omega$   |
| Internal Input Pullup Resistor                         | 75 k $\Omega$   |
| ESD Protection   | Human Body Model > 4 kV<br>Machine Model > 400 V<br>Charged Device Model > 2 kV |
| Moisture Sensitivity (Note 1)                          | Level 1   |
| Flammability Rating                                    | Oxygen Index: 28 to 34<br>UL 94 V-0 @ 0.125 in                                  |
| Transistor Count                                       | 79  |
| Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |   |

1. Refer to Application Note AND8003/D for additional information.

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**Table 3. MAXIMUM RATINGS**

| Symbol           | Parameter  | Condition 1                                    | Condition 2  | Rating            | Unit         |
|------------------|--|--|--|-------------------|--------------|
| V <sub>CC</sub>  | PECL Mode Power Supply                             | V <sub>EE</sub> = 0 V                          |  | 8 to 0            | V            |
| V <sub>EE</sub>  | NECL Mode Power Supply                             | V <sub>CC</sub> = 0 V                          |  | -8 to 0           | V            |
| V <sub>I</sub>   | PECL Mode Input Voltage<br>NECL Mode Input Voltage | V <sub>EE</sub> = 0 V<br>V <sub>CC</sub> = 0 V | V <sub>I</sub> ≤ V <sub>CC</sub><br>V <sub>I</sub> ≥ V <sub>EE</sub> | 6 to 0<br>-6 to 0 | V<br>V       |
| I <sub>out</sub> | Output Current                                     | Continuous<br>Surge                            |  | 50<br>100         | mA<br>mA     |
| I <sub>BB</sub>  | V <sub>BB</sub> Sink/Source                        |  |  | ± 0.5             | mA           |
| T <sub>A</sub>   | Operating Temperature Range                        |  |  | -40 to +85        | °C           |
| T <sub>stg</sub> | Storage Temperature Range                          |  |  | -65 to +150       | °C           |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 LFPM<br>500 LFPM                             | SO-8<br>SO-8   | 190<br>130        | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | SO-8   | 41 to 44 ± 5%     | °C/W         |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 LFPM<br>500 LFPM                             | TSSOP-8<br>TSSOP-8   | 185<br>140        | °C/W<br>°C/W |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | Standard Board                                 | TSSOP-8  | 41 to 44 ± 5%     | °C/W         |
| θ <sub>JA</sub>  | Thermal Resistance (Junction-to-Ambient)           | 0 lfpm<br>500 lfpm                             | DFN8<br>DFN8   | 129<br>84         | °C/W<br>°C/W |
| T <sub>sol</sub> | Wave Solder<br>Pb<br>Pb-Free                       | <2 to 3 sec @ 248°C<br><2 to 3 sec @ 260°C     |  | 265<br>265        | °C           |
| θ <sub>JC</sub>  | Thermal Resistance (Junction-to-Case)              | (Note 2)                                       | DFN8   | 35 to 40          | °C/W         |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

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**Table 4. LVPECL DC CHARACTERISTICS**  $V_{CC} = 3.3\text{ V}$ ;  $V_{EE} = 0.0\text{ V}$  (Note 3)

| Symbol      | Characteristic  | -40°C     |      |      | 25°C |      |      | 85°C |      |      | Unit          |
|-------------|---|-----------|------|------|------|------|------|------|------|------|---------------|
|             |   | Min       | Typ  | Max  | Min  | Typ  | Max  | Min  | Typ  | Max  |               |
| $I_{EE}$    | Power Supply Current  |           | 17   | 23   |      | 17   | 23   |      | 18   | 24   | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 4)  | 2215      | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 4)   | 1470      | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | 2135      |      | 2420 | 2135 |      | 2420 | 2135 |      | 2420 | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | 1490      |      | 1825 | 1490 |      | 1825 | 1490 |      | 1825 | mV            |
| $V_{BB}$    | Output Voltage Reference  | 1.92      |      | 2.04 | 1.92 |      | 2.04 | 1.92 |      | 2.04 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 5)<br>$V_{pp} < 500\text{ mV}$<br>$V_{pp} \geq 500\text{ mV}$ | 1.2       |      | 2.9  | 1.1  |      | 2.9  | 1.1  |      | 2.9  | V             |
|             |   | 1.5       |      | 2.9  | 1.4  |      | 2.9  | 1.4  |      | 2.9  | V             |
| $I_{IH}$    | Input HIGH Current  |           |      | 150  |      |      | 150  |      |      | 150  | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | D         | 0.5  |      | 0.5  |      |      | 0.5  |      |      | $\mu\text{A}$ |
|             |   | $\bar{D}$ | -600 |      | -600 |      |      | -600 |      |      | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

**Table 5. LVNECL DC CHARACTERISTICS**  $V_{CC} = 0.0\text{ V}$ ;  $V_{EE} = -3.3\text{ V}$  (Note 6)

| Symbol      | Characteristic  | -40°C     |       |       | 25°C  |       |       | 85°C  |       |       | Unit          |
|-------------|---|-----------|-------|-------|-------|-------|-------|-------|-------|-------|---------------|
|             |   | Min       | Typ   | Max   | Min   | Typ   | Max   | Min   | Typ   | Max   |               |
| $I_{EE}$    | Power Supply Current  |           | 17    | 23    |       | 17    | 23    |       | 18    | 24    | mA            |
| $V_{OH}$    | Output HIGH Voltage (Note 7)  | -1085     | -1005 | -880  | -1025 | -955  | -880  | -1025 | -955  | -880  | mV            |
| $V_{OL}$    | Output LOW Voltage (Note 7)   | -1830     | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV            |
| $V_{IH}$    | Input HIGH Voltage (Single-Ended)   | -1165     |       | -880  | -1165 |       | -880  | -1165 |       | -880  | mV            |
| $V_{IL}$    | Input LOW Voltage (Single-Ended)  | -1810     |       | -1475 | -1810 |       | -1475 | -1810 |       | -1475 | mV            |
| $V_{BB}$    | Output Voltage Reference  | -1.38     |       | -1.26 | -1.38 |       | -1.26 | -1.38 |       | -1.26 | V             |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 8)<br>$V_{pp} < 500\text{ mV}$<br>$V_{pp} \geq 500\text{ mV}$ | -2.1      |       | -0.4  | -2.2  |       | -0.4  | -2.2  |       | -0.4  | V             |
|             |   | -1.8      |       | -0.4  | -1.9  |       | -0.4  | -1.9  |       | -0.4  | V             |
| $I_{IH}$    | Input HIGH Current  |           |       | 150   |       |       | 150   |       |       | 150   | $\mu\text{A}$ |
| $I_{IL}$    | Input LOW Current   | D         | 0.5   |       | 0.5   |       |       | 0.5   |       |       | $\mu\text{A}$ |
|             |   | $\bar{D}$ | -600  |       | -600  |       |       | -600  |       |       | $\mu\text{A}$ |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .
- Outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ , max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and  $1\text{ V}$ .

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**Table 6. AC CHARACTERISTICS**  $V_{CC}= 3.3\text{ V}$ ;  $V_{EE}= 0.0\text{ V}$  or  $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -3.3\text{ V}$  (Note 9)

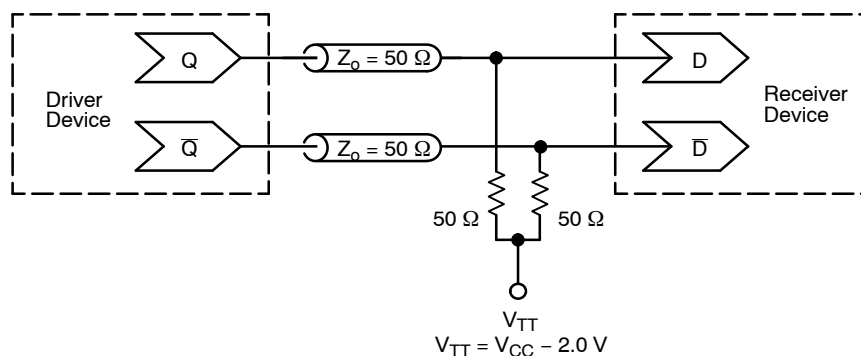
| Symbol                               | Characteristic  | -40°C      |            |            | 25°C       |            |            | 85°C       |            |            | Unit |
|--------------------------------------|---|------------|------------|------------|------------|------------|------------|------------|------------|------------|------|
|                                      |   | Min        | Typ        | Max        | Min        | Typ        | Max        | Min        | Typ        | Max        |      |
| $f_{\max}$                           | Maximum Toggle Frequency                                    |            | 1.75       |            |            | 1.75       |            |            | 1.75       |            | GHz  |
| $t_{\text{PLH}}$<br>$t_{\text{PHL}}$ | Propagation Delay to Output<br>Differential<br>Single-Ended | 150<br>100 | 275<br>275 | 400<br>450 | 225<br>175 | 300<br>300 | 375<br>425 | 240<br>190 | 315<br>315 | 390<br>440 | ps   |
| $t_{\text{SKEW}}$                    | Duty Cycle Skew (Differential) (Note 10)                    |            | 5          | 30         |            | 5          | 20         |            | 5          | 20         | ps   |
| $t_{\text{JITTER}}$                  | Random Clock Jitter (RMS)                                   |            | 0.7        |            |            | 0.7        |            |            | 0.7        |            | ps   |
| $V_{\text{PP}}$                      | Input Swing (Note 11)                                       | 150        |            | 1000       | 150        |            | 1000       | 150        |            | 1000       | mV   |
| $t_r$<br>$t_f$                       | Output Rise/Fall Times Q<br>(20% - 80%)                     | 120        | 220        | 320        | 120        | 220        | 320        | 120        | 220        | 320        | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9.  $V_{EE}$  can vary  $\pm 0.3\text{ V}$ .

10. Duty cycle skew is the difference between a  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  propagation delay through a device.

11.  $V_{\text{PP}(\text{min})}$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 2. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

# MC100LEVEL16

## ORDERING INFORMATION

| Device            | Package              | Shipping†          |
|-------------------|----------------------|--------------------|
| MC100LEVEL16D     | SO-8                 | 98 Units / Rail    |
| MC100LEVEL16DG    | SO-8<br>(Pb-Free)    | 98 Units / Rail    |
| MC100LEVEL16DR2   | SO-8                 | 2500 Tape & Reel   |
| MC100LEVEL16DR2G  | SO-8<br>(Pb-Free)    | 2500 Tape & Reel   |
| MC100LEVEL16DT    | TSSOP-8              | 100 Units / Rail   |
| MC100LEVEL16DTG   | TSSOP-8<br>(Pb-Free) | 100 Units / Rail   |
| MC100LEVEL16DTR2  | TSSOP-8              | 2500 Tape & Reel   |
| MC100LEVEL16DTR2G | TSSOP-8<br>(Pb-Free) | 2500 Tape & Reel   |
| MC100LEVEL16MNR4  | DFN8                 | 1000 / Tape & Reel |
| MC100LEVEL16MNR4G | DFN8<br>(Pb-Free)    | 1000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

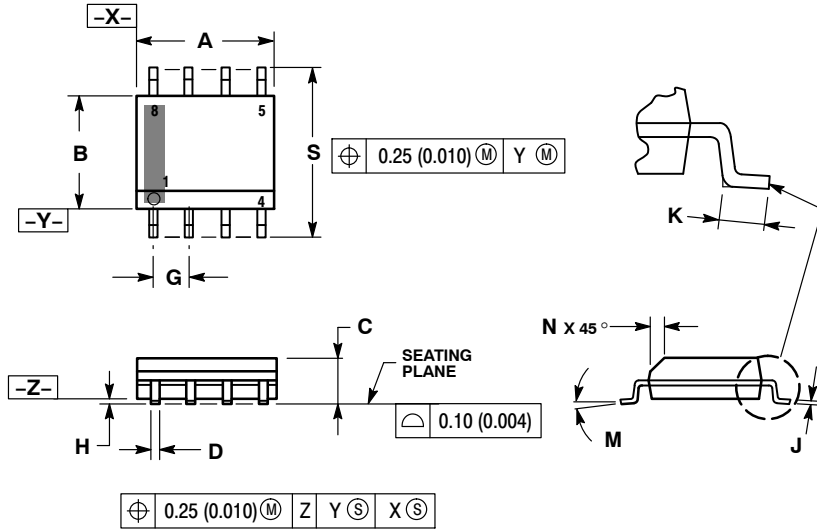
### Resource Reference of Application Notes

- AN1405/D** - ECL Clock Distribution Techniques
- AN1406/D** - Designing with PECL (ECL at +5.0 V)
- AN1503/D** - ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** - Metastability and the ECLinPS Family
- AN1568/D** - Interfacing Between LVDS and ECL
- AN1672/D** - The ECL Translator Guide
- AND8001/D** - Odd Number Counters Design
- AND8002/D** - Marking and Date Codes
- AND8020/D** - Termination of ECL Logic Devices
- AND8066/D** - Interfacing with ECLinPS
- AND8090/D** - AC Characteristics of ECL Devices

# MC100LEVEL16

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

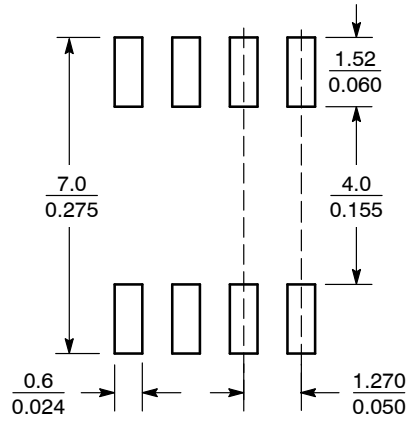


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.80        | 5.00 | 0.189     | 0.197 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.053     | 0.069 |
| D   | 0.33        | 0.51 | 0.013     | 0.020 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| H   | 0.10        | 0.25 | 0.004     | 0.010 |
| J   | 0.19        | 0.25 | 0.007     | 0.010 |
| K   | 0.40        | 1.27 | 0.016     | 0.050 |
| M   | 0 °         | 8 °  | 0 °       | 8 °   |
| N   | 0.25        | 0.50 | 0.010     | 0.020 |
| S   | 5.80        | 6.20 | 0.228     | 0.244 |

### SOLDERING FOOTPRINT\*



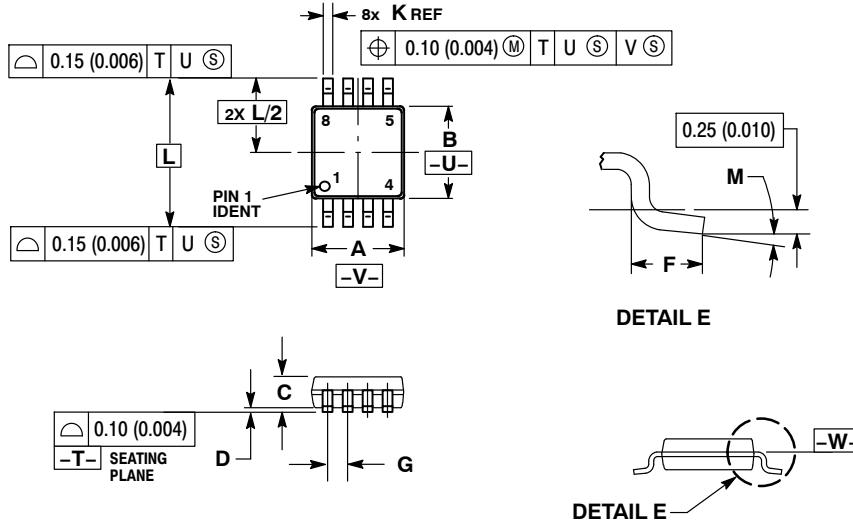
SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC100LVEL16

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

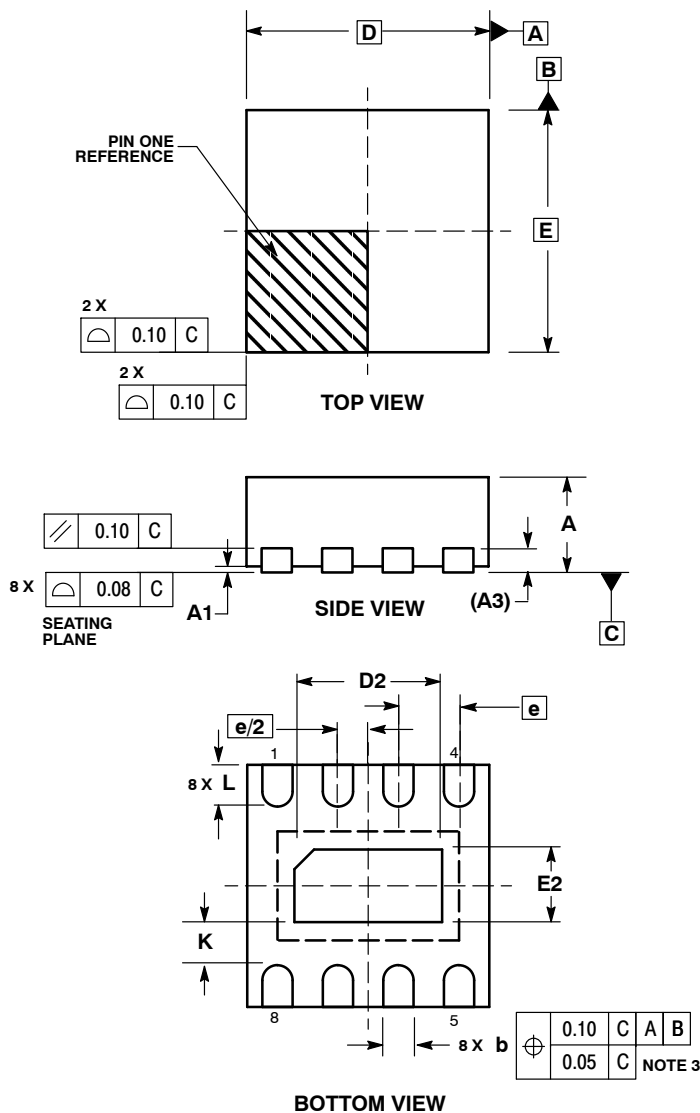
| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 2.90        | 3.10 | 0.114     | 0.122 |
| B   | 2.90        | 3.10 | 0.114     | 0.122 |
| C   | 0.80        | 1.10 | 0.031     | 0.043 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.40        | 0.70 | 0.016     | 0.028 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| K   | 0.25        | 0.40 | 0.010     | 0.016 |
| L   | 4.90 BSC    |      | 0.193 BSC |       |
| M   | 0°          | 6°   | 0°        | 6°    |



# MC100LEVEL16

## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| MILLIMETERS |          |      |
|-------------|----------|------|
| DIM         | MIN      | MAX  |
| A           | 0.80     | 1.00 |
| A1          | 0.00     | 0.05 |
| A3          | 0.20 REF |      |
| b           | 0.20     | 0.30 |
| D           | 2.00 BSC |      |
| D2          | 1.10     | 1.30 |
| E           | 2.00 BSC |      |
| E2          | 0.70     | 0.90 |
| e           | 0.50 BSC |      |
| K           | 0.20     | ---  |
| L           | 0.25     | 0.35 |

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Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

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- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
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- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

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