USBDFxxW5

EMI filter and line termination for USB downstream ports

Applications

EMI Filter and line termination for USB downstream ports on:

- Desktop computer
- Notebooks
- Workstations
- USB Hubs

Features

- Monolithic device with recommended line termination for USB downstream ports
- Integrated Rt series termination and Ct bypassing capacitors.
- Integrated ESD protection
- Small package size

Description

The USB specification requires USB downstream ports to be terminated with pull-down resistors from the D+ and D- lines to ground. On the implementation of USB systems, the radiated and conducted EMI should be kept within the required levels as stated by the FCC regulations. In addition to the requirements of termination and EMC compatibility, the computing devices are required to be tested for ESD susceptibility.

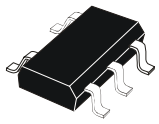
The USBDFxxW5 provides the recommended line termination while implementing a low pass filter to limit EMI levels and providing ESD protection which exceeds IEC 61000-4-2 level 4 standard. The device is packaged in a SOT323-5L, which is a very small (50% smaller than the standard SOT23).

Complies with the following standards

IEC 61000-4-2, level 4 ±15 kV (air discharge)

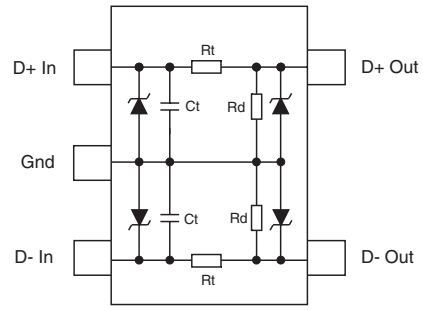
±8 kV (contact discharge)

MIL STD 883C, Method 3015-6
Class 3 C = 100 pF R = 1500 W
3 positive strikes and 3 negative strikes (F = 1 Hz)



SOT323-5L

Functional diagram



	R_t	R_d	C_t
USBDF01W5	33 Ω	15 kΩ	47 pF
USBDF02W5	15 Ω	15 kΩ	47 pF
Tolerance	±10%	±10%	±20%

Order codes

Part number	Marking
USBDF01W5	UD1
USBDF02W5	UD2

Benefits

- EMI / RFI noise suppression
- Required line termination for USB downstream ports
- ESD protection exceeding IEC61000-4-2 level 4
- IPAD™ technology provides high flexibility in the design of high density boards
- Tailored to meet USB 1.1 standard

TM: IPAD is a trademark of STMicroelectronics

1 Characteristics

Table 1. Absolute maximum ratings (T_{amb} = 25° C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD discharge IEC 61000-4-2, contact discharge ESD discharge - MIL STD 883 - Method 3015-6	±15 ±25	kV
T_j	Operating junction temperature range	-40 to 150	°C
T_{stg}	Storage temperature range	- 55 to +150	°C
T_L	Lead solder temperature (10 second duration)	260	°C
P_r	Power rating per resistor	100	mW

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameters	Test conditions	Min	Typ	Max	Unit
V_{BR}	Diode breakdown voltage	I_R = 1 mA	6			V
V_F	Diode forward voltage drop	I_F = 50 mA		0.9		V

2 Application information

Figure 1. USB Standard requirements

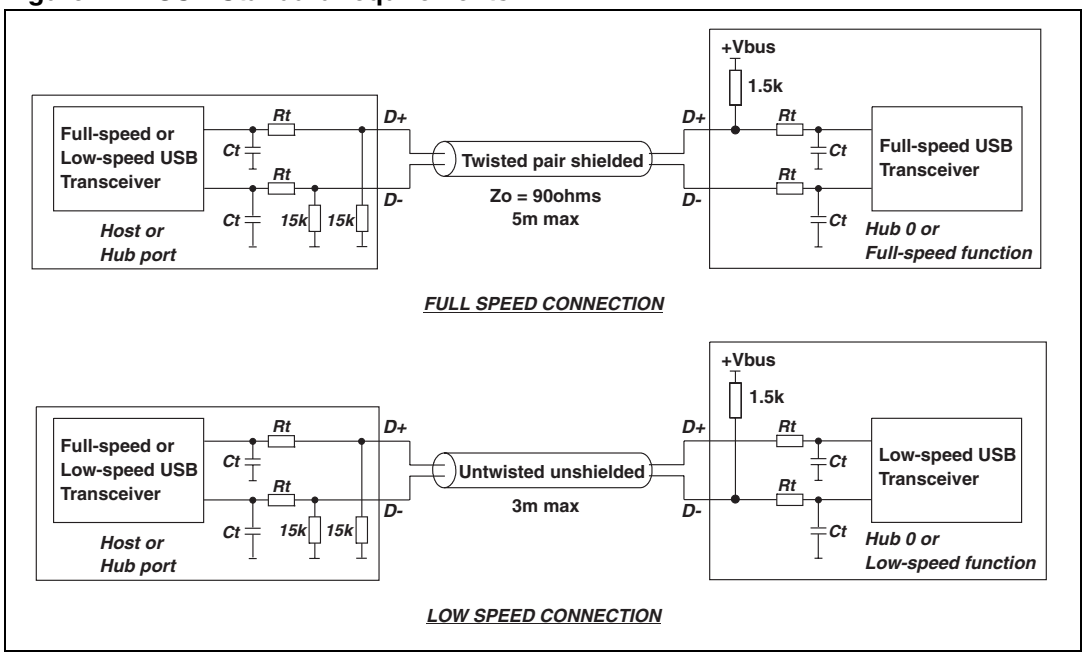
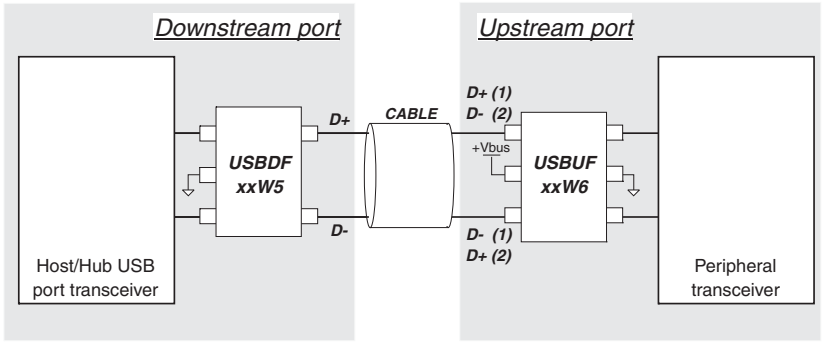


Figure 2. Application example



(1) for a low-speed port
(2) for a full-speed port

2.1 EMI filtering

Current FCC regulations requires that class B computing devices meet specified maximum levels for both radiated and conducted EMI.

- Radiated EMI covers the frequency range from 30 MHz to 1 GHz.
- Conducted EMI covers the 450 kHz to 30 MHz range.

For the types of devices utilizing the USB the most difficult test to pass is usually the radiated EMI test. For this reason the USBDF device aims to minimize radiated EMI.

The differential signal (D+ and D-) of the USB does not contribute significantly to radiated or conducted EMI because the magnetic field of the two conductors exactly cancels each other.

The inside of the PC environment is very noisy and designers must minimise noise coupling from the different sources. D+ and D- must not be routed near high speed lines (clocks...).

Induced common mode noise can be minimised by running pairs of USB signals parallel to each other and running grounded guard trace on each side of the signal pair from the USB controller to the USBDF device.

If possible, locate the USBDF device physically near the USB connectors. Distance between the USB controller and the USB connector must be minimized.

The 47 pF (C_t) capacitors are used to divert high frequency energy to ground and for edge control, and must be placed between the USB Controller and the series termination resistors (R_t). Both C_t and R_t should be placed as close to the mSB Controller as practicable.

The USBDFxxW5 ensure a filtering protection against electroMagnetic and radio-frequency Interference thanks to its low-pass filter structure. This filter is characterized by the following parameters :

- cut-off frequency
- Insertion loss
- high frequency rejection

Figure 4. shows the attenuation curve for frequencies up to 3 GHz.

Figure 3. Measurement configuration

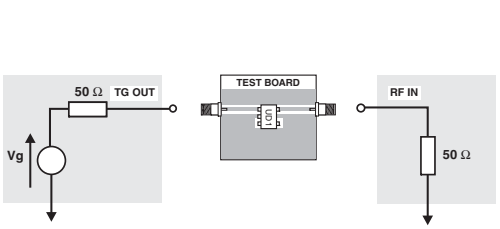
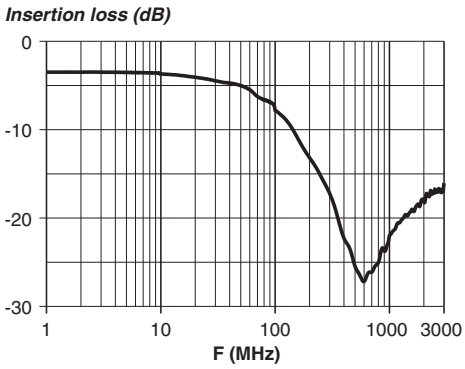


Figure 4. USBDFxxW5 attenuation curve



2.2 ESD protection

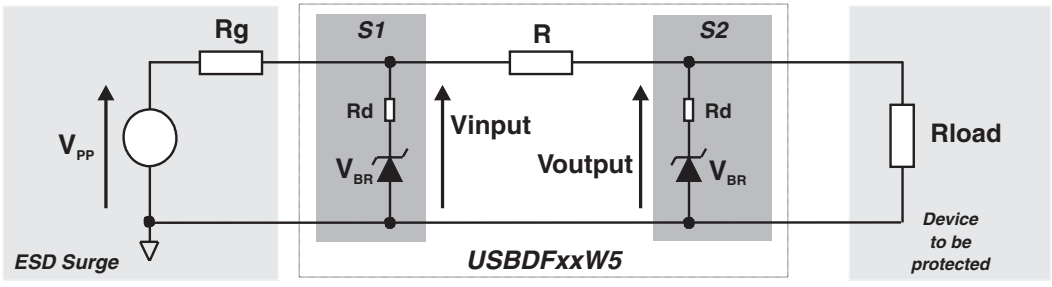
In addition to the requirements of termination and EMC compatibility, computing devices are required to be tested for ESD susceptibility. This test is described in the IEC 61000-4-2 and is already in place in Europe. This test requires that a device tolerates ESD events and remain operational without user intervention.

The USBDFxxW5 is particularly optimized to perform ESD protection. ESD protection is based on the use of device which clamps at :

$$V_{INPUT} = V_{BR} + R_d.I_{pp}$$

This protection function is split in 2 stages. As shown in *Figure 5.*, the ESD strikes are clamped by the first stage S1 and then the remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage very low at the V_{out} level.

Figure 5. USBDFxxW5 ESD clamping behavior



To have a good approximation of the remaining voltages at both V_{in} and V_{out} stages, we give the typical dynamical resistance value R_d. Taking into account the following hypothesis: $R_t > R_d$, $R_g > R$ and $R_{load} > R_d$, gives these formulas::

$$V_{input} = \frac{R_g.V_{BR} + R_d.V_g}{R_g}$$

$$V_{output} = \frac{R_t.V_{BR} + R_d.V_{input}}{R_t}$$

The results of the calculation done for V_{PP} = 8 kV, R_g = 330 W (IEC61000-4-2 standard), V_{BR} = 7 V (typ.) and R_d = 1 Ω (typ.) give:

V_{input} = 31.2 V

V_{output} = 7.95 V

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the V_{in} side. This parasitic effect is not present at the V_{out} side due the low current involved after the resistance R.

The measurements results shown below show very clearly (*Figure 7.*) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on Vout stage
- output clamping voltage very close to V_{BR} (positive strike) and $-V_F$ (negative strike)

Figure 6. Measurement board

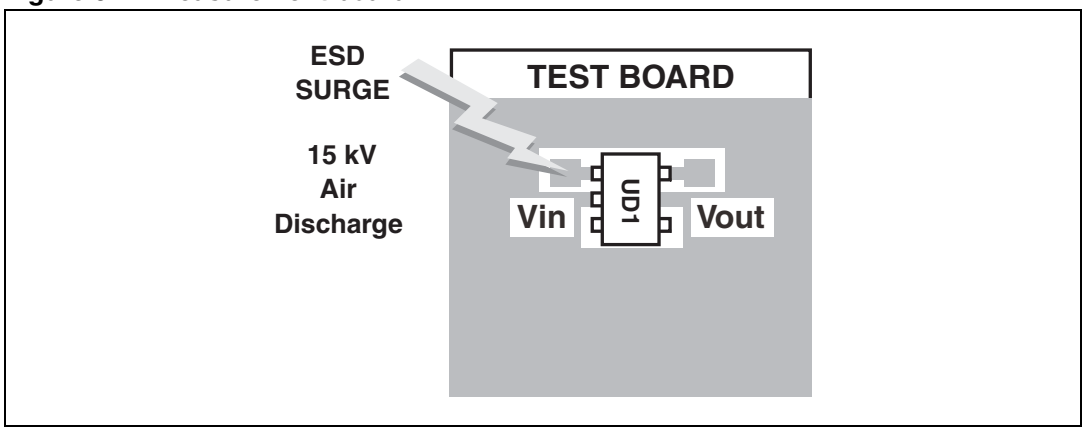
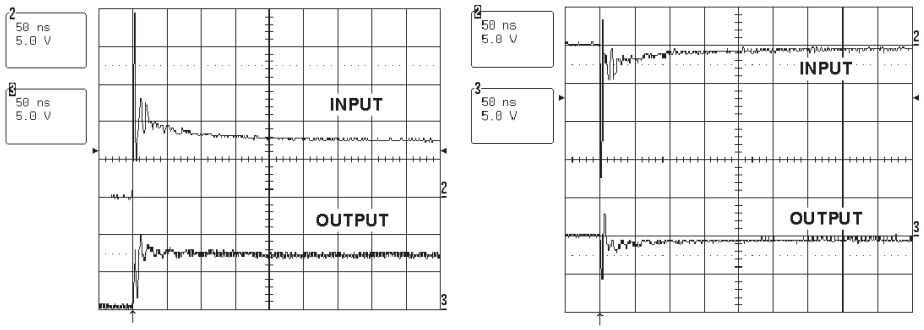


Figure 7. Remaining voltage at both stages S1 (V_{input}) and S2 (V_{output}) during ESD surge



A. Positive surge B. Negative surge

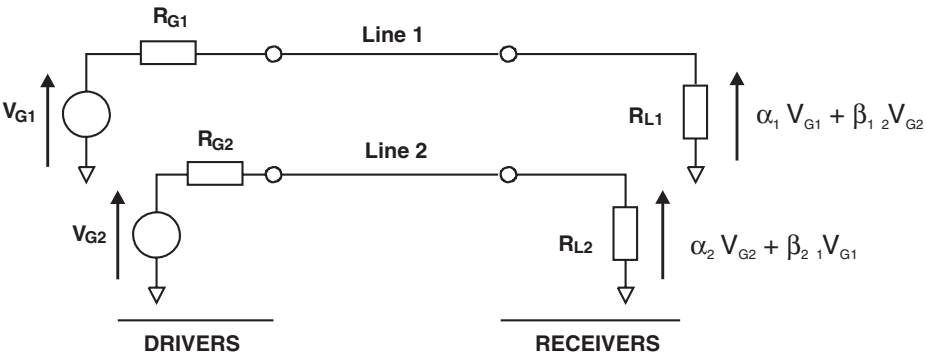
Note that the USBDFxxW5 is not only acting for positive ESD surges but also for negative ones. Negative disturbances are clamped close to ground voltage as shown in *Figure 7.b*.

2.3 Latch-up phenomena

The early ageing and destruction of IC's is often due to latch-up phenomena which is mainly induced by dV/dt. Thanks to its structure, the USBDFxxW5 provides a high immunity to latch-up phenomena by smoothing very fast edges.

2.4 Crosstalk behaviour

Figure 8. Crosstalk phenomena



The crosstalk phenomena is due to the coupling between 2 lines. The coupling factor (β12 or β21) increases when the gap across lines decreases, this is the reason why we provide crosstalk measurements for a monolithic device to guarantee negligeable crosstalk between the lines. In the example above, the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta 21 V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ).

Figure 9. Analog crosstalk measurements

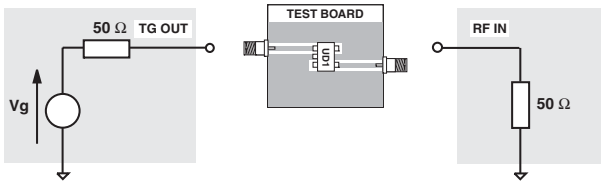


Figure 10. Typical analog crosstalk results

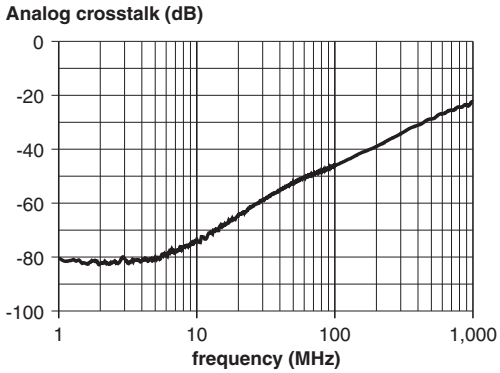


Figure 8. gives the measurement circuit for the analog crosstalk application. In *Figure 10.*, the curve shows the effect of the D+ cell on the D- cell. In usual frequency range of analog signals (up to 100 MHz) the effect on disturbed line is less than -46 dB.

Figure 11. Digital crosstalk measurements configuration

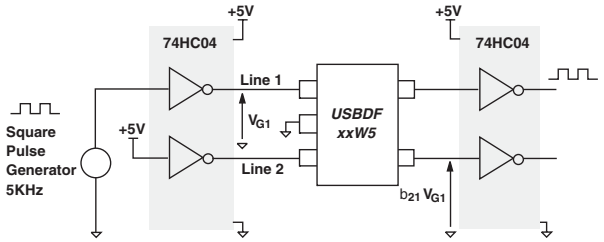


Figure 12. Digital crosstalk results

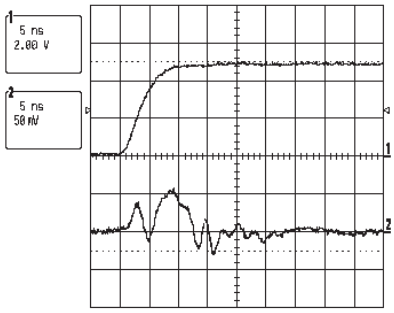


Figure 11. shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure 12. shows that in such a condition signal, from 0 to 5 V and rise time of few ns, the impact on the other line is less than 100 mV peak to peak (below the logic high voltage threshold). The measurements performed with falling edges give the same results.

2.5 Transition times

This low pass filter has been designed in order to meet the USB 1.1 standard requirements that implies the signal edges are maintained within the 4 ns-20 ns stipulated USB specification limits.

Figure 13. Typical rise and fall times: measurements configuration

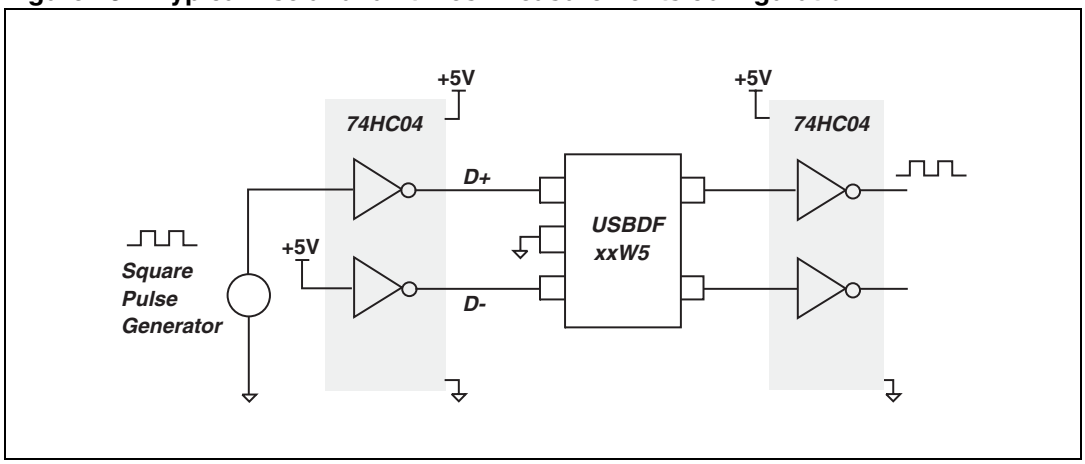
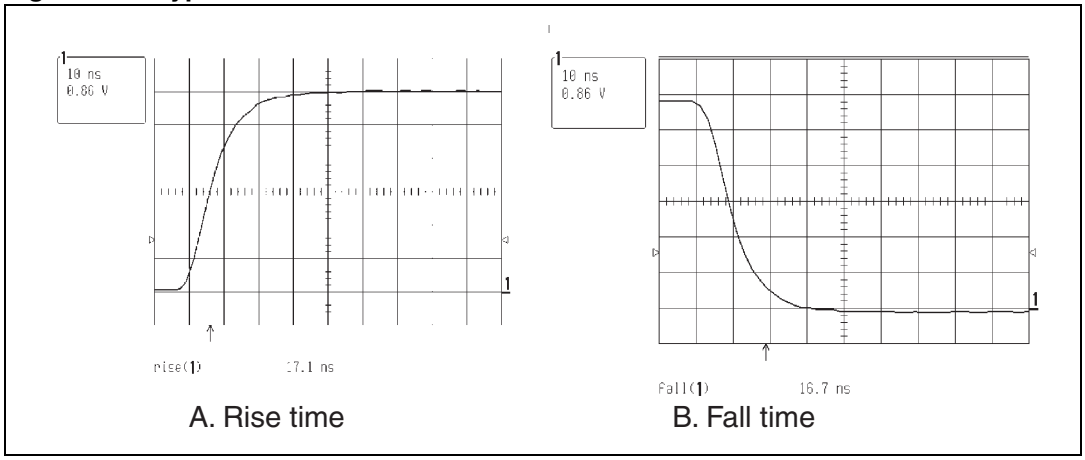


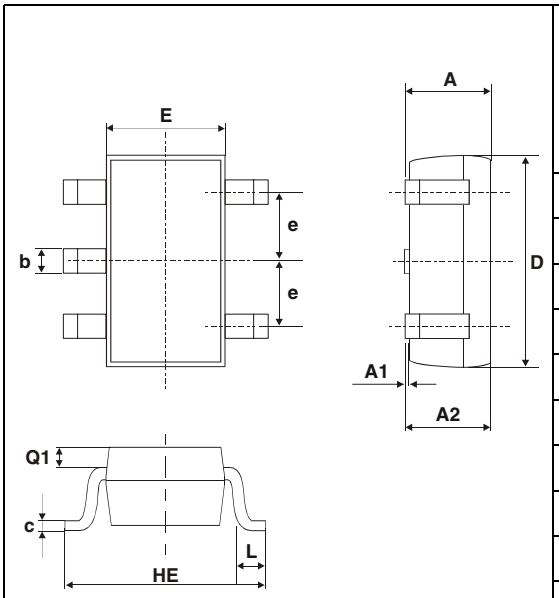
Figure 14. Typical rise and fall times



A. Rise time B. Fall time

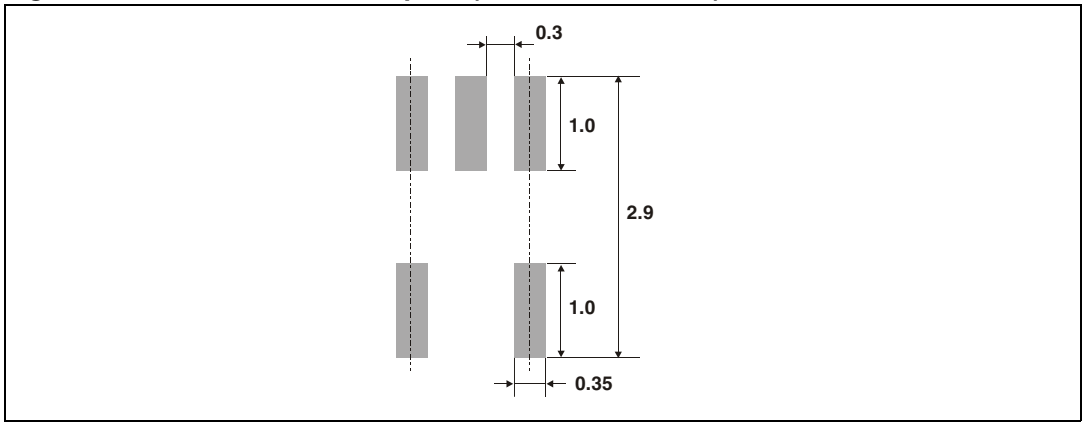
3 Package information

Table 3. SOT323-5L dimensions



Ref.	Dimensions			
	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.8	1.1	0.031	0.043
A1	0	0.1	0	0.004
A2	0.8	1	0.031	0.039
b	0.15	0.3	0.006	0.012
c	0.1	0.18	0.004	0.007
D	1.8	2.2	0.071	0.086
E	1.15	1.35	0.045	0.053
e	0.65 Typ.		0.025 Typ.	
H	1.8	2.4	0.071	0.094
Q1	0.1	0.4	0.004	0.016

Figure 15. Recommended footprint (dimensions in mm)



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Type	Order Code	Weight	Marking	Package	Base Qty
USBDF01W5	USBDF01W5	5.4 mg	UD1	SOT323-5L	3000
USBDF02W5	USBDF02W5		UD2		

5 Revision history

Date	Revision	Changes
May-2000	1C	Initial release.
7-Sep-2006	2	Reformatted to current standard. Modified Operating junction temperature range in Table 1.
15-Sep-2006	3	Corrected units of R_d to kΩ instead of Ω on page 1

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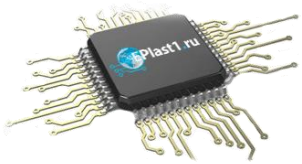

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