

## Analog Signal Input Class-D Amplifier with DC-DC Converter for Piezo Speaker

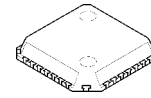
### ■ GENERAL DESCRIPTION

The **NJU8753** is an analog signal input monaural class D power amplifier with DC-DC converter for Piezo speaker. Input part operates on 2.85V(typ) and a built-in DC-DC converter generates variable output voltage(up to 12V) with input voltage(2.6 to 4.2V). Therefore, it drives Piezo speaker with louder sound and high efficiency.

The **NJU8753** incorporates BTL amplifier, which eliminate AC coupling capacitors, capable of driving Piezo speaker with simple external LC low-pass filters.

Class D operation achieves lower power operation for Piezo speaker, thus the **NJU8753** is suited for battery- powered applications.

### ■ PACKAGE OUTLINE

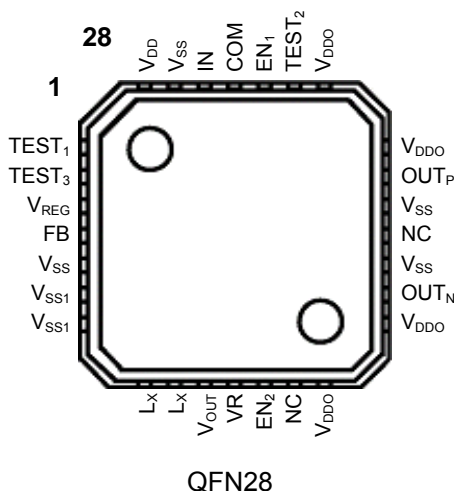


**NJU8753KN1**

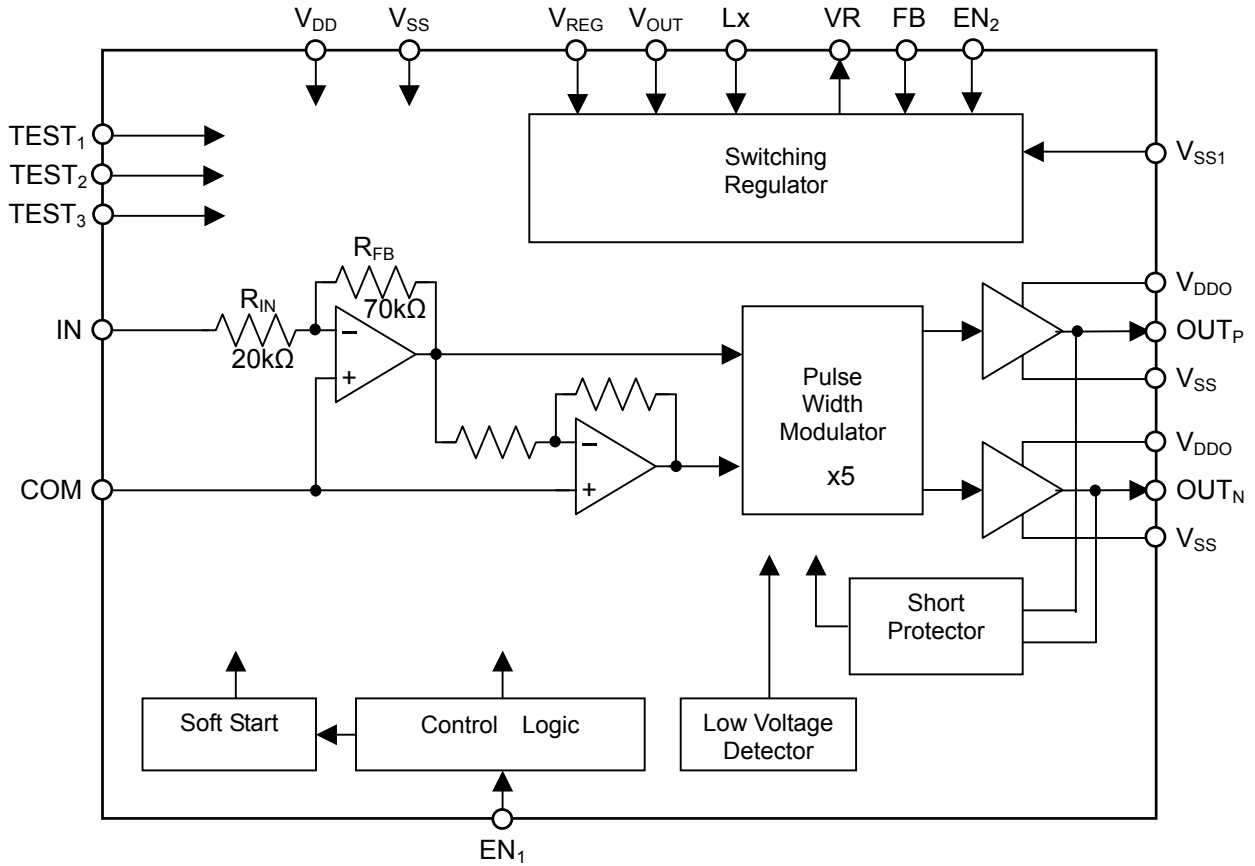
### ■ FEATURES

- Operating Voltage :2.6 to 3.6V( $V_{DD}$ ,  $V_{REG}$ )  
:2.6 to 4.2V( $V_{BAT}$ )
- Output voltage :8Vrms(Typ.) @ $V_{DDO}=10.0V$
- Piezo Speaker Driving
- 1-channel Analog Signal Input, 1-channel BTL output
- Standby(Hi-Z),
- Built-in DC-DC Converter
- Built-in Low Voltage Detector
- Built-in Short Protector
- CMOS Technology
- Package Outline :QFN28

### ■ TERMINAL CONFIGURATION



## ■ BLOCK DIAGRAM



## ■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	Function
1, 2, 23	TEST <sub>1</sub> TEST <sub>3</sub> TEST <sub>2</sub>	I	Maker test These terminals must be connected to GND.
3	V <sub>REG</sub>	–	Switching regulator Power Supply : V <sub>REG</sub> =2.85V
4	FB	I	Switching regulator Feedback resistor connection
5, 17, 19, 27	V <sub>SS</sub>	–	Power GND : V <sub>SS</sub> =0V
6,7	V <sub>SS1</sub>	–	Switching regulator Power GND: V <sub>SS1</sub> =0V
8,9	Lx	I	Switching regulator coil connection
10	V <sub>OUT</sub>	–	Switching regulator Power Supply : V <sub>OUT</sub> =10.0V
11	VR	O	Switching regulator step-up voltage setting resistor connection
12	EN <sub>2</sub>	I	Switching regulator Standby Control High : Step-up ON Low : Standby ON This terminal must be connected to V <sub>REG</sub> when step-up ON.
13, 18	NC	–	Non connection
14, 15, 21, 22	V <sub>DDO</sub>	–	Output Power supply
16	OUT <sub>N</sub>	O	Negative Output
20	OUT <sub>P</sub>	O	Positive Output
24	EN <sub>1</sub>	I	Power Amplifier Standby Control High : Standby OFF Low : Standby ON This terminal must be connected to V <sub>DD</sub> when Standby OFF.
25	COM	–	Analog common
26	IN	I	Audio Signal Input
28	V <sub>DD</sub>	–	Power Supply: V <sub>DD</sub> =2.85V

\* V<sub>SS</sub> terminals(pins 5 and 17 and 19 and 27), V<sub>SS1</sub> terminals(pins 6 and 7) should be connected at the nearest point to the IC.

\* V<sub>DDO</sub> terminals(pins 14 and 15 and 21 and 22) should be connected at the nearest point to the IC.

\* OUT<sub>P</sub> terminal(pin 20), OUT<sub>N</sub> terminal(pin 16) require Schottky barrier diodes. (Refer to the "TYPICAL APPLICATION CIRCUIT")

\* Lx terminals(pins 8 and 9) require caution to the extraneous noise including the ESD(electrical static discharge) because the ESD protection can't be designed as well as other terminals.  
Require extra caution when the input voltage (V<sub>BAT</sub>: Refer to the "TYPICAL APPLICATION CIRCUIT") to the Lx terminal is supplied directly from the external because the extraneous noise including the ESD appears easily.

## ■ FUNCTIONAL DESCRIPTION

### (1) Input signal

The amount of current passing through a capacitive load increases proportionately with frequency of audio signal. Input filters should be put in the input line to reduce load current at high frequency-band.

The 1st-order RC type HPF(High Pass Filter) and the 1st-order RC type LPF(Low Pass Filter) are composed of input filters.

$f_{CH1}$ (Cut-off frequency of HPF) and  $f_{CL1}$ (Cut-off frequency of LPF) are determined by input resistance( $R_{IN}$ ), resistor for LPF( $R_{LPF}$ ), capacitor for LPF( $C_{LPF}$ ) and AC coupling capacitor( $C_C$ ). ( $R_{LPF}$ ,  $C_{LPF}$ ,  $C_C$ : Refer to the "TYPICAL APPLICATION CIRCUIT")

When  $R_{IN}=20k\Omega$ ,  $R_{LPF}=2.4k\Omega$  and  $C_{LPF}=0.022\mu F$ ,  $C_C=2.2\mu F$ ,  $f_{CH1}$  and  $f_{CL1}$  are roughly calculated as following expressions.

$$f_{CH1} = \frac{1}{2\pi(R_{IN} + R_{LPF})C_C} = \frac{1}{2 \times 3.14 \times (20 \times 10^3 + 2.4 \times 10^3) \times 2.2 \times 10^{-6}} \cong 5[\text{Hz}]$$

$$f_{CL1} = \frac{1}{2\pi(R_{IN} // R_{LPF})C_{LPF}} = \frac{1}{2 \times 3.14 \times (20 \times 10^3 // 2.4 \times 10^3) \times 0.022 \times 10^{-6}} \cong 3[\text{kHz}]$$

When SBDs are added between  $OUT_P$  and  $V_{SS}$ ,  $OUT_N$  and  $V_{SS}$ , the  $f_{CL1}$ (Cut-off frequency of LPF) must be less than 7KHz. When SBDs are not added, the  $f_{CL1}$  must be less than 3KHz.

Input amplitude impressed to IN terminal of IC ( $V_{IC}$ ) must be less than  $V_{DD}$ [Vpp].

When  $V_{DD}=2.85V$ ,  $R_{LPF}=2.4k\Omega$ , Audio signal maximum input level  $V_{INMAX}$  for considering as  $V_{IC} \leq V_{DD}$  [Vpp]  $V_{INMAX}$  are roughly calculated as following expressions.

$$V_{INMAX} = \frac{(R_{LPF} + R_{IN}) \times V_{IC}}{R_{IN}} = \frac{(2.4 \times 10^3 + 20 \times 10^3) \times 2.85}{20 \times 10^3} \cong 3.1[\text{Vpp}]$$

### (2) Output signal

The  $OUT_P$  and  $OUT_N$  generate PWM output signals, which will be converted to analog signal via external 2nd-order or higher LC filter.

LC type LPF is composed of the coil (L) and Piezo Speaker ( $C_L$ ).

The dump resistance ( $R_{DAMP}$ ) is connected between the  $OUT_N$  terminal and the coil between the  $OUT_P$  terminal and the coil to reduce the cut off frequency (fc) of LPF consumption electric current neighborhood signal input.

Set it up so that the value of L,  $C_L$  and  $R_{DAMP}$  may become Gain(Q) <1 of LPF in fc. (L,  $C_L$ ,  $C_{OUT}$ ,  $R_{DAMP}$ : Refer to the "TYPICAL APPLICATION CIRCUIT")

When  $L=47\mu H$ ,  $C_L=2.0\mu F$ ,  $C_{OUT}=0.1\mu F$ ,  $R_{DAMP}=4.7\Omega$ ,  $R_{DCR}=0.2\Omega$ , LPF( $f_c$ ) and Q are roughly calculated as following expressions.

$$f_c = \frac{1}{2\pi\sqrt{L(2C_L + C_{OUT})}} = \frac{1}{2 \times 3.14 \times \sqrt{47 \times 10^{-6} \times (2 \times 2.0 \times 10^{-6} + 0.1 \times 10^{-6})}} \cong 11[\text{kHz}]$$

$$Q = \frac{1}{(R_{DAMP} + R_{DCR})\sqrt{(2C_L + C_{OUT})}} = \frac{1}{(4.7 + 0.2)} \times \sqrt{\frac{47 \times 10^{-6}}{(2 \times 2.0 \times 10^{-6} + 0.1 \times 10^{-6})}} \cong 0.7$$

### (3) Power Amplifier Standby

By setting the  $EN_1$  terminal to "L", the standby mode is enabled. In the standby mode, the entire functions of the NJU8753 enter a low-power state, and the output terminals ( $OUT_P$  and  $OUT_N$ ) are high impedance.

### (4) Low Voltage Detector

When the power supply voltage drops down to below  $V_{DD}(\text{MIN})$ , the internal oscillation is halted for prevention to generate unwanted frequency, and the output terminals ( $OUT_P$ ,  $OUT_N$ ) become in high impedance.

## (5) Step-up switching regulator

The switching regulator is used as power supply( $V_{DDO}$ ) for power amplifier of class-D. The PFM controlled switching regulator works with external components, which are coil, capacitor, Schottky barrier diode and step-up voltage setting resistance.

By setting the EN<sub>2</sub> terminal to "H", the step-up operation is enabled, and in case of "L", standby mode is enabled.

Step-up voltage is set by internal reference voltage( $V_{REG} / 2$ ) and external resistors.

The step-up voltage can be calculated by the following methods:

<Calculation of the step-up voltage>

The step-up voltage is determined by internal reference voltage( $V_{REF}$ ),  $R_1$  and  $R_2$ . (See Figure.2)

example:  $V_{DD}=2.85V$ , Internal reference voltage( $V_{REF} = V_{REG} / 2=1.425[V]$ ,  $R_1=2M\Omega$ ,  $R_2=330k\Omega$ "

Step-up voltage[V] =  $V_{REF} \times ((R_1+R_2)/R_2) = 1.425 \times ((2M + 330k)/330k) = 10.06[V]$  "

Note)

- \*1 Apply  $V_{REG}$  first, next  $V_{BAT}$ . Otherwise, the voltage stress may cause a permanent damage to the IC.
- \*2 The kickback voltage by the step-up voltage operation varies with the fixed number of the external components and the PCB patterns. Output power supply( $V_{DDO}$ ) must not exceed the absolute maximum rating.

## (6) Short Circuit Protection

The short protector, which protects the **NJU8753** against high short-circuit current, turns off the output driver. After about 5 seconds from the protection, the **NJU8753** returns to normal operation. The short protector functions at the following accidents.

- Short between OUT<sub>P</sub> and OUT<sub>N</sub>
- Short between OUT<sub>P</sub> and  $V_{SS}$
- Short between OUT<sub>N</sub> and  $V_{SS}$

Note)

- \*1 The detectable current and the period for the protection depend on the power supply voltage, chip temperature and ambient temperature.
- \*2 The short protector is not effective for a long term short-circuit current but for an instantaneous accident. Continuous high-current may cause permanent damage to the **NJU8753**.

## ■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT	Note
Supply Voltage	$V_{DD}$		-0.3 to +4.0	V	
	$V_{REG}$		-0.3 to +4.0	V	
	$V_{DDO}$	With SBDs	-0.3 to +14.0	V	6
Without SBDs		-0.3 to +9.5			
$L_X$ Input Voltage	$V_{LX}$	With SBDs	-0.3 to +14.0	V	6
		Without SBDs.	-0.3 to +9.5		
FB Input Voltage	$V_{FB}$		-0.3 to +4.0	V	
Input Voltage	$V_{in}$		-0.3 to $V_{DD}+0.3$	V	
Operating Temperature	$T_{opr}$		-40 to +85	°C	
Storage Temperature	$T_{stg}$		-40 to +125	°C	
Power Dissipation	$P_D$		640 *	mW	

\* : Mounted on two-layer board of based on the JEDEC.

Note 1) All voltage are relative to "VSS= 0V" reference.

Note 2) The LSI must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.

## ■ ELECTRICAL CHARACTERISTIC

(Ta=25°C, V<sub>DD</sub>=V<sub>REG</sub>=2.85V, V<sub>BAT</sub>=3.7V, V<sub>DDO</sub>=10V, V<sub>SS</sub>=V<sub>SS1</sub>=0V,  
 TEST<sub>1</sub>=TEST<sub>2</sub>=TEST<sub>3</sub>=0V, EN<sub>1</sub>=EN<sub>2</sub>=2.85V,  
 Input Signal=1kHz, Input Signal Level=150mVrms, Frequency Band=20Hz to 20kHz,  
 Load Impedance=2.0μF, 2nd-order 11kHz LC Filter(Q=0.7),  
 When the SBDs are connected between OUT<sub>P</sub> and V<sub>SS</sub>, OUT<sub>N</sub> and V<sub>SS</sub>.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
V <sub>DD</sub> Supply Voltage	V <sub>DD</sub>		2.6	2.85	3.6	V	
V <sub>REG</sub> Supply Voltage	V <sub>REG</sub>		2.6	2.85	3.6	V	
V <sub>BAT</sub> Input Voltage	V <sub>BAT</sub>		2.6	3.7	4.2	V	
V <sub>DDO</sub> Supply Voltage	V <sub>DDO</sub>	With SBDs	6.5	10.0	12.0	V	6
		Without SBDs.	6.5	7.5	8.5		
Input Impedance	Z <sub>IN</sub>	IN terminal	-	20	-	KΩ	
Voltage Gain	A <sub>V</sub>		-	31	-	dB	
THD+N	THD	Input Signal Level =200mVrms	-	0.05	0.08	%	4
Maximum Output	V <sub>o</sub>	Output THD+N=10%	-	8.0	-	Vrms	
S/N	SN	A weight	-	80	-	dB	4
Operating Current(Standby)	I <sub>ST</sub>	EN <sub>1</sub> =EN <sub>2</sub> =0V	-	-	1	μA	
Operating Current (No signal input)	I <sub>SS</sub>	No-load operating No Signal Input	-	10	15	mA	
Input Voltage	V <sub>IH</sub>	EN <sub>1</sub> , EN <sub>2</sub> terminals	0.7V <sub>DD</sub>	-	V <sub>DD</sub>	V	
	V <sub>IL</sub>	EN <sub>1</sub> , EN <sub>2</sub> terminals	0	-	0.3V <sub>DD</sub>	V	
Input Leakage Current	I <sub>LK</sub>	EN <sub>1</sub> , EN <sub>2</sub> terminals	-	-	±1.0	μA	
Switching regulator Oscillating Frequency	f <sub>OSC</sub>		220	300	380	kHz	
Switching regulator Maximum Load Current	I <sub>OUT</sub>	Step-up Voltage =10.0V V <sub>OUT</sub> = 10.0V X 95%	50	-	-	mA	
Switching regulator Load Stability	ΔV <sub>OUT</sub>	Step-up Voltage =10.0V I <sub>OUT</sub> =10mA to 50mA	-	100	-	mV	

\*The LSI must be used within the “Absolute maximum ratings”. Otherwise, a stress may cause permanent damage to the LSI.

Note 3) Test system of the THD+N and S/N

The THD+N and S/N are tested in the system shown in Figure 1, where a 2nd-order LC LPF and another filter incorporated in an audio analyzer are used.

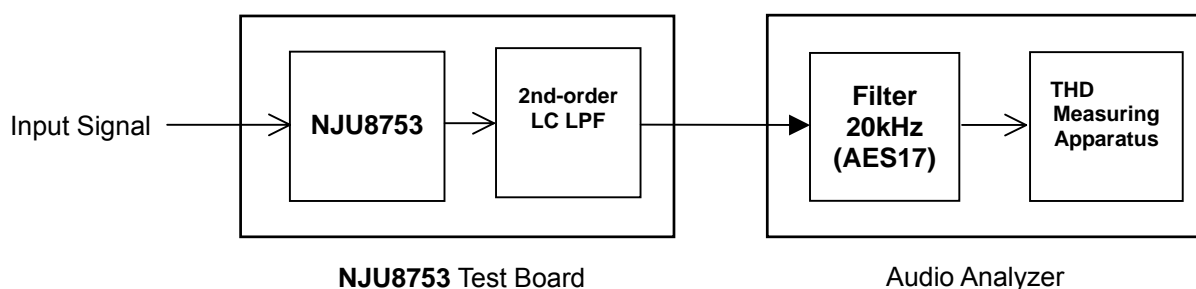


Figure 1. Output THD+N and S/N Test System

2nd-order LC LPF : Refer to “Typical Application Circuit”  
 Filters : 22Hz HPF + 20kHz LPF(AES17)  
 (with the A-Weight filter for S/N test)

## ■ TYPICAL APPLICATION CIRCUIT

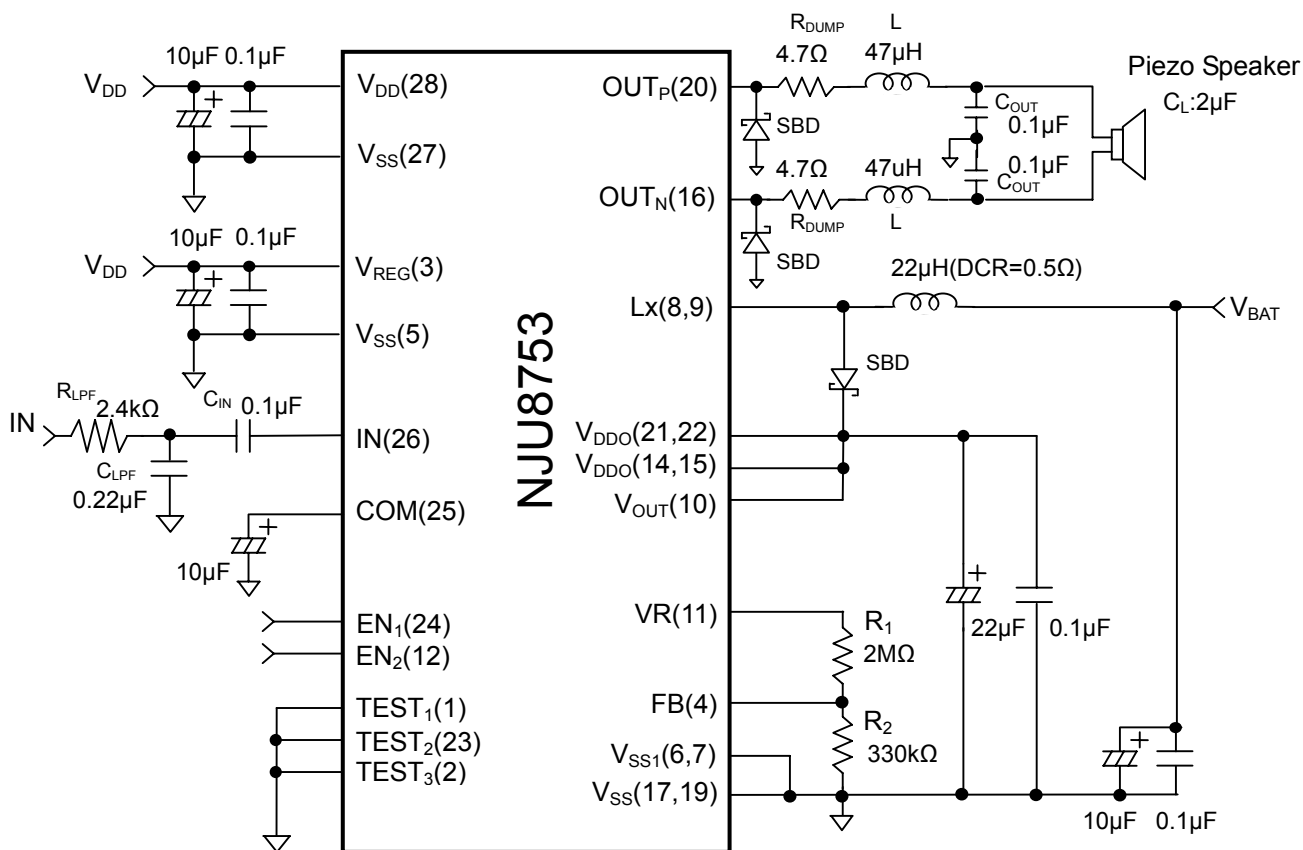


Figure 2. Application Circuit example

Note 4) De-coupling capacitors must be connected between each power supply terminal and GND.

Note 5) The LC filter and the schottky barrier diodes should be laid out nearest to the IC.  
 OUT<sub>P</sub> terminal(pin 20), OUT<sub>N</sub> terminal(pin 16) require schottky barrier diodes for terminal protection.  
 When SBDs is not used, the V<sub>DDO</sub> supply voltage maximum is 8.5V. (SBD: When T<sub>j</sub>=125°C, I<sub>R</sub>=less than 10mA at reverse voltage 12V\*<sup>1</sup>. When T<sub>j</sub>=25°C, Forward voltage (V<sub>F</sub>)=0.45V, Forward current (I<sub>F</sub>)=more than 1A at more than 12V)  
 \*1 Absolute maximum ratings is more than 20V.

Note 6) The LSI must be used inside of the following ratings. Otherwise, a stress may cause permanent damage to the regulator.

	SBDs are added	No SBDs
V <sub>DDO</sub> (Supply Voltage)	MAX=12V	MAX=8.5V
Input cut-off frequency	MAX=7kHz	MAX=3kHz
Output cut-off frequency	MAX=15kHz	
Q (The gain of LPF at f <sub>c</sub> )	MAX=1	
Piezo Speaker	MAX=2.2μF	
The capacitor between V <sub>DDO</sub> and V <sub>SS</sub>	MAX=22μF	
The coil for Lx terminal	MIN=22μH	
Input voltage	MAX=V <sub>DD</sub> [V <sub>pp</sub> ]	

Note 7) The transition time for EN<sub>1</sub> and EN<sub>2</sub> signals must be less than 100μs. Otherwise, a malfunction may be occurred.



- Note 8) Apply  $V_{REG}$  first, next  $V_{BAT}$ . Otherwise, the voltage stress may cause a permanent damage to the IC.  
The  $V_{DDO}$  is not able to accept from external power supply. Therefore use the DC-DC converter of the NJU8753.
- Note 9) The Lx terminals require caution to the extraneous noise including the ESD(electrical static discharge) because the ESD protection can't be designed as well as other terminals.  
Require extra caution when the input voltage ( $V_{BAT}$ ) to the Lx terminal is supplied directly from the external because the extraneous noise including the ESD appears easily.
- Note 10) The kickback voltage by the step-up voltage operation varies with the fixed number of the external components and the PCB patterns. Output power supply( $V_{DDO}$ ) must not exceed the absolute maximum rating.
- Note 11) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please test the circuit carefully to fit your application.  
The cut off frequency of the LC filter influences the quality of sound.  
The Q factor of the LC filter must be less than "1". Otherwise, the operating current increase when the frequency of input signal is closed to the cut off frequency.

[CAUTION]

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