



SY75576L

267MHz 1:4 3.3V HCSL/LVDS Fanout Buffer

PrecisionEdge™

General Description

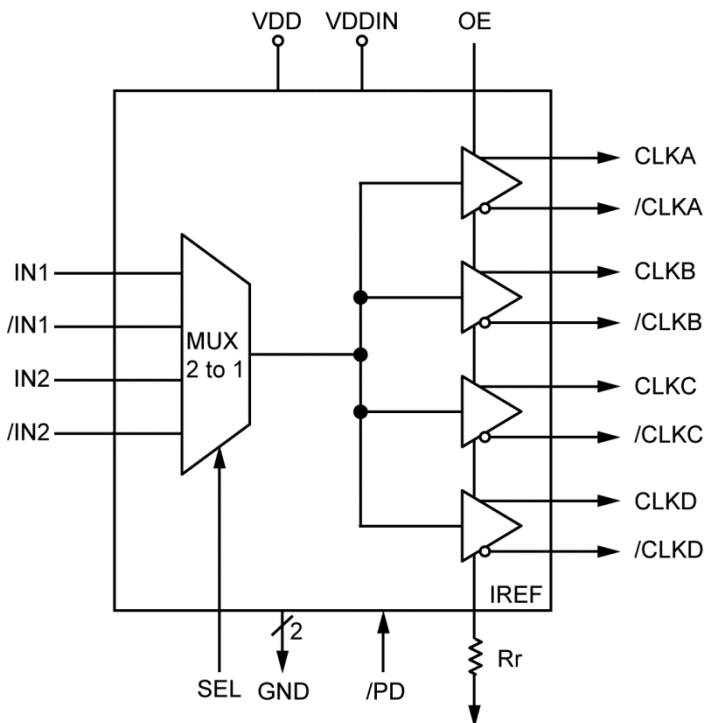
The SY75576L is a high-speed, fully differential 1:4 clock fanout buffer optimized to provide four identical output copies with 137fs phase jitter and maximum 50ps output-to-output skew. Designed to be used with PCI-Express applications, SY75576L accepts and outputs HCSL or LVDS logic levels.

The SY75576L operates from a 3.3V $\pm 5\%$ power supply and is guaranteed over the full industrial temperature range (-40°C to $+85^{\circ}\text{C}$). It is available in a 20-pin TSSOP lead-free package.

The SY75576L is part of Micrel's high-speed, ultra-low jitter, PrecisionEdge™ product line.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Features

- Four differential pairs of LVDS or HCSL outputs
- Two pairs of differential inputs accept LVDS or HCSL logic levels
- 267MHz max HCSL frequency
- 100MHz max LVDS frequency
- Ultra low phase jitter:
 - 137fs_{rms}, 200MHz (12kHz–20MHz)
 - 153fs_{rms}, 156.25MHz (12kHz–20MHz)
 - 212fs_{rms}, 100MHz (12kHz–20MHz)
- <2ps Total_Jitter_{pk-pk}, 200MHz (BER = 10^{-12})
- 50ps output-to-output skew
- 3.3V $\pm 5\%$ power supply operation
- -40°C to $+85^{\circ}\text{C}$ operating temperature
- Available in 20-pin TSSOP lead-free package

Applications

- Clock distribution
- PCI-Express
- Servers
- Switches
- Routers

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Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax +1 (408) 474-1000 • <http://www.micrel.com>

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hbwhelp@micrel.com or (408) 955-1690

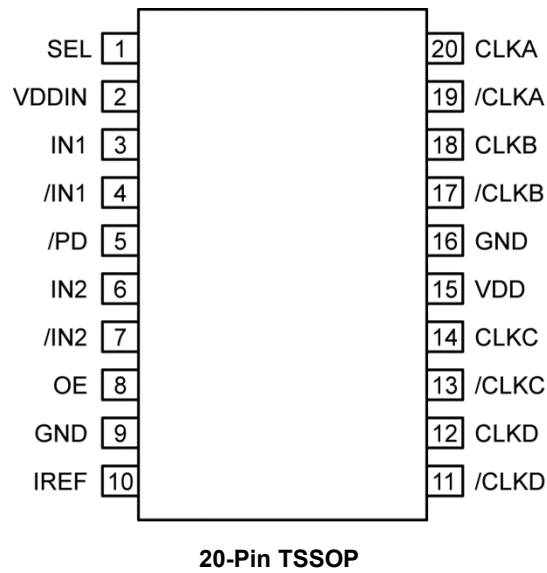
Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|------------------------------|--------------|-----------------|---|-------------|
| SY75576LKY | TSSOP-20 | Industrial | 75576L with Pb-Free bar-line indicator | Matte-Sn |
| SY75576LKY TR ⁽²⁾ | TSSOP-20 | Industrial | 75576L with Pb-Free bar-line indicator | Matte-Sn |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|----------|--|
| 1 | SEL | SEL = 0 propagates IN2, /IN2 to outputs. SEL = 1 propagates IN1, /IN1 to outputs. Internal pull-up resistor, IN1, /IN1 is selected by default. |
| 2 | VDDIN | 3.3V power supply |
| 3 | IN1 | HCSSL/LVDS input 1 |
| 4 | /IN1 | HCSSL/LVDS inverted input 1 |
| 5 | /PD | PD = 0 powers down the chip and tri-states outputs. The pin is attached to an internal pull-up resistor. |
| 6 | IN2 | HCSSL/LVDS input 2 |
| 7 | /IN2 | HCSSL/LVDS inverted input 2 |
| 8 | OE | Tri-state outputs. High = enable outputs. Low = disable outputs. Internal pull-up resistor, outputs are enabled by default. |
| 9 | GND | Ground |
| 10 | IREF | External resistor Rref between pin IREF and GND controls reference current |
| 11 | /CLKD | Inverted output D |
| 12 | CLKD | Non-inverted output D |
| 13 | /CLKC | Inverted output C |
| 14 | CLKC | Non-inverted output C |
| 15 | VDD | 3.3V power supply |
| 16 | GND | Ground |
| 17 | /CLKB | Inverted output B |
| 18 | CLKB | Non-inverted output B |
| 19 | /CLKA | Inverted output A |
| 20 | CLKA | Non-inverted output A |

Clock Input Function Table

| SEL | Input Pair |
|-----|-------------------------------|
| 0 | IN2 / $\overline{\text{IN2}}$ |
| 1 | IN1 / $\overline{\text{IN1}}$ |

Absolute Maximum Ratings⁽³⁾

| | |
|---------------------------------------|----------------------------|
| Supply Voltage (V_{DD}, V_{DDIN}) | 5.5V |
| Input Voltage (V_{IN}) | -0.5V to $V_{DDIN} + 0.5V$ |
| Lead Temperature (soldering, 20s) | 260°C |
| Maximum Junction Temperature | 125°C |
| Storage Temperature (T_s) | -65°C to +150°C |
| ESD Protection (input) | 2000V min. |

Operating Ratings⁽⁴⁾

| | |
|---|------------------|
| Supply Voltage (V_{DD}, V_{DDIN}) | 3.135V to 3.465V |
| Ambient Op Temperature (T_A) | -40°C to +85°C |
| Package Thermal Resistance ⁽⁵⁾ | |
| TSSOP | |
| Still-air (θ_{JA}) | 93°C/W |
| Junction-to-Case (θ_{JC}) | 20°C/W |

DC Electrical Characteristics⁽⁶⁾

$V_{DD} = V_{DDIN} = 3.135V$ to $3.465V$, $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. $R_{ref} = 475\Omega$

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------------------------|---|--------------------------|-------|------|------------------|------------|
| V_{DD}, V_{DDIN} | Power Supply Voltage Range | | 3.135 | 3.3 | 3.465 | V |
| C_{IN} | Input Capacitance | | | | 7 | pF |
| C_{out} | Output Capacitance | | | | 6 | pF |
| L_{Pin} | Pin Inductance | | | | 5 | nH |
| R_{out} | Output Resistance | | 3 | | | k Ω |
| $R_{pull\ up}$ | Pull up Resistance | SEL, /PD, OE | | 110 | | k Ω |
| V_{IH} | Input High Voltage | SEL, /PD, OE | 2 | | $V_{DDIN} + 0.3$ | V |
| V_{IL} | Input Low Voltage | SEL, /PD, OE | -0.3 | | 0.8 | V |
| V_{IH} | Input High Voltage | HCSL, IN, /IN | 660 | 750 | 850 | V |
| V_{IL} | Input Low Voltage | HCSL, IN, /IN | -150 | 0 | | V |
| V_{IN} | Differential Input Voltage Range | LVDS, IN, /IN | 250 | 350 | 550 | mV |
| $V_{input\ offset}$ | Input Common Mode Voltage | LVDS, IN, /IN, | 1.125 | 1.25 | 1.375 | V |
| V_{OH} | Output High Voltage | HSCL | 660 | 750 | 850 | mV |
| V_{OL} | Output Low Voltage | HSCL | -150 | 0 | 27 | mV |
| $V_{cross}^{(7, 8)}$ | Crossing Point Voltage | Absolute | 250 | 350 | 550 | mV |
| $V_{cross_variation}^{(7, 8, 9)}$ | Variation of Crossing Point Voltage | Variation over all edges | | | 140 | mV |
| I_{DD} | Power Supply Current For $V_{DD} + V_{DDIN}$ | 50 Ω , 2pF | | 75 | 90 | mA |
| | | No load, /PD = Low | | | 0.4 | mA |
| | | OE = Logic Low | | | 20 | mA |
| $I_{IL}^{(10)}$ | Input Leakage Current | $0 < V_{IN} < V_{DDIN}$ | -5 | | 5 | μA |

Notes:

- Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this datasheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
- The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
- Package thermal resistance assumes that the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air unless otherwise stated. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Test setup is $R_L = 50\Omega$ with 2pF, $R_r = 475\Omega \pm 1\%$.
- Measurement taken from Q and /Q.
- Measured at the crossing point where instantaneous voltages of CLK and /CLK are equal.
- Inputs with pull-up/pull-down resistances are not included.

AC Electrical Characteristics⁽⁶⁾

$V_{DD} = V_{DDIN} = 3.135V$ to $3.465V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------------|---|---|------|------|------|-------------------|
| f_{MAX} | Maximum Frequency | HCSL Termination | | | 267 | MHz |
| | | LVDS Termination | | | 100 | MHz |
| t_{PD} | Propagation Delay | Note 11 | | 2 | | ns |
| t_{Skew} | Output-to-Output skew | Notes 12, 13 | | | 50 | ps |
| t_R, t_F | Output Rise/Fall Times 0.175V to 0.525V / 0.525V to 0.175V | At full output swing. 50Ω, 2pF | 175 | 338 | 700 | ps |
| t_{R/F_var} | Rise/Fall Time Variation | At full output swing. 50Ω, 2pF | | | 125 | ps |
| T_{RJ_jitter} | Phase Jitter | At 200MHz | | 137 | | fs _{rms} |
| | | At 156.25MHz | | 153 | | fs _{rms} |
| | | At 100MHz | | 212 | | fs _{rms} |
| T_{TJ_jitter} | Total Jitter | BER = 10^{-12} , $T_{DJ} = 0$, at 200MHz | | 2 | | ps |
| T_{OE_enable} | Output Enable Time | All Outputs | | 2 | | μs |
| $T_{OE_disable}$ | Output Disable Time | All Outputs | | 10 | | ns |
| T_{DCY} | Duty Cycle | | 45 | 50 | 55 | % |

Notes:

- Measured from the differential input crossing point to the differential output crossing point.
- Output-to-Output skew is the difference in time between outputs, receiving data from the same input, for the same temperature, voltage, and transition.
- This parameter is defined in accordance with JEDEC Standard 65.

Jitter Analysis

Jitter is defined as the deviation of a signal from its ideal position. Phase noise is the presence of signal energy at frequencies other than the carrier. Random jitter has a Gaussian distribution and is specified as an rms unit, which is one standard deviation of the distribution. Since Gaussian distribution is unbounded in an infinite sample, no communication system can be completely error free. Instead, communication links are rated with a maximum bit error rate (BER), which is typically around 10^{-12} for high-speed communication equipment. Achieving a desired BER requires accounting for a number of standard deviations of random noise by using the appropriate value for N (see Table 1) in the formula in Equation 1.

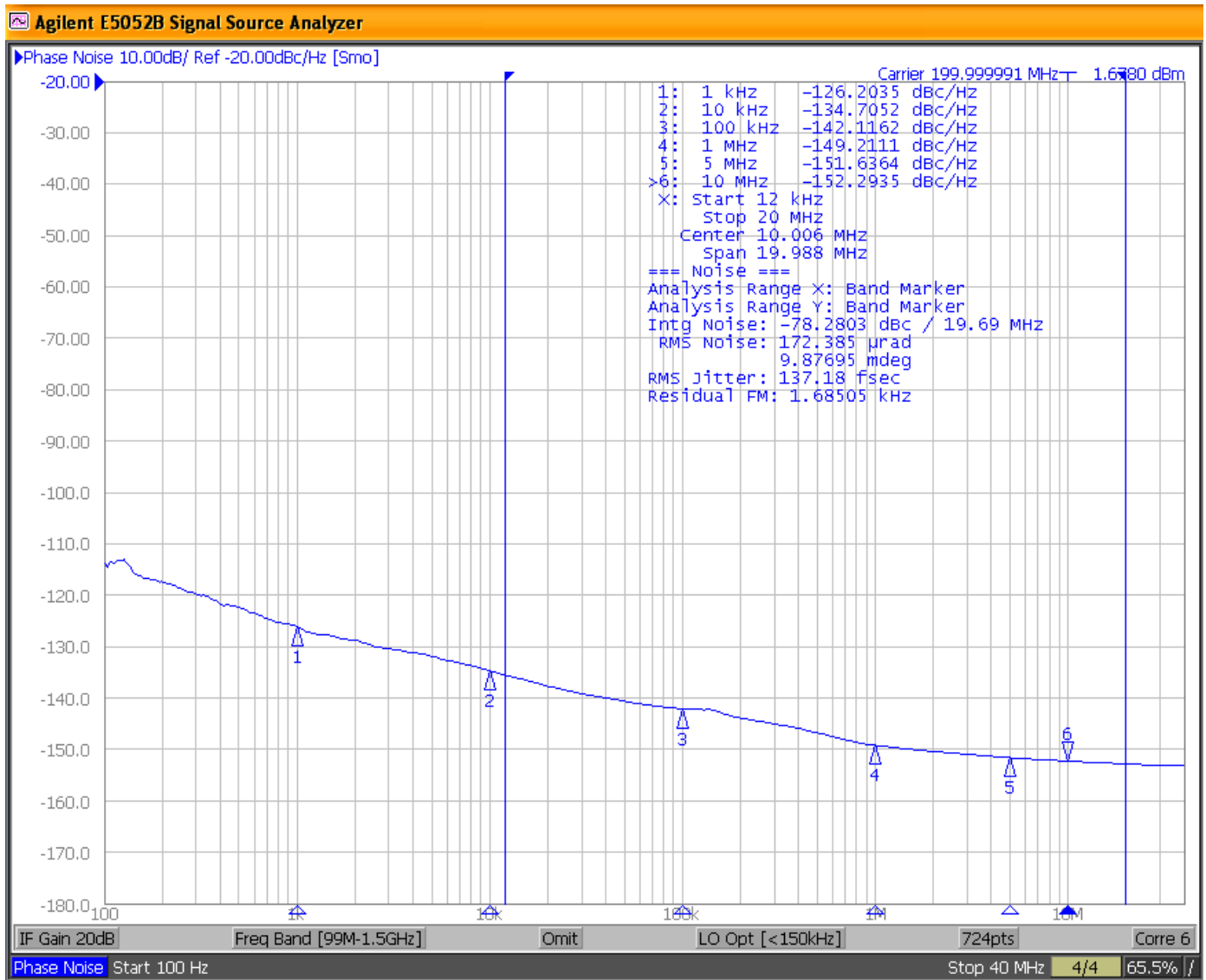
$$T_j = N \times R_j + D_j \quad \text{Eq. 1}$$

Where T_j is total jitter, R_j is random jitter, and D_j is deterministic jitter. If routing clock signals, the deterministic jitter is usually negligible and the T_j is dominated by the random jitter. Calculating T_j from R_j using Equation 1 gives the values in Table 1.

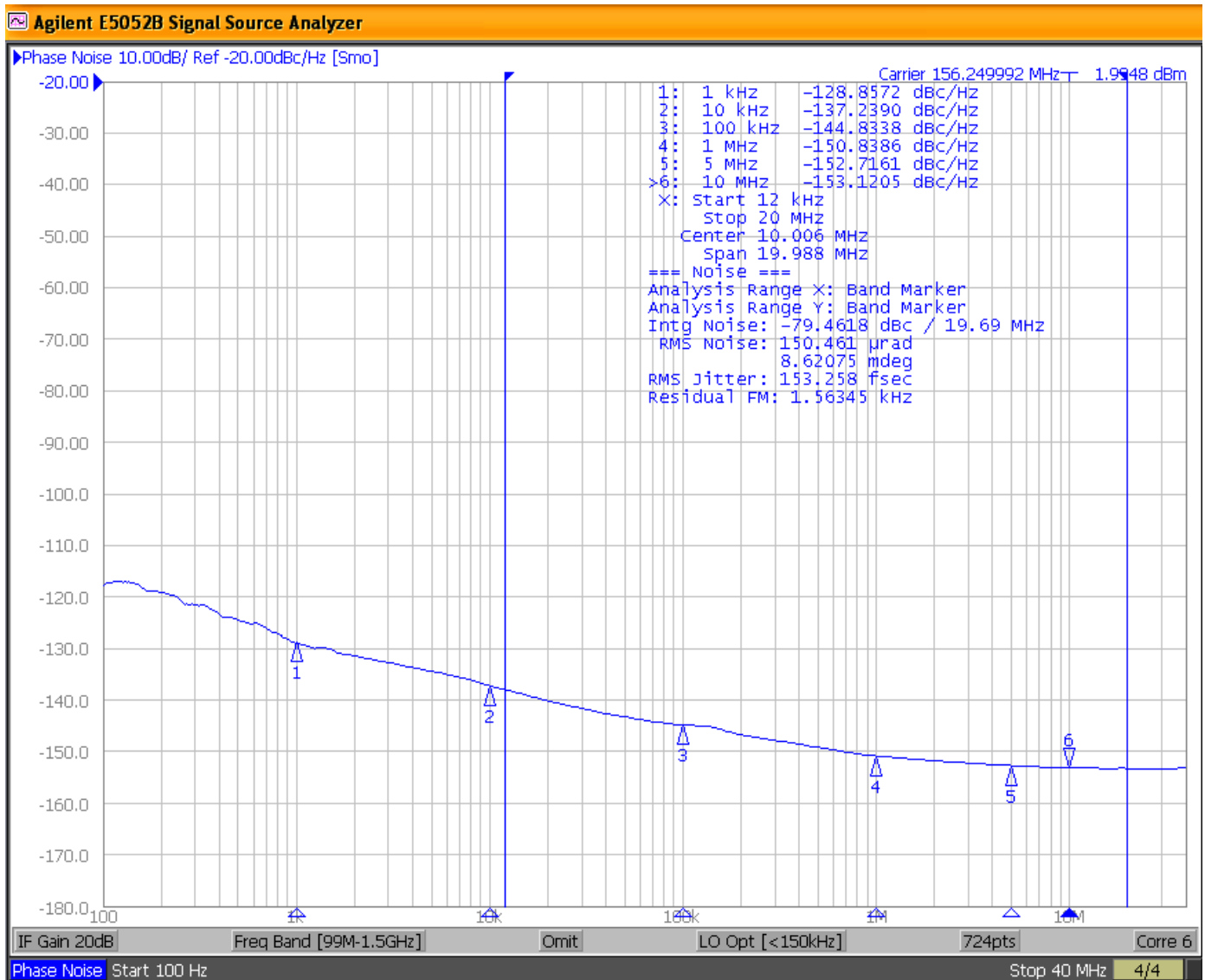
Table 1. Standard Deviations of Random Noise

| BER | N | R_j at 200MHz | T_j at 200MHz |
|------------|--------|----------------------|-----------------|
| 10^{-10} | 12.723 | 137fs _{rms} | 1.743ps |
| 10^{-11} | 13.412 | 137fs _{rms} | 1.837ps |
| 10^{-12} | 14.069 | 137fs _{rms} | 1.927ps |
| 10^{-13} | 14.698 | 137fs _{rms} | 2.013ps |

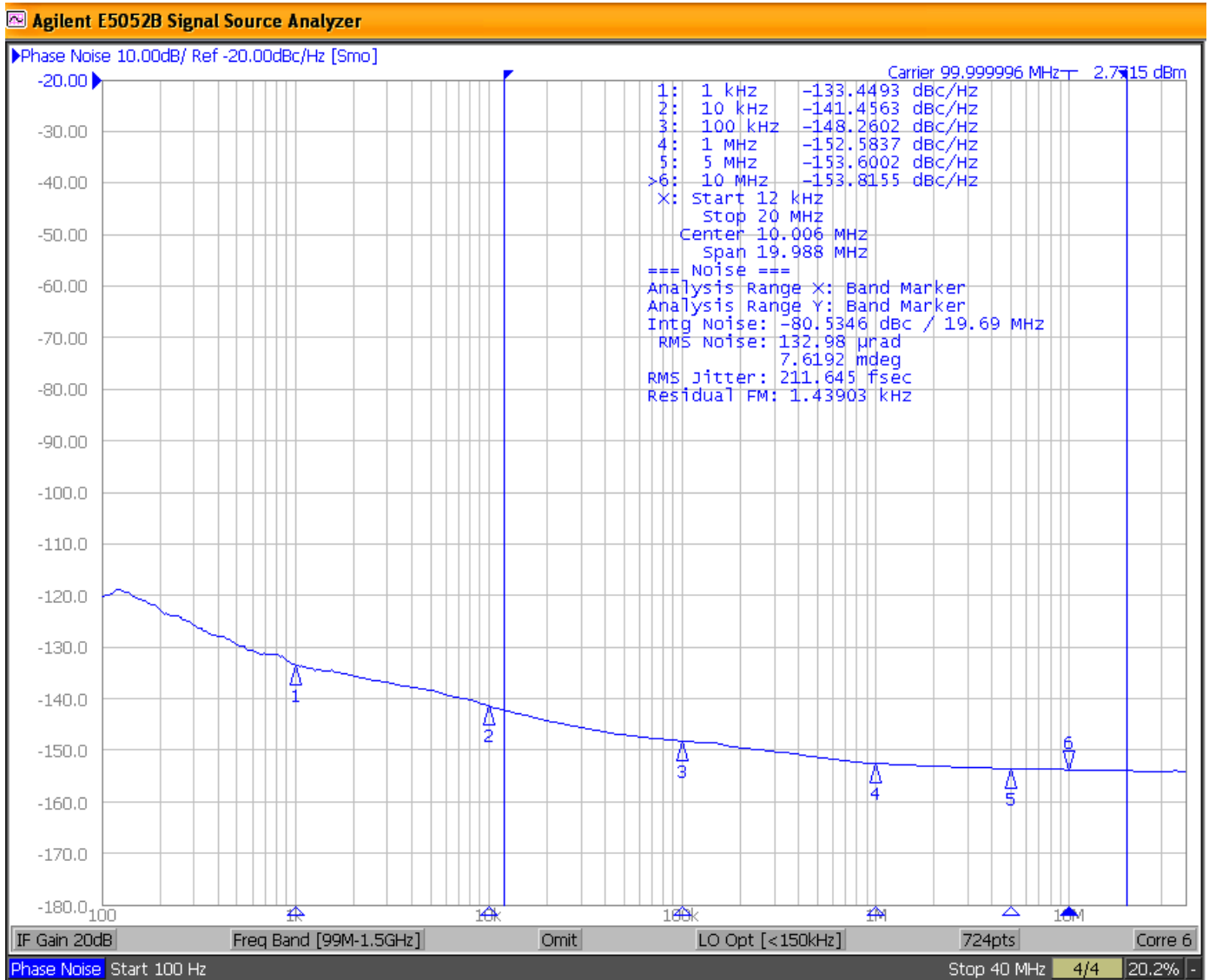
Phase Noise Plots



Phase jitter = 137fs_{rms}, 200MHz carrier frequency; integration range: 12kHz–20MHz

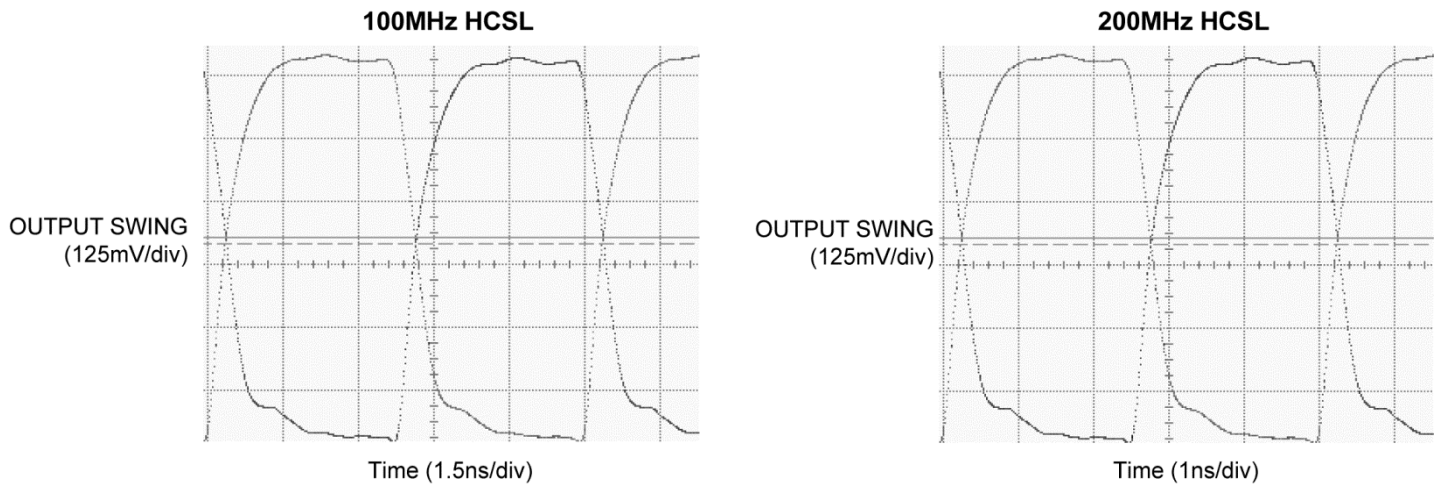


Phase jitter = 153fs_{rms}, 156.25MHz carrier frequency; integration range: 12kHz–20MHz

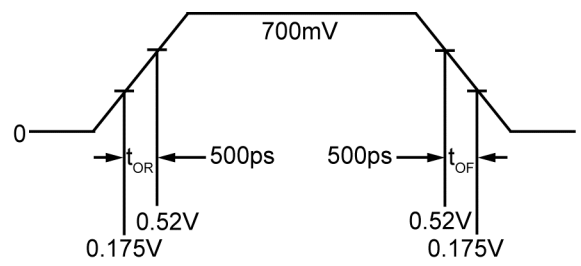


Phase jitter = 212fs_{rms}, 100MHz carrier frequency; integration range: 12kHz–20MHz

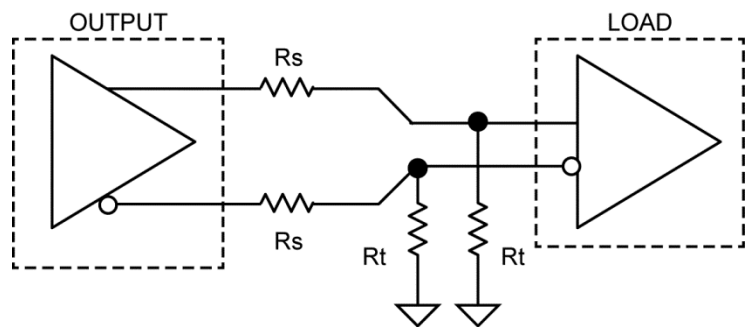
Functional Characteristics



HCSL Waveform Diagram



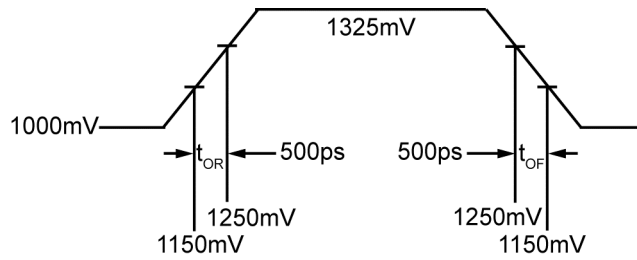
HCSL Interface Application



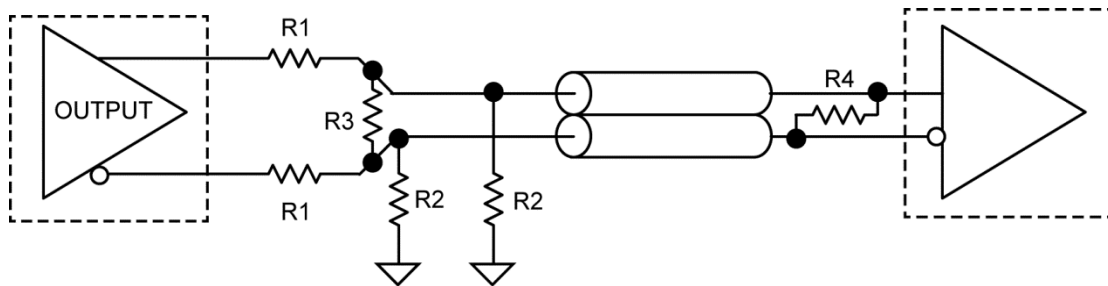
PCI-Express Device Routing

$R_s = 33\Omega$
 $R_t = 50\Omega$

LVDS Waveform Diagram

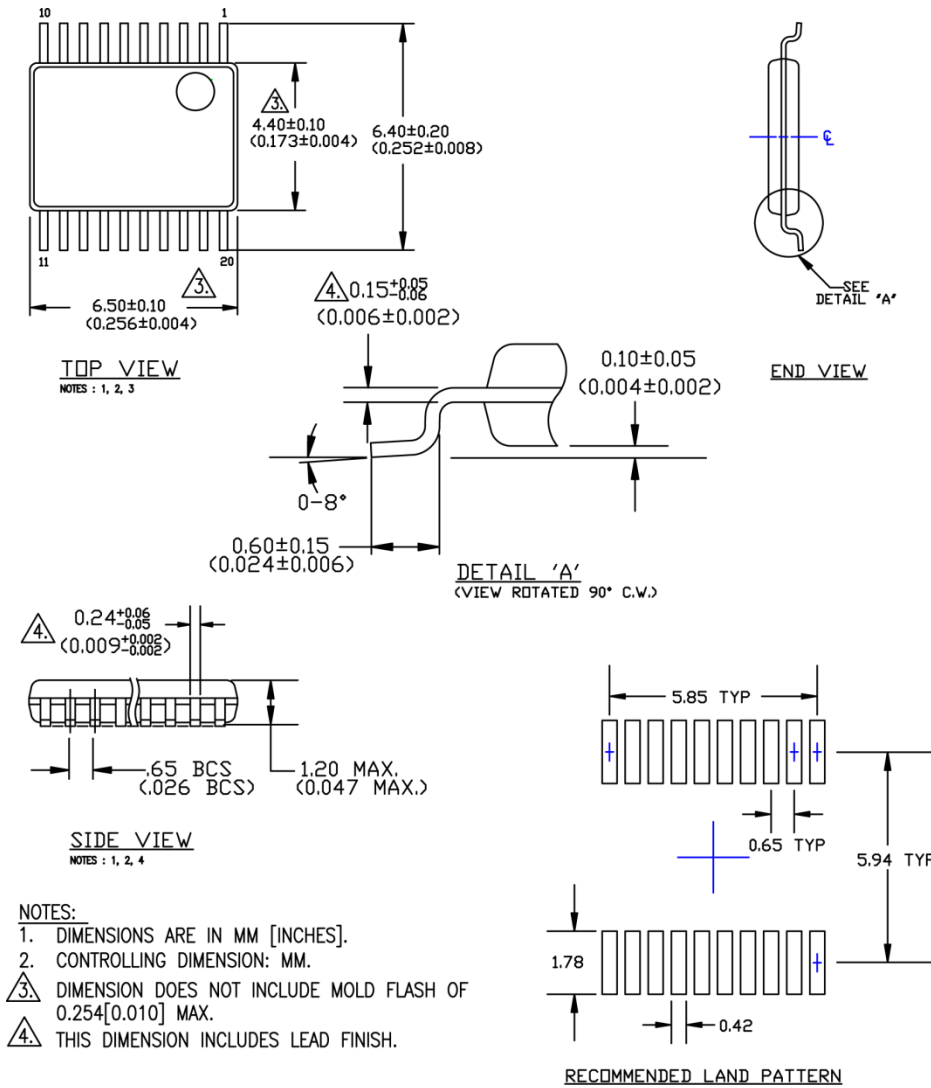


LVDS Interface Application



- R1 = 33Ω
- R2 = 175Ω
- R3 = 140Ω
- R4 = 100Ω

Package Information⁽¹⁴⁾



- NOTES:**
1. DIMENSIONS ARE IN MM [INCHES].
 2. CONTROLLING DIMENSION: MM.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
 4. THIS DIMENSION INCLUDES LEAD FINISH.

20-Pin TSSOP

Note:

14. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
 TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

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Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.