NCL30051LEDGEVB

35-50 Volt, Up to 1.5 Amp, Offline Power Factor Corrected LED Driver with Flexible Dimming Options Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

This application note describes a 60 W, off−line, power factor corrected, line isolated, LED driver using ON Semiconductor's new NCL30051 two−stage controller. This controller contains the control circuitry for both a critical conduction mode (CRM) boost power factor corrector (PFC), and a fixed frequency, series resonant half−bridge converter, and is housed in a 16 pin SOIC package. The high level of integration and low pin count is based on a novel control topology where the PFC output bulk voltage is adjusted via closed loop to change the amount of power transferred by the fixed duty cycle half−bridge. The resonant half−bridge essentially functions as a dc−to−dc step−down transformer. This approach is simpler to implement and stabilize compared to the more complex LCC topology where the frequency of the resonant controller is varied to change the amount of power transferred to the load. The fixed frequency and symmetrical duty cycle of the resonant half−bridge clocking allows for very simple transformer design. This topology is capable of powering series LED loads with efficiencies reaching 90%. This is mainly due to the CRM power factor corrector and the very high efficiency of the resonant half−bridge which results in zero current and voltage switching in the power MOSFETs. Such efficiencies would be quite difficult using a conventional flyback converter in the second stage. Constant voltage, constant current control (CVCC) is handled on the secondary side of the power circuit using ON Semiconductor's NCS1002 CVCC controller with integrated reference. Although this particular design represents a 60 W nominal application, the controller topology is ideal for power levels to 200 W and higher. This specific design is available as evaluation board NCL30051LEDGEVB.

There are a wide variety of medium power lighting applications that would benefit from replacing the traditional light source with an LED source including street lights, refrigerator cases, parking garages, wall washers, wall packs and architectural lighting. All of these applications have high operating hours, challenging environmental conditions, and can benefit from advanced dimming control to further save energy. Moreover many of these applications have accessibility issues that would significantly reduce maintenance costs given the LEDs long operating lifetime. This specific driver design is tailored to support LEDs such as the Cree XLAMP™ XP−G and XM−L, and OSRAM Golden DRAGON® Plus that have maximum drive currents of at least 1000 mA. These LEDs exhibit good efficacies at higher drive currents allowing fewer LEDs to be used to achieve the same light output. For example, the Cree XLAMP XM−L is rated for up to 3 A drive current and has a very low typical forward voltage of 3.1 V @ 1500 mA drive current. At 1500 mA and 85°C junction temperature, in cool white, each LED generates from 440−475 lumens typical with an efficacy of greater than 100 lm/W. So with just 12 LEDs, the source lumen output would be in the range of 5200−5700 lumens at 85°C junction temperature and the typical load power would be ~53 W which is over 100 lm/W.

This application note also focuses on various options for dimming including PWM, analog and bi−level dimming. Intelligent dimming takes full advantage of the instant turn−on characteristics of LEDs and combines it with lighting controls to save significant energy without compromising lighting quality or user safety and comfort. Some traditional large area light sources are difficult to easily dim and have long turn−on times to full brightness. This is not the case with LEDs as they can quickly be turned on and off and their lifetime improves when dimmed because the average operating junction temperature is reduced. PWM and analog dimming are traditional techniques for dimming. Bi−level or multi−level dimming uses these techniques and adds sensors or controls (motion, networked, or timer based) to incorporate two or more discrete lighting levels. This allows additional energy savings without compromising safety and convenience. This is especially useful in outdoor and underground lighting were bi−level control can reduce the light level based on time−of−day or activity detection to save power without compromising safety. In fact the California Lighting Technology recently published a study where bi−level LED lighting saved 87% over conventional 70 W HID outdoor pathway bollards.

Beyond the power stage design, circuitry is provided for demonstrating three types of dimming control:

- Analog dimming with a 0 to 10 V programming signal;
- Bi−level dimming with a simple logic level input signal;
- PWM dimming using an onboard oscillator with variable pulse width.

These three dimming functions are incorporated on an optional plug−in DIM card. Without the card, the demo board can be dimmed with a user provided PWM input signal operating from 150 to 300 Hz. The maximum output voltage can be adjusted via selection of a single resistor; however, it is compliant enough to handle almost a 2:1 output voltage compliance range depending on the string forward voltage and worst case high line voltage. The default output current is set at 1 A, but a maximum DC output current of 1.5 A is available by modifying a single resistor value. Higher currents can be supported with different transformer designs. The power level of this design is targeted at applications operation below 60 Vdc maximum and below 100 VA to be under the maximum power requirements of IEC (EN) 60950−1 (UL1310 Class 2) supplies. The specification table below lists the key design objectives.

Specifications

Universal Input:	90 – 265 Vac (up to 305 Vac with component changes)
Frequency	47 – 63 Hz
Power Factor:	> 0.9 (50−100% of Load with dimming)
Harmonic Content	EN61000−3−2 Class C Compliance
Efficiency	> 88% at 50 −100% of 50 W, I_{out} = 1 A / V_f = 50 V
Target	UL1310 Class 2 Dry/Damp, isolated < 100 VA and < 60 V peak
V_{max} Range:	35 to 50 Vdc (selectable by resistor divider)
Constant Current I_{out} Range:	0.7 – 1.5 A, 1 A nominal (selectable by resistor)
V_{out} Compliance	>50 to 100% of V_{out}
Current Tolerance	±2% or better
Cold Startup	< 1 sec typical to 50% of load
Pout Maximum:	60 W
Dimming:	Two Step Bi−level Analog Dimming PWM dimming with optional DIM board PWM dimming frequency 160 Hz – 300 Hz with external signal input (referenced to a secondary side signal ground) Dimming range > 10:1 0−10 V (100K) analog voltage input dimming, 1 = minimum, 10 V is 100% on (range dependent on nominal AC input)
Protection:	Short Circuit Protection Open Circuit Protection < 60 V peak Over Temperature – (optional) Over Current Protection − Auto recovery Over voltage protection (input and optional output)

Primary Side Circuitry

The primary side circuit schematic is shown in Figure 1. It contains the PFC and resonant half−bridge along with the associated bias, drive, and primary feedback circuitry. As shown in the primary side schematic, the circuit grounds should are segregated into three areas (logic, drive, and power) and interconnected at strategic “star” or “tree” points as shown to minimize ground loops and cross talk interaction. For optimum circuit performance and stability, it is critical that “star” grounding be used for the PCB layout. Logic level timing and filter components such as C10, C12, C14, C15, C17, and C16 should be located as close to main controller U1 as possible.

Jumper JMP1 and test point terminals are provided to facilitate testing the PFC and resonant half−bridge separately. Jumper JMP3 can be used as a wire loop for a clip−on current probe to check the current waveform profile and tuning of the resonant half−bridge.

Referring to Figure 1, a combination common and differential mode conducted EMI filter is incorporated at the mains input. The leakage inductance of L1 in conjunction with “X” capacitors C1 and C2 form a differential mode filter. Common mode filtering is achieved via the coupled inductance of L1 and “Y2” capacitor C27 which ac couples the primary and secondary grounds. In this particular design, the simple common mode filter indictor of L1 was sufficient to pass EN55022, Level A for commercial applications. A plot of the conducted EMI is shown in Figure 14 and the harmonic line current profile is shown in Figure 15.

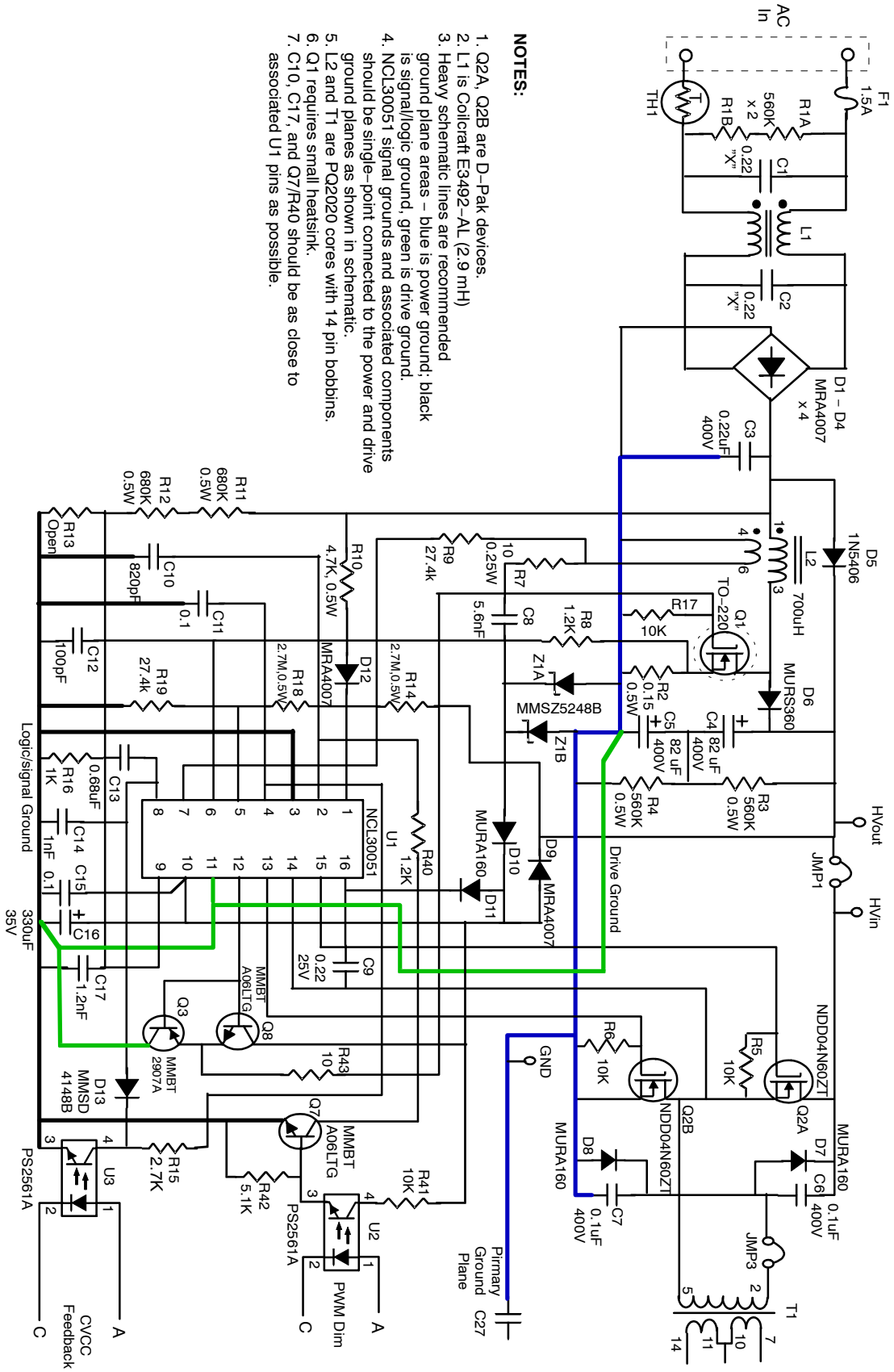


Figure 1. Primary Side Schematic

Power Factor Correction Section

The boost power factor corrector circuit is composed of MOSFET Q1, boost diode D6, boost inductor L2, and the components associated with the PFC control section and pins of the NCL30051 control IC U1. D5 provides a bypass diode to prevent resonant (L/C) charging of series boost output capacitors C4 and C5 during initial startup when the line voltage is first applied. Two 400 Vdc capacitors are used in series for the bulk capacitors to accommodate the 550 maximum bulk voltage. 300 Vdc rated capacitors could have also been used in this application. C3 is a polypropylene film capacitor used to "stiffen" the input source impedance to the boost converter and provide EMI filtering.

Operating bias (V_{CC}) for the control IC U1 is derived from the low voltage auxiliary winding on boost choke L2. This is essentially a charge pump circuit comprised of R7, C8, Z1, D10 and V_{CC} filter capacitors C15 and C16.

The power factor correction circuit operates in critical (or boundary) conduction mode (CRM) and, hence, has a variable switching frequency depending on line and load conditions. Since the L2 inductor current always drops to zero before Q1 is turned back on again, boost diode D6 will have essentially no reverse recovery losses when Q1 is switched on each cycle. In addition the turn−on gate drive requirement for Q1 is minimized since the MOSFET current always starts at zero, however, complementary driver Q3/Q8 is implemented in the gate drive line for efficient switching of Q1.

In some cases it is possible to vary the resistance of R11/R12 slightly to improve the power factor at high line. This circuit provides "feed forward" signal information to the PFC on−time setting capacitor C17. It should also be noted that resistor R9 is used to provide the zero current detect signal (or de−magnetizing signal) to the chip from L2's aux winding so that the circuit can operate in true CRM.

Resonant Half−Bridge Section

The resonant half−bridge is comprised of MOSFET switches Q2A and Q2B, resonant capacitors C6/C7, transformer T1, and the associated components and half−bridge driver section of U1. Since Q2A, the upper MOSFET is "floating" at a switched node, a "bootstrap" driver bias supply composed of D11, C9 and the internal circuitry of U1 is implemented for gate drive of this MOSFET.

The half−bridge is operated with a fixed frequency, symmetric duty ratio (with dead time between each half−cycle) signal and is powered from the PFC bulk voltage. The NCL30051 controller is rated for up to 600 Vdc operation in the half−bridge section, so factoring in system derating, a maximum operating PFC bulk voltage in the 480−510 V range is recommended. Resonant circuit operation is achieved by resonating the leakage inductance of T1's primary with capacitors C6/C7 which appear in parallel. By adjusting the L/C ratio of these parameters to match the switching frequency of the gate drive output of U1, resonant operation is possible with very low switching losses in MOSFETs Q2A and Q2B. The frequency of the half−bridge drive is set by the C_t capacitor C10. This value can be changed to accommodate the resonant frequency determined by C6/C7 and T1's leakage inductance. Without any complex winding structure, the leakage inductance of T1 came out to about 100 μH with the transformer design shown in Figure 4. The waveform of the sinusoidal primary current (45 W output) is shown in Figure 2. The use of fixed frequency, resonant switching in the half−bridge creates a condition of zero current switching in the MOSFETs which results in very high conversion efficiency. Diodes D7 and D8 provide voltage clamping to the bulk rail in the event of parasitically generated voltages or transients during start up and/or dynamic operation.

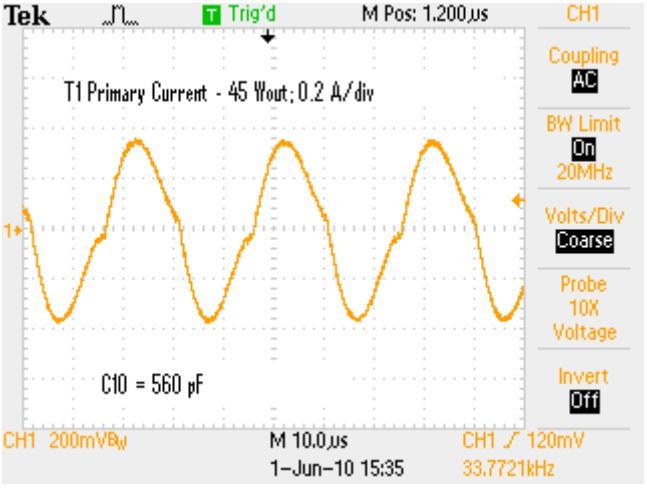


Figure 2. Resonant Half−Bridge Current Waveform

Secondary Side Circuitry

The secondary winding of the half−bridge transformer, the full−wave, center−tap rectifier, and the associated secondary side circuitry are shown in the schematic of Figure 3. The secondary rectifier D16 is a dual Schottky device and, because of the symmetrical duty ratio, only a modest amount of capacitive filtering is necessary to attenuate the high frequency output ripple. In this design a paralleled pair of 4.7 μF, 100 Vdc film capacitors were used.

The current and voltage sensing circuitry is based around the NCS1002 CVCC controller. The specific sensing circuitry is essentially identical to that used in ON Semiconductor application note AND8470 for the NCL30001 LED controller and will only be briefly described here.

Current regulation is accomplished by section B of U4. The output current is sensed by resistor R22 and the dc output current level can be adjusted by changing R26. If PWM dimming is used, the circuit of Q5, C22, R31 and R32 form a sample and hold circuit that prevents the current pulse interruptions through current sense resistor R22 from corrupting the dc current sense information presented to pin 6 of U4B. This keeps the peak current output level constant during PWM dimming.

Output voltage sensing is achieved via the sense divider of R28 and R29 and U4A. The maximum output voltage can be adjusted by the value of R28 and is set to approximately 50 V in this application.

Both amplifiers drive optocoupler U3 which controls the pulse width of the PFC MOSFET by pulling compensation pin 8 low on the main controller U1. In this way the bulk output voltage of the PFC is regulated so as to provide a correct high voltage dc input to the resonant half−bridge converter. The amplifier whose output is lowest will be dominant, thus providing constant current, constant voltage control with a smooth transition at the CVCC knee. To minimize the Miller capacitance effects of optocoupler U3's photo transistor to the feedback loop, R15 and D13 have been added to force extra current through the opto transistor without loading pin 8 of U1.

Since the PFC also senses the bulk output voltage via resistor network R14, R18, and R19, this divider is set via R19 such that this "inner" voltage loop is closed when the bulk voltage reaches 550 Vdc so as to not prematurely interfere with the secondary voltage loop of U4A. Note that if the secondary voltage feedback loop were to fail, the inner PFC voltage feedback loop would clamp the bulk voltage to approximately 550 Vdc.

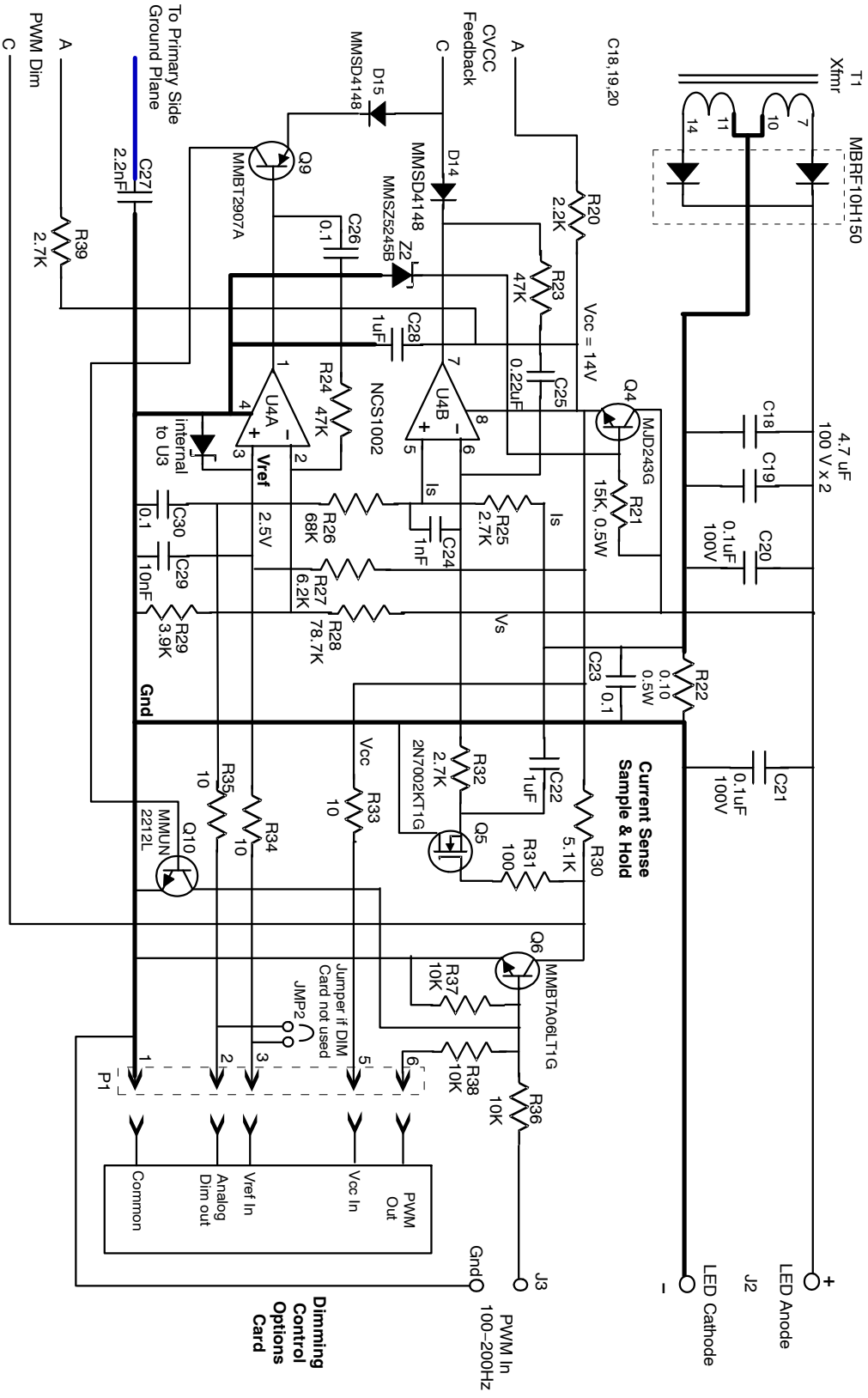


Figure 3. Secondary Side Schematic

Notes:

1. D16 requires small heatsink.
2. Heavy schematic lines are recommended ground plane areas.

NCL30051 LED Driver CVCC Secondary Sensing

Resonant Half−Bridge Transformer Design (T1)

Since the half−bridge transformer operates in a fixed frequency, symmetrical duty ratio, the design becomes very straightforward. A half−bridge converter switches 1/2 of bulk voltage across the transformer primary due to the capacitive divider network formed by resonant capacitors C6 and C7. By choosing the maximum bulk voltage at about 500 Vdc and assuming a maximum output voltage of 50 V, the turns ratio on the transformer will be:

$V_{bulk}/2$ divided by 50 V_{out} = 250/50 = 5

So, a turns' ratio of 5:1 is required between the primary and one of the half's of the−secondary(note: push−pull output rectification!). All that is required now is to determine the minimum number of primary turns necessary to avoid core saturation and then ratio the secondary turns from this point. The selected core is a PQ−2020 with a cross sectional core area (Ae) of 0.6 cm^2. Using the transformer design relationship:

$$Np = \frac{V \times D \times 10^8}{4 \times F \times BM \times Ae} = \frac{20\ V \times 1 \times 10^8}{4 \times 35\ kHz\ 3200G \times 0.6\ cm^2}$$

$$= 96.7\ turns$$

Where: Np is the minimum primary turns needed
V is the max voltage across the primary (with a little margin)
F is the switching frequency
Bm is the maximum flux density in the ferrite core
Ae is the cross sectional area of the core

The average primary current will be a little more than 60 W / 250 Vdc x 0.95 = 228 mA assuming close to 95% converter efficiency. The rms value will actually be a little higher but AWG # 28 magnet wire will easily handle this and 96 turns can comfortably be wound over 3 layers with 32 turns per layer.

The number of secondary turns will be 96 / 5 = 19.2 turns so 19 turns will be close enough. It turns out that due to the center tapped secondary, two strands of #26 magnet wire wound bifilar on top of the primary will make the secondary easily handle up to 1.5 A output current. The primary leakage inductance is the only unknown factor that was not actually purposely designed in, however, with the three layer primary and adequate insulating tape between the primary and secondary there should be adequate leakage inductance that will facilitate a resonant capacitor with a common value that will obtain a reasonable resonant frequency that can be accommodated by the internal half−bridge clock in the NCL30051 controller. By shorting the transformer secondary pins out with very short wires, the primary leakage can be measured with an inductance meter. In this design the leakage inductance worked out to be between 90 and 100 μH, sufficient to produce a resonant frequency of 36 kHz with a pair of 0.1 μF capacitors (in parallel effectively) for C6 and C7. It turned out that a clock timing capacitor of 1 nF for C10 sets the switching frequency to about 36 kHz which provided the optimum tuning as displayed in primary current waveform of Figure 2. The design summary of the transformer T1 is shown in Figure 4.

Since the output current and/or voltage is regulated by controlling the PFC bulk voltage, the value of the bulk voltage will be directly proportional to V_{out} via the turns ratio of the transformer. For example, if we have an LED string with a nominal forward voltage of 40 V, the bulk voltage will be regulated at: V_{out} x Np/Ns x 2 = 40 x 5 x 2 = 400 Vdc (where two represents the fact that the half−bridge primary switches only 1/2 of the bulk voltage). Herein highlights a limitation of this topology in cases where the string voltage may be very low. For a V_f of 32 V, the bulk voltage will be 320 Vdc and this puts a limit on the maximum line voltage in which the PFC boost converter can function. The bulk voltage must always be higher than the peak of the line voltage for the boost converter to work, so at 230 Vac input, the line peak is 1.4 x 230 = 322 V so now we have reached the lower limit of the LED forward voltage range. Obviously at 120 Vac (V_{peak} = 170 Vdc) we could feasibly allow the output V_f to go even as low as 25 Vdc without any problems (25 Vdc x 5 x 2 = 250 Vdc bulk which is still higher than Vac peak). Careful analysis of the throughput voltage conversion and proper selection of the transformer turns ratio will allow optimization for a given LED application. A maximum operating PFC bulk voltage of 510 Vdc is recommended for adequate safety margins. Examples and further discussions of the circuit limitations are addressed below under "Topology Limitations".

Part Description: Resonant Half−bridge Transformer − 60 W, 35 kHz (Rev 3)

Schematic ID: T1

Core Type: PQ20/20, Ferroxcube 3C95 or equivalent material

Primary Inductance: 6 mH minimum

Leakage Inductance: 90 − 100 uH nominal (resonant half−bridge, leakage inductance is Lr)

Bobbin Type: PQ20/20 14 pin PC mount bobbin

Windings (in order):

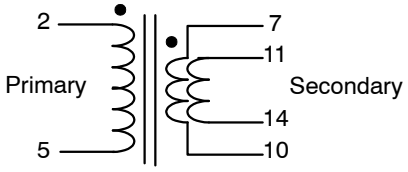
Winding # / type	Turns / Material / Gauge / Insulation Data
Primary winding (2 − 5)	96 turns of #28 HN magnet wire over 3 layers, 32 turns per layer approx. Self−leads to pins. Insulate with Mylar tape sufficient for 3 kV Hipot to next winding.
Secondary winding (7,11 − 10,14)	19 turns of 2 X #26 magnet wire bifilar wound over two layers. Self−leads to pins per schematic below. Final insulate with Mylar tape.

Note: The critical parameter is to achieve a leakage inductance of 90 − 100 uH with a min primary inductance of 6 mH. The overall turns can be increased or decreased to achieve this as long as the turns ratio remains 5:1.

Vacuum varnish assembly.

Hipot: 3000 volts from Primary to Secondary (1 minute)

Schematic



Lead Breakout / Pinout

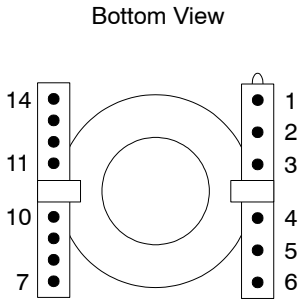


Figure 4. Resonant Half−Bridge Transformer Design (T1)

PFC Choke Design (L2)

Using the PFC design approach illustrated in ON Semiconductor Application Note AND8123, we can analyze the PFC choke design.

Inductor rms current at 50 W output and 85 Vac input: 0.72 A

Inductor peak current at 50 W out and 85 Vac input: 1.75 A

Maximum inductance for reasonable switching frequency: 1200 μH max.

Turns ratio to aux winding to produce a 15 to 18 Vdc V_{CC}: 9:1 or 10:1

To maintain component consistency, a PQ−2020 ferrite core was also selected for the PFC choke. Based on an rms choke current of 0.72 A and an average switching frequency of around 100 kHz, three strands of AWG #30 magnet wire was chosen for the main winding to minimize ac losses. Calculations based on the approximate wire diameter (2 x 0.012" or 0.61 mm), and a core bobbin inside winding width of about 0.47" (12 mm); it appears that 75 turns of this wire can comfortably be wound on 4 or 5 layers with about 18 turns per layer. Using the above parameters from the design spreadsheet, and the following inductor relationships we can determine the optimum design using this PQ−2020 core:

$$L = \frac{N \times B_{max} \times Ae}{Ipk \times 10^8} \text{ and } Lg = \frac{0.4\pi \times N \times Ipk}{B_{max}}$$

Where: N is the number of turns
B_{max} is the max flux density
Ipk is the peak inductor current
Ae is the core cross sectional area (cm^2)
Lg is the total core gap (cm)

Substituting the known values into first equation for N = 75 turns, B_{max} = 3000 gauss, Ae = 0.6, and Ipk = 1.75 A we get L = 770 μH which is less than the max of 1200 μH. This will result in a switching frequency of 70 kHz min and 200 kHz max for typical operation, so this is probably a reasonable inductance to start with. We could increase the inductance and lower the PFC switching frequency by adding more turns, but this would probably require a larger core.

In order to prevent saturation, the core must be gapped per the second equation. Substituting in the known parameters we get Lg = 0.055 cm or 0.022 inches. Since this is the total gap, we would use half of this length if we were gapping all three pole legs of the core. This gap should also give us the required inductance of about 700 μH. The final choke design is shown in Figure 5.

Part Description: PFC Choke – 60 W, 100 kHz (CRM); Rev. 4 (6/8/10)

Schematic ID: L2

Core Type: PQ20/20, Ferroxcube 3C95 or equivalent material

Core Gap: Gap for 675 uH +/–25 uH across pins 1 to 3.

Inductance: 650 – 700 uH nominal

Bobbin Type: PQ20/20 14 pin PC mount bobbin

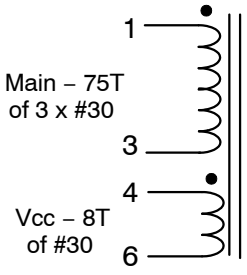
Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
Main winding (1 – 3)	75 turns of 3 strands of #30 trifilar wound. Wire can be twisted if desired. Self–leads to pins. Insulate with 2 or 3 layers of Mylar tape to next winding. (Other option: 2 strands #28 bifilar)
Vcc winding (4 – 6)	8 turns of #30 magnet wire spiral wound over one layer. Self–leads to pins. Final insulate with Mylar tape.

Vacuum varnish assembly.

Hipot: 1000 volts from main winding to Vcc winding..

Schematic



Lead Breakout / Pinout

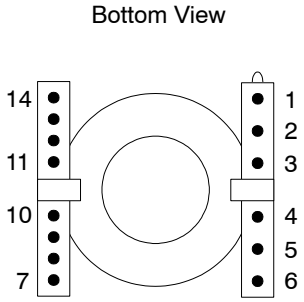


Figure 5. PFC Choke Design Details (L2)

Dimming Capabilities

To demonstrate the LED dimming capabilities of this circuit, the same DIM control card used in the NCL30001 LED driver circuit described in AND8470 has been used here. Dimming can be accomplished using three methods: pulse width modulation (PWM) of the output current; analog current dimming where the current reference voltage for U4B is modified via a 1 to 10 V control signal to linearly control the output current to the LEDs; and bi−level dimming in which a logic level signal will lower the LED intensity level by reducing the LED output current. Without this DIM card, a PWM input terminal (J3) is still provided for an external 160 to 300 Hz PWM input signal to control the output current. This is done by switching transistor Q6 on and off which in turn switches the sample and hold transistor gate drive, and toggles optocoupler U2 which switches U1's Ct pin (2) via buffer transistor Q7. This pin, when grounded, will terminate drive to the half−bridge MOSFETs (Q2A, Q2B) thus rapidly stopping output current flow. Due to the low value of output capacitors C18 and C19, a rectangular wave signal in the frequency range of 160 to 300 Hz will adequately PWM the output current with good rise and fall times (see Figure 6). C1 on the DIM card sets this frequency. Higher dimming frequencies can but used but the dynamic range of the dimming can be limited due to waveform fall times. It should be noted that jumper J2 across pins 2 and 3 of connector P1 is necessary if the DIM card is not installed. More details of the DIM card operation can be found in AND8470. A table for configuring the three different operating modes is shown below and the schematic for the DIM card circuit is shown in Figure 7.

Dimming Configuration	Modifications; Jumper Configurations
External PWM dimming input	Omit DIM card; short pins 2 and 3 of P1. Inject PWM signal into J3
Internal PWM dimming	Add DIM card with JMP1 added to P1 on DIM card; Add JMP3 to P2 on DIM card. Adjust pot R1 to vary pulse width.
Bi−Level Dimming	Add DIM card with JMP1 (P1) removed; Add JMP3 to P2 on card; Connect switch from TP1 and TP2. Closed switch gives low dim level.
Analog Dimming, Internal Adjust	Add DIM card with JMP1 (P1) removed: Add JMP2 to P2; Adjust pot R9 for LED brightness.
Analog Dimming, External Adjust	Add DIM card with JMP1 (P1) removed. Add JMP2 to P2. Remove pot R9 and wire in external 100k potentiometer to TPs 2, 3 and 4. TP3 is the pot wiper. Adjust external pot for LED brightness.

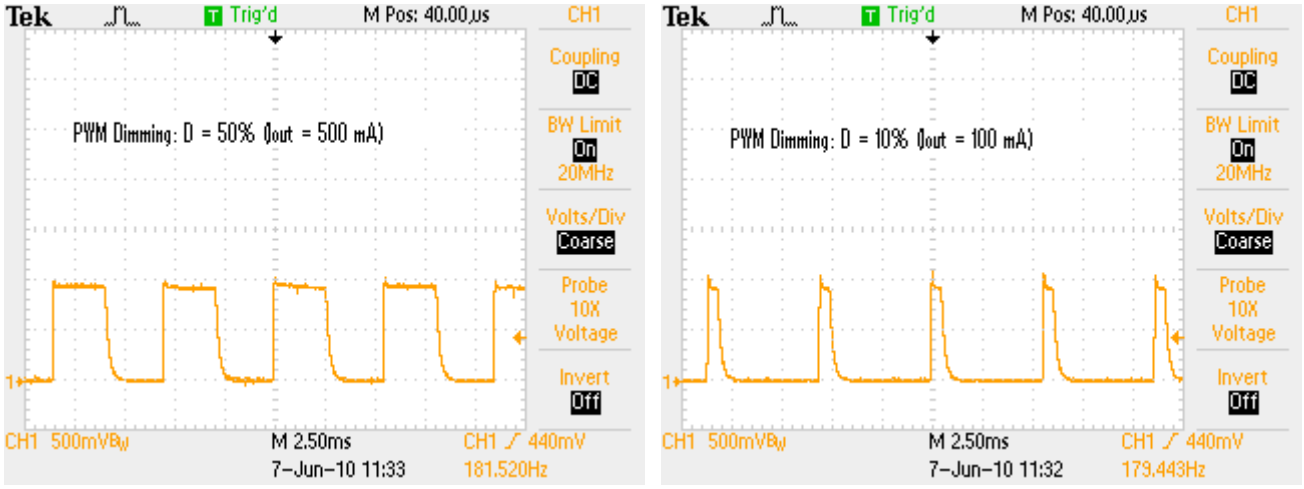
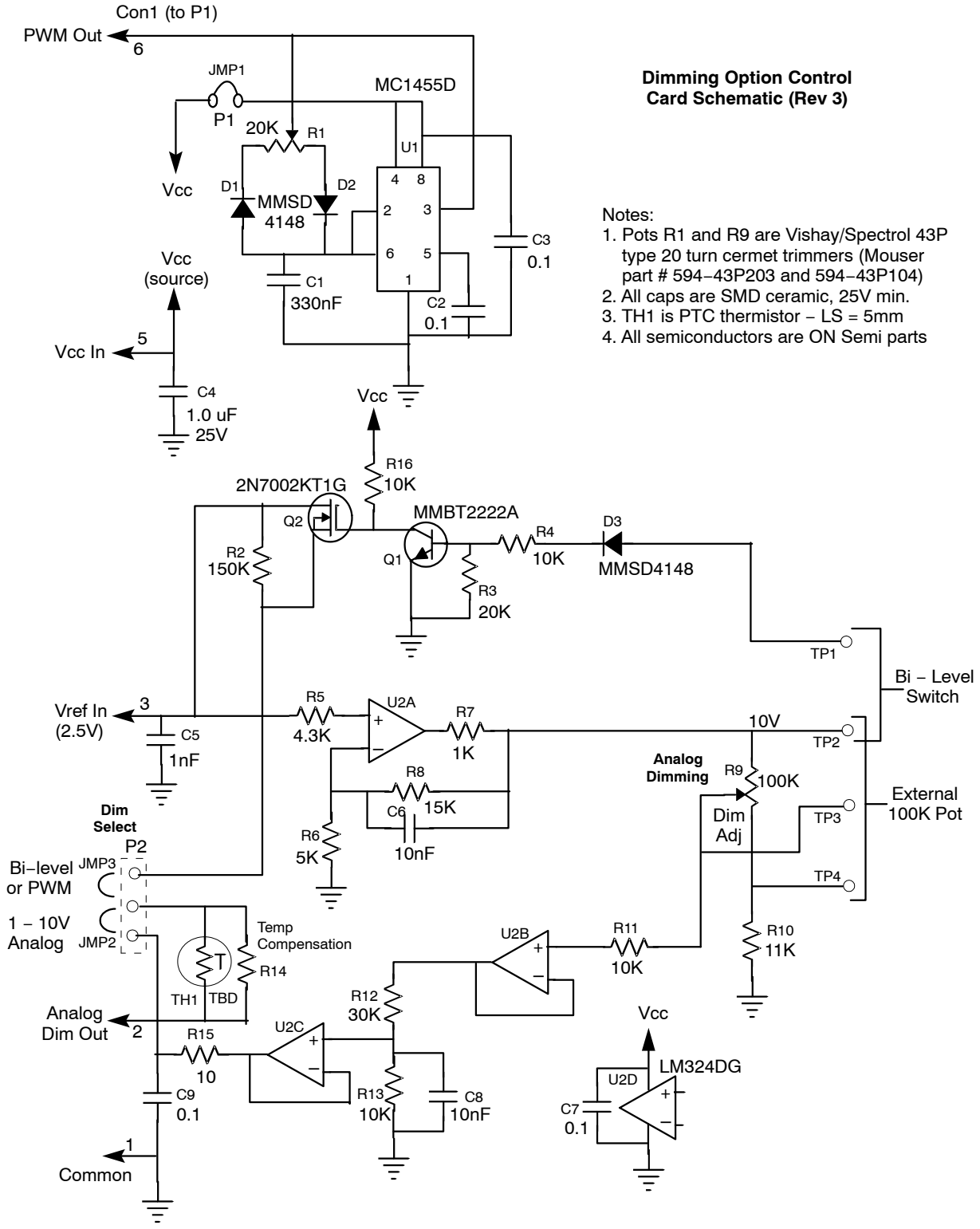


Figure 6. PWM Dimming Mode – Output Current Profile

Depending on the selected PWM dimming frequency (C1 of Figure 7), it is possible to get a slight beat between this frequency and a harmonic of the line frequency. Depending on the magnitude of the overall output ripple and the selection of C4 / C5, there is the potential for LED current modulation at some pulse widths. It is best to select the PWM dimming frequency to be in between the line frequency harmonics. Thus, 160 or 220 Hz would be recommended optimum PWM frequencies for a line frequency of 60 Hz. (See section on Output Ripple below.)



Dimming Option Control Card Schematic (Rev 3)

Notes:
1. Pots R1 and R9 are Vishay/Spectrol 43P type 20 turn cermet trimmers (Mouser part # 594−43P203 and 594−43P104)
2. All caps are SMD ceramic, 25V min.
3. TH1 is PTC thermistor − LS = 5mm
4. All semiconductors are ON Semi parts

Figure 7. DIM Card Schematic

Topology Limitations

Despite the high efficiency and relatively low complexity of the resonant half−bridge and magnetics design in this topology, it does have some limitations with respect to the ac line and output load forward voltage extremes. These limitations are primarily due to the fact that, since the feedback loop controls the output voltage of the power factor corrector, the "bulk" voltage is directly proportional to V_{out} or the V_f of the diode string when operating in the normal constant current mode. Since the output (V_{bulk}) of a boost converter must always be higher then the peak ac input voltage for the boost converter to function, the relationship that V_{bulk} > Vac peak must always be maintained for continuous circuit operation and constant output. In the design example for this demo board, the PFC output bulk voltage is 10 times the output voltage (or V_f) due to the transformer turns ratio (5:1) and the fact that the resonant half−bridge switches 1/2 of the bulk across the transformer primary. We can deduce some of the limitations from this fact. The best way is to see the impact the nominal ac line voltage has on the output V_f. The NCL30051 has a 600 V max rating on the high side gate driver section (pins 15 and 16). As a consequence, assuming an 85% derating, the bulk bus can be set at 510 Vdc max. Under these conditions V_{out} max under no load conditions could be 50 Vdc with the 5:1 turns ratio on T1. Assuming this 50 Vdc output max as our nominal open circuit V_{out}, let's see what the minimum output V_f can be that will still maintain boost converter operation for normal ac line voltages.

120 Vac: In this case the peak line voltage will be 1.4 x 120 Vac = 168 Vpk. Dividing this peak by 10 (T1 turns ratio x half−bridge factor of 2) yields 16.8 V which is less than 1/3 of the V_f max of 55 V. This would theoretically allow a 3:1 V_f compliance ratio, however, due to the fact that the primary V_{CC} is derived from the PFC inductor aux winding, experimentation has shown that 20 Vdc is actually the lowest safe minimum V_f for 120 Vac input for reliable V_{CC} maintenance for this design.

230 Vac: The peak line voltage will be 230 x 1.4 = 322 Vpk. Again, dividing this by 10 yields 32.2 V, or 35 V for the minimum output V_f with a tolerance margin.

277 Vac: Vpk = 277 x 1.4 = 388 Vdc, so output V_f minimum becomes about 40 Vdc.

305 Vac: Vpk = 305 x 1.4 = 427 Vdc; so output V_f minimum becomes about 45 Vdc

This limitation should considered up front when designing the LED driver and the consequential effects of the min and max of the diode string V_f as a result of binning, forward current and thermal variations. For applications with high nominal line levels, the transformer turns ratio becomes more critical when optimizing max and min load V_f tolerances. As seen from the 120 Vac input example, there is much V_f latitude.

The usable dimming range can also be affected by the combination of line voltage and V_f. This is particularly acute when using the analog dimming mode because this mode also reduces the primary side control circuit V_{CC} as the output current is reduced. PWM dimming mode has less effect on the V_{CC} due to the fact that the V_{CC} capacitor is peak charged and the reflected peak V_{CC} aux voltage does not appreciably decrease with PWM dimming.

Figure 8 shows the limitations of increasing AC input line on the minimum usable V_f out. The diagonal section of the graph indicates converter shutdown and re−start action.

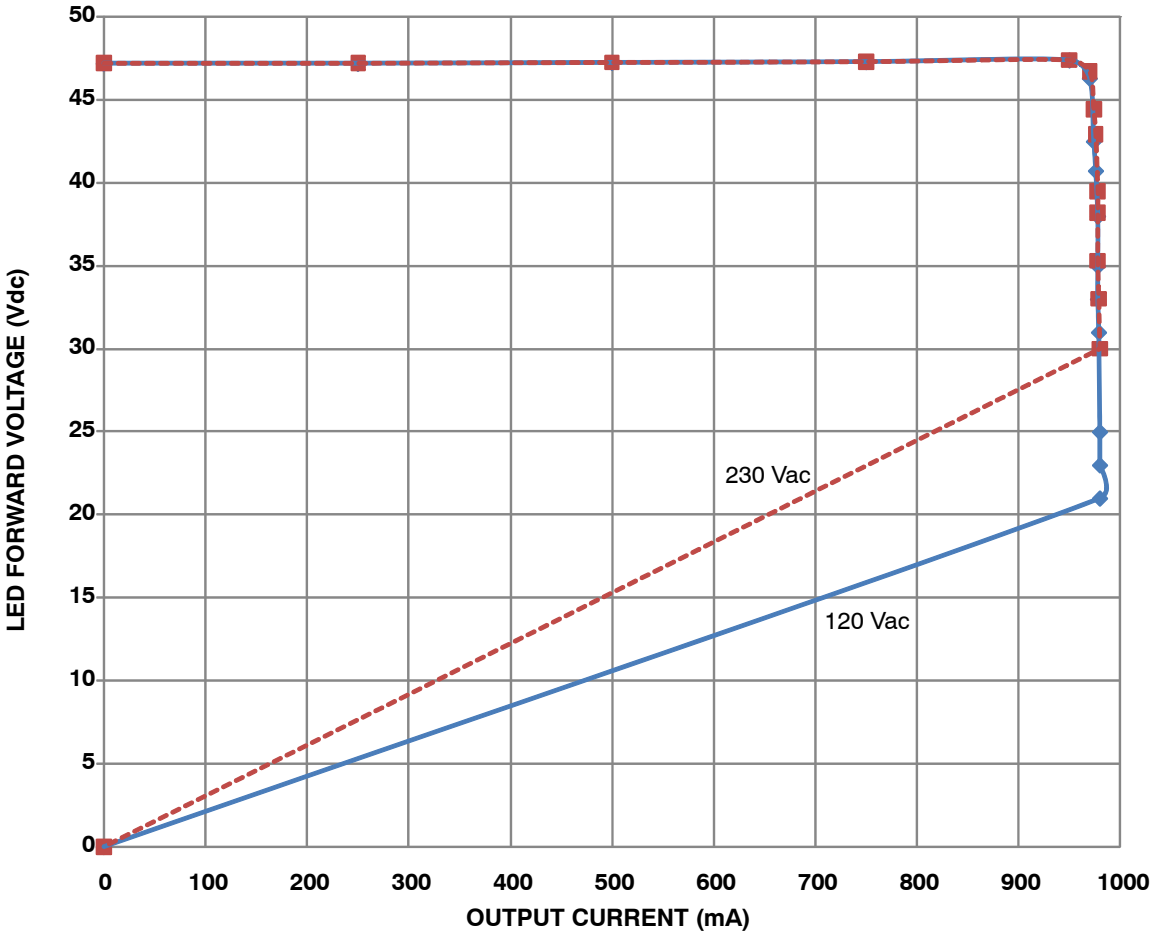


Figure 8. Output Current/Voltage Transfer Function versus Line

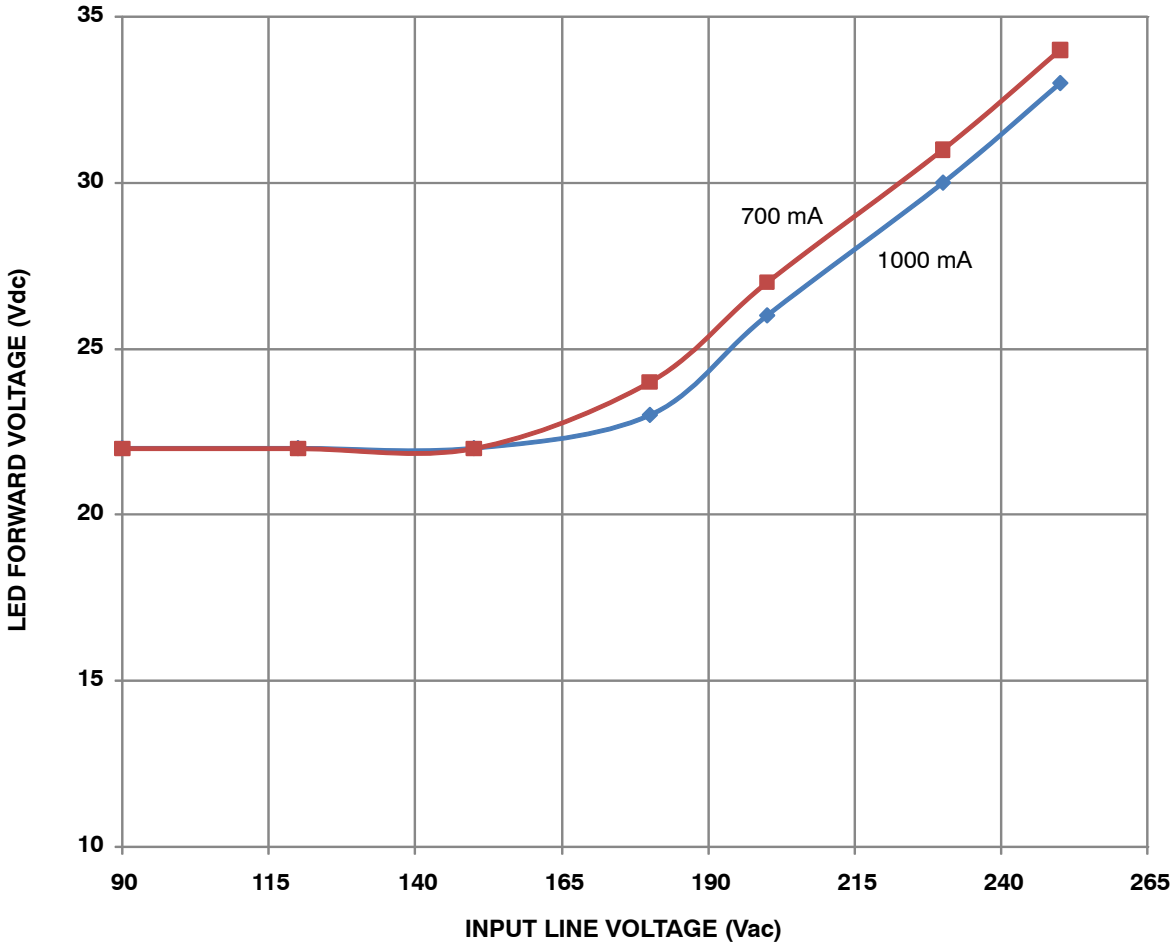


Figure 9. Minimum Forward Voltage versus Line and Output Current

Efficiency

With this topology it is possible to achieve better than 90% efficiency even at modest loads. As illustrated in Figure 10, the efficiency is greater than 90% from 35−45 W for both 120 and 230 Vac for this 50 W nominal design.

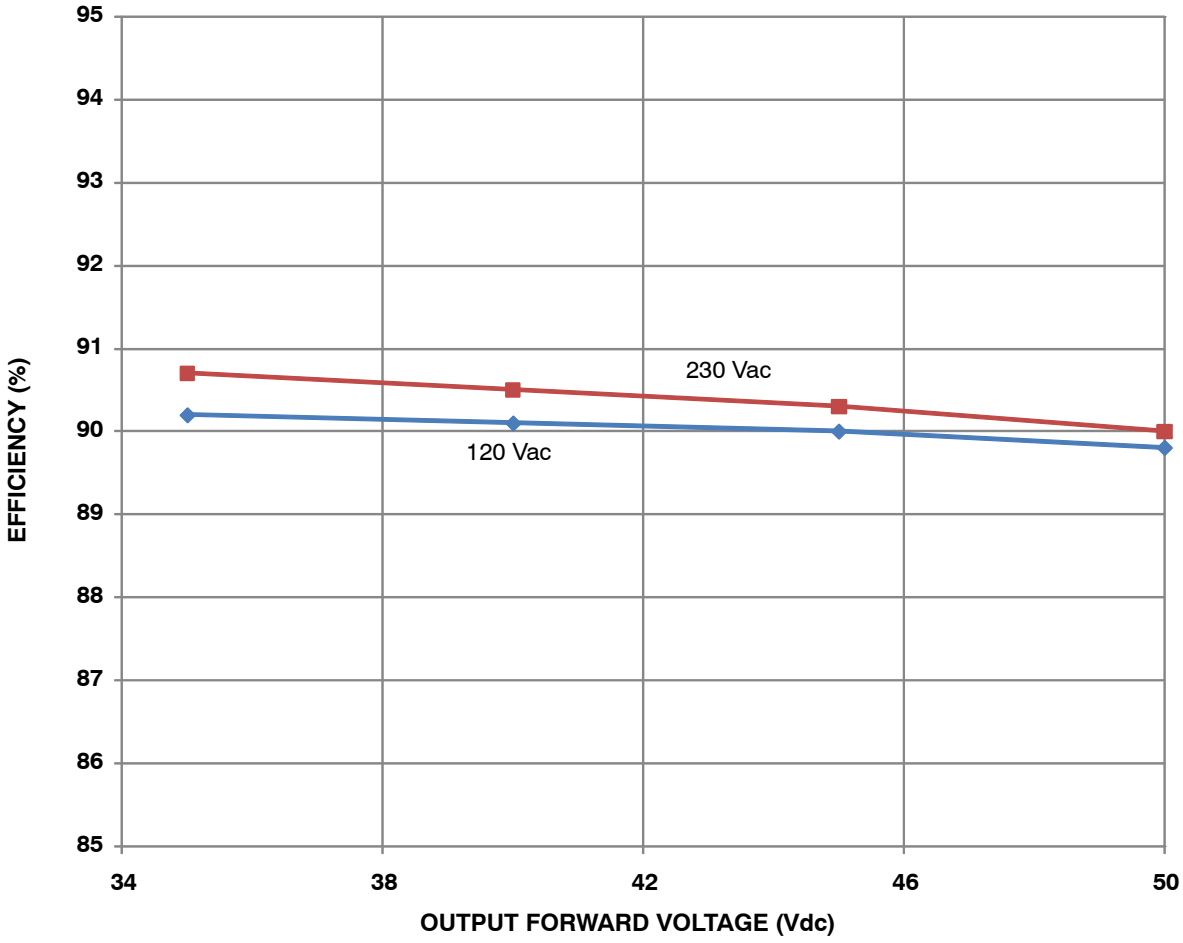


Figure 10. Efficiency versus line and load

Power Factor and Input Harmonic Content

The power factor will remain above 0.90 for the rated load output (1 A) and to minimum V_f levels for 120 Vac input and down to V_f = 35 Vdc for 230 Vac. As the actual current load is decreased from the rated maximum, the power factor will also degrade with lower V_f. These effects are shown in Figure 10.

In addition to power factor, a more critical parameter in some regions is harmonic content. Lighting Power supplies fall under the IEC61000−3−2 Class C standard and there are vary strict limits on harmonic content for power supplies > 25 W.

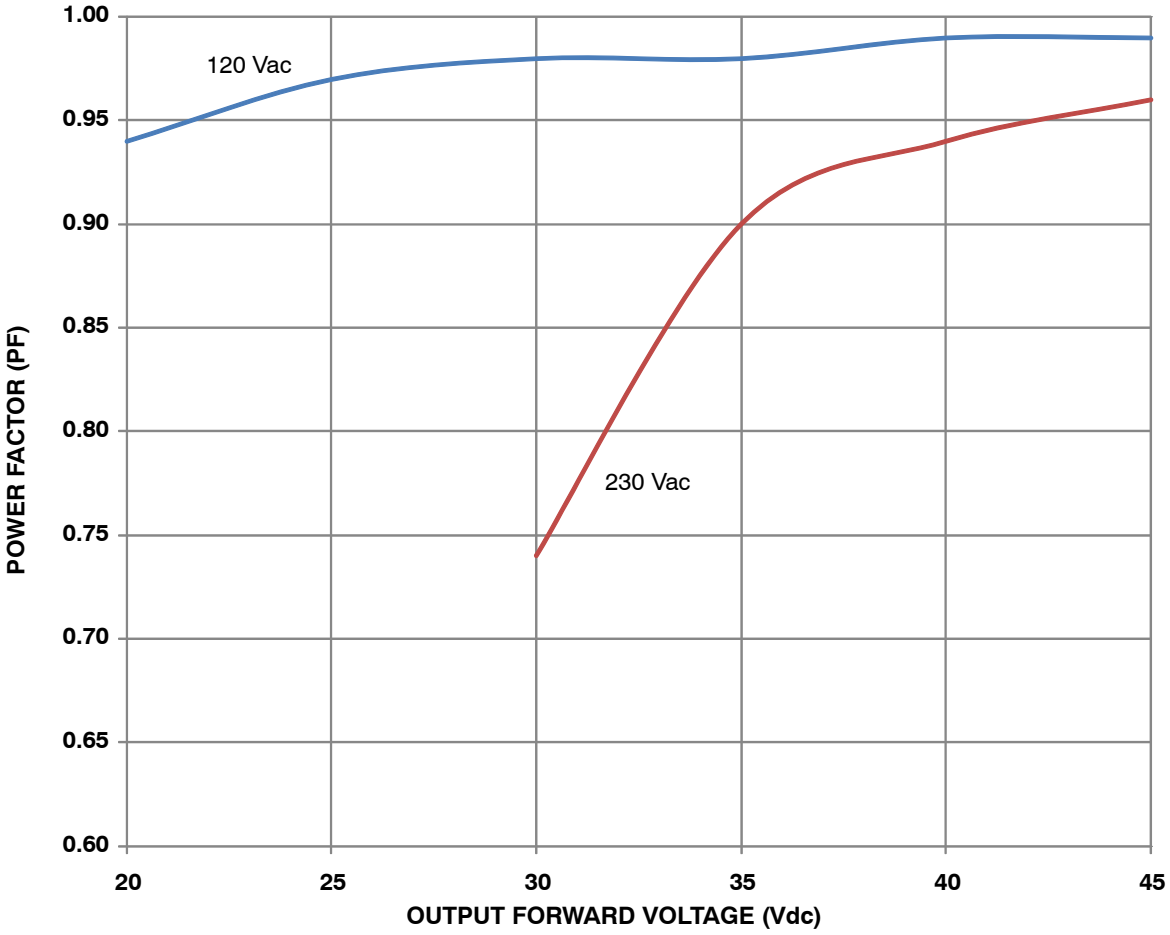


Figure 11. Power Factor versus Forward Voltage (I_{out} = 1 A)

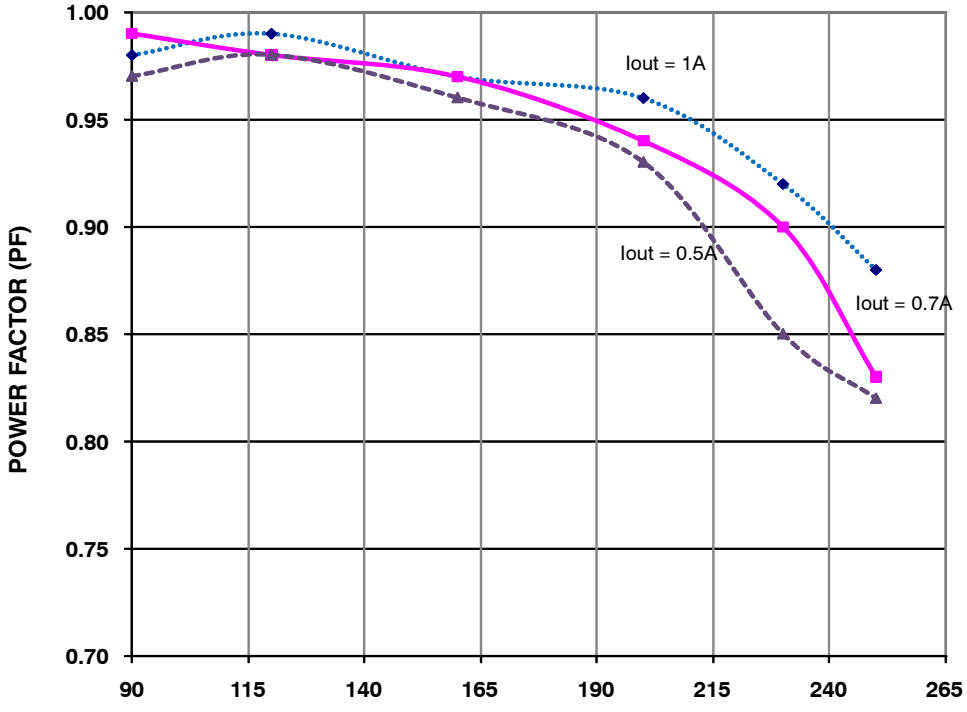


Figure 12. Power Factor versus Output Current

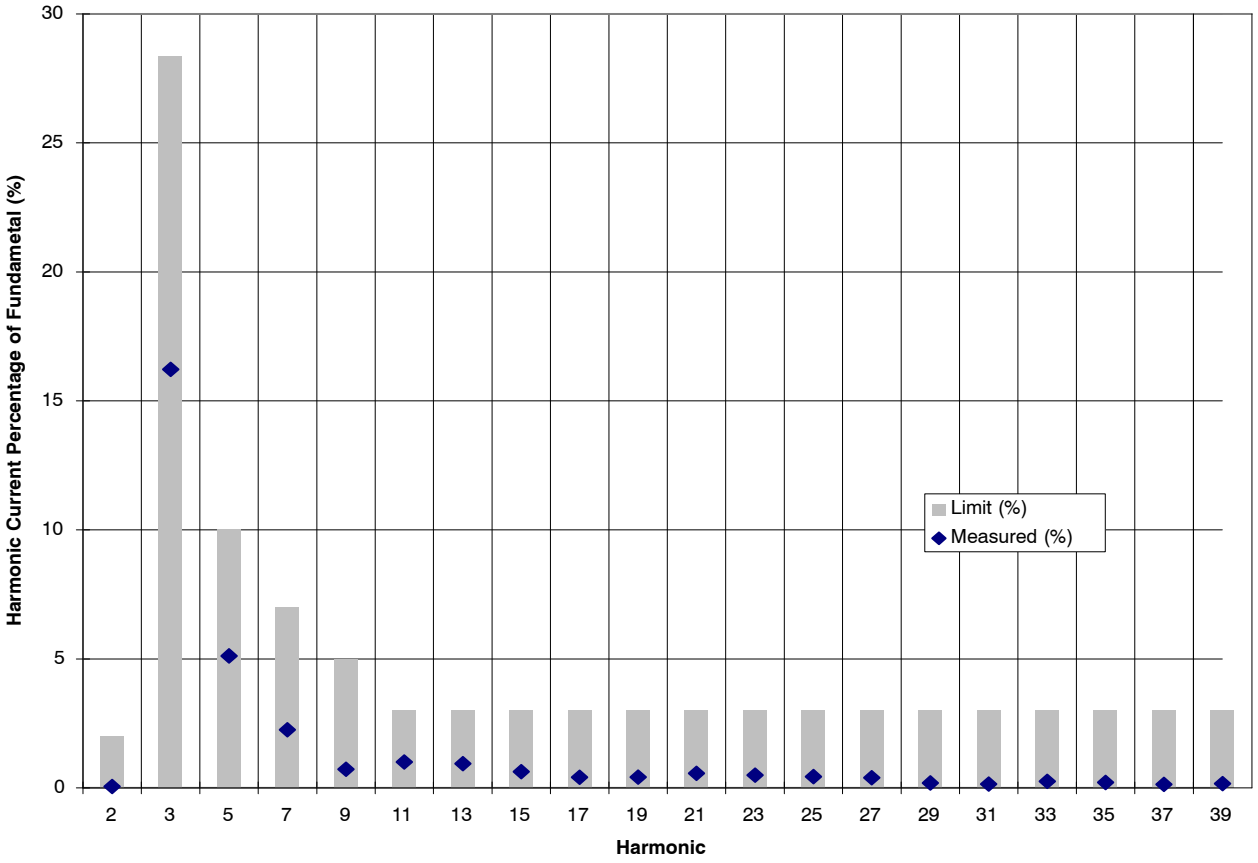


Figure 13. Harmonic Levels (230 Vac input, Full Load)

Dimming Effects on Power Factor and V_f Limits

The power factor is also affected by both analog and PWM dimming and is reduced at lower dimming levels. This is shown in Figure 14.

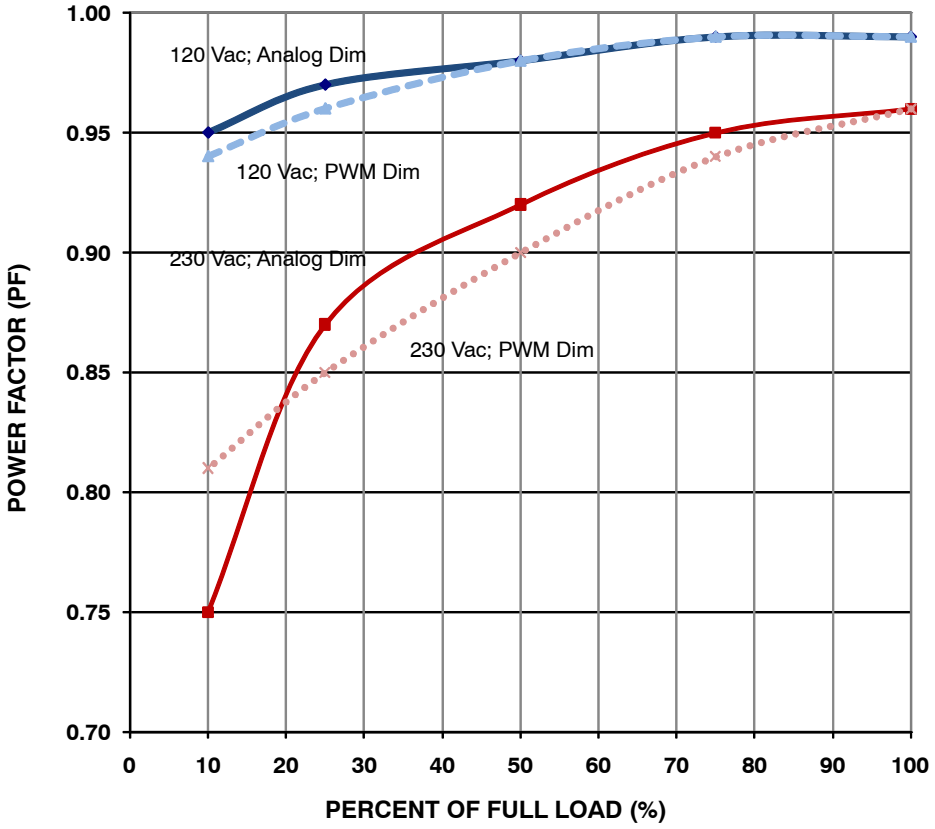


Figure 14. Power Factor versus Dimming

Dimming Limitations

PWM dimming is effective down to less than 5% duty ratio for 120 and 230 Vac within the V_f ranges shown in the graphs of Figure 8 above. It is not recommended to take PWM dimming to zero as this will ultimately result in the power supply going into a start−stop "hiccup" mode due to controller V_{CC} depletion. Analog dimming is limited to 10% (of rated max current) due to depletion of primary circuitry V_{CC}.

Output Ripple

The output current ripple is primarily a function of the amount of bulk capacitance (C4 and C5), and the ripple on the bulk will be reflected to the output by the product of the transformer turns ratio and the half−bridge switch voltage reduction ratio, or, as mentioned previously, 5 x 2 = 10. Since the power factor control loop must have a low bandwidth to produce high power factor, the 120 Hz bulk ripple will naturally be transferred to the output proportionally. In this example, the use of two bulk capacitors of 82 μF in series, giving a total capacitance of 41 μF, was adequate to keep the output current ripple below 10%. Figure 15 shows the output current ripple with an LED string of V_f = 40 V. The magnitude of the ripple is only slightly affected by V_f and line voltage.

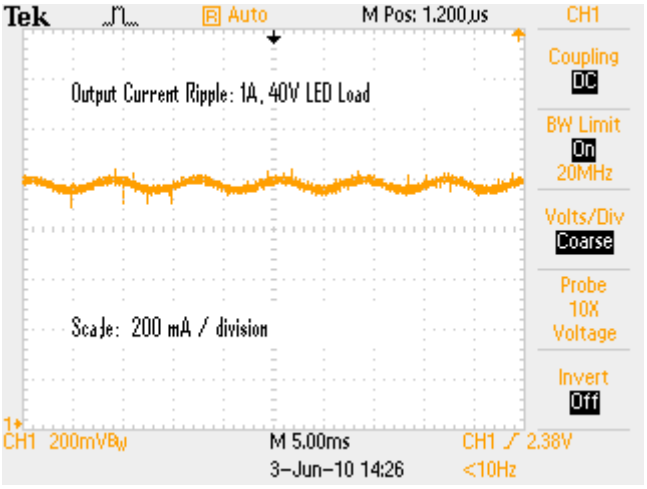


Figure 15. Output Current Ripple at 1 A Load and V_f = 40 Vdc

Output Current Profile at Turn−on

Despite the low control loop bandwidth (approximately 25 Hz), the output current profile during start−up when the ac line is applied is very well controlled from excessive overshoot. The nature of the start−up profile can be tailored by the proper selection of feedback compensation components R23 and C25 around current amplifier U4B. The start−up profile is shown in Figure 16.

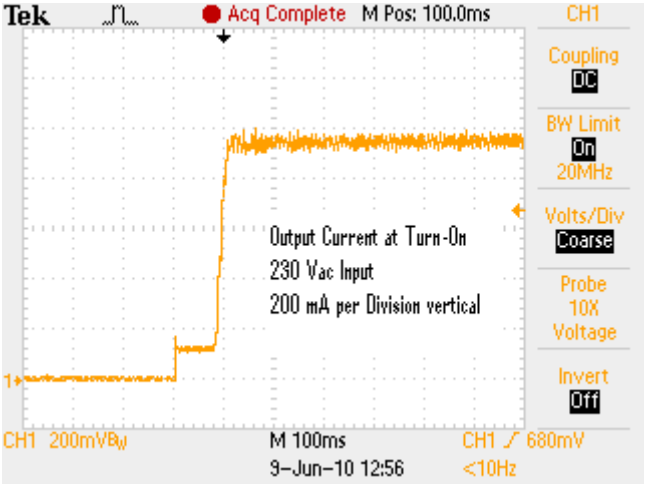


Figure 16. Output Current Profile at Supply Turn−on (230 Vac)

Line Current and Conducted EMI

The prototype supplies were tested for FCC Level A conducted emissions. Waveforms of the input line current at different line voltages and V_f points were also captured. These results are shown in the figures below (Green is peak and red is average).

Figure 17. Conducted EMI Spectrum at 1 A with V_f = 45 V (Red = average)

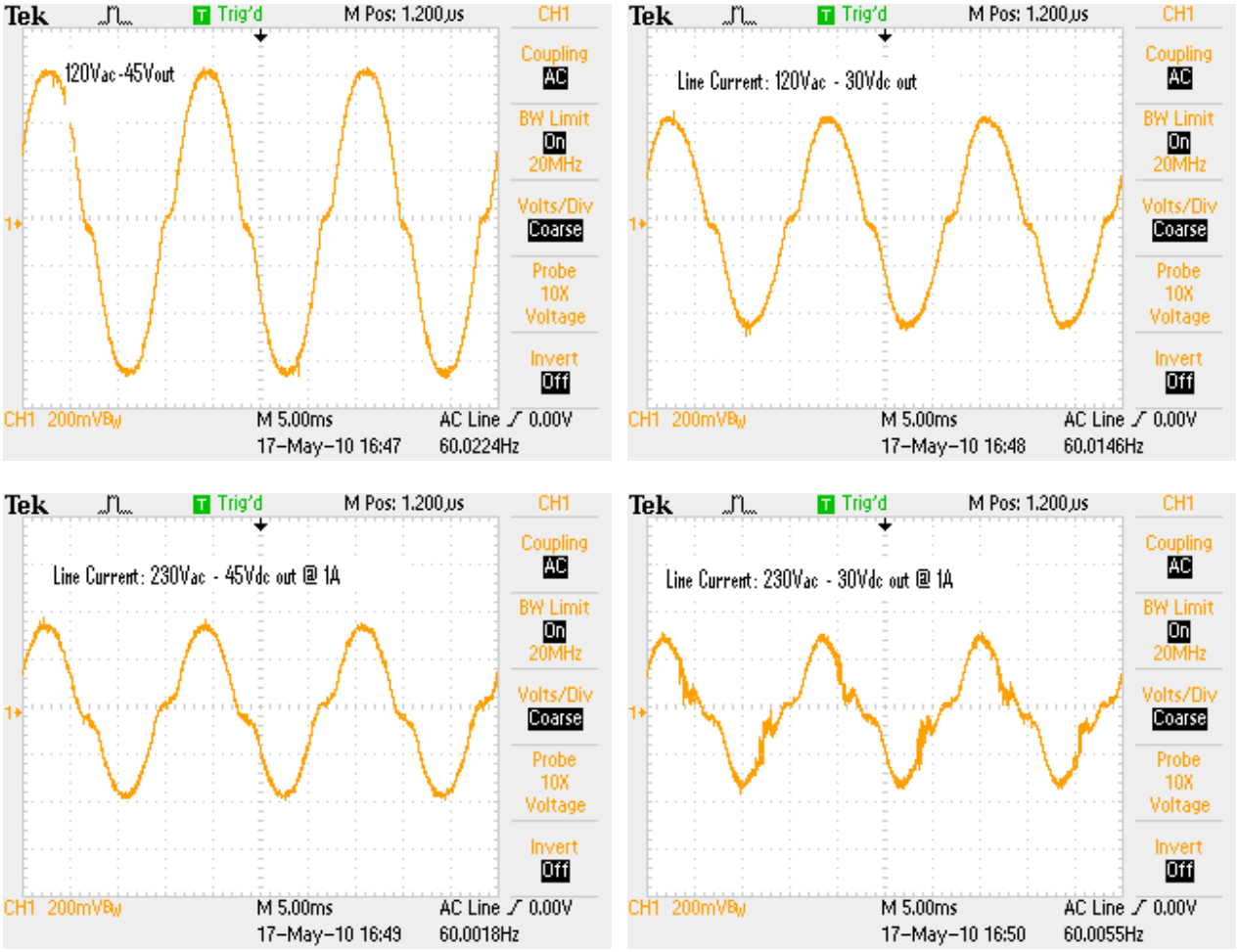


Figure 18. Input Line Current under Different Operating Conditions

CONCLUSIONS

The application note describes the operation of the NCL30051LED Evaluation board and describes the primary design stages including transformer design as well as operational behaviors. This architecture can achieve very high efficiency for LED lighting applications while meeting power factor and harmonic content requirements. The evaluation board is flexible to support a range of LED drive current needs and illustrates different methods to implement dimming

References

1. NCL30051 Data Sheet
2. NCS1002 CVCC controller data sheet
3. ON Semiconductor Application Note AND8470/D
4. ON Semiconductor Application Note AND8427/D
5. ON Semiconductor Design Note DN06068/D

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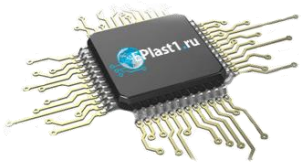

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