# MTCH112

## Dual-Channel Proximity/Touch Controller

### Features:

- Capacitive Proximity Detection System:
  - High Signal to Noise Ratio (SNR)
  - Adjustable sensitivity
  - Noise Rejection Filters
  - Scanning method actively optimized to attenuate strongest noise frequencies
  - Automatic calibration with optional user presets
  - Dynamic threshold management adjusts sensitivity of sensor based on the level of environmental noise
  - Constant press calibration tracks the expected offset when the sensor is pressed and adjusts the threshold to automatically achieve the best press/release behavior
  - User-defined “minimum shift” values specify the lowest amount of signal change to activate a state transition. Automatic thresholds never decrease below these settings.
  - Automatic Environmental Compensation
  - Stuck release mechanism
- No Required External Components
- Low-Power mode: Highly Configurable Low-Power mode
  - 1 ms to 4s Sleep interval between sensor samples
- Response Time as Low as 10 ms
- Hardware Error Detection notifies if either sensor is shorted to VDD, VSS or the other sensor
- Operating Voltage Range:
  - 1.8V to 3.3V
- Operating Temperature:
  - 40°C to +85°C

### Package Type

The device is available in 8-lead SOIC and DFN packaging (see Figure 1).

**FIGURE 1: 8-PIN DIAGRAM FOR MTCH112**

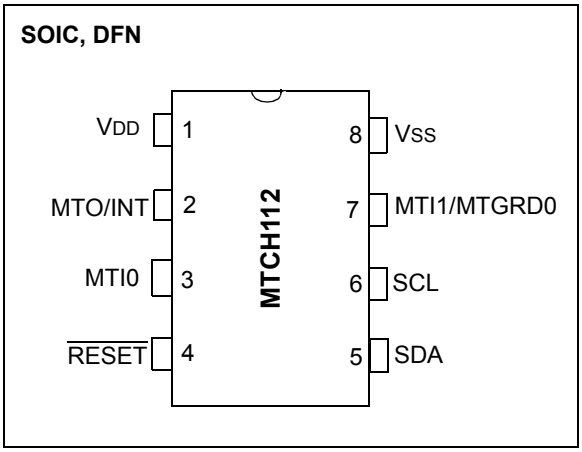


**TABLE 1: 8-PIN SOIC/DFN PINOUT DESCRIPTION**

| I/O | 8-Pin SOIC/DFN | Description |
|---|---|---|
| VDD | 1 | Power Supply Input |
| MTO/INT | 2 | Detect Output (Active-Low) Notification Interrupt Pin |
| MTI0 | 3 | Proximity/Touch Sensor Input |
| $\overline{\text{RESET}}$ | 4 | Device Reset (Active-Low) |
| SDA | 5 | $I^2C$™ Data |
| SCL | 6 | $I^2C$™ Clock |
| MTI1/MTGRD0 | 7 | Proximity/Touch Sensor Input Active Guard Shield for MTI0 |
| VSS | 8 | Ground Reference |

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# 1.0 DEVICE OVERVIEW

The Microchip mTouch™ sensing MTCH112 Dual-Channel Proximity/Touch Controller provides an easy way to add proximity and/or touch sensor detection to any application. The device implements either two capacitive sensors or one sensor and one active guard driver. The optional device configuration through I$^2$C™ allows presets to be loaded in a production environment. Automatic calibration routines are used by default to choose the best options, so user configuration is not required.

The MTCH112 uses a sophisticated optimization algorithm to actively eliminate noise from the signal. While the noise level is being measured, the requirements for a proximity or touch detection are updated to reflect the degree of uncertainty in the readings. When a press is detected for the first time, the threshold is automatically calibrated to choose a smart threshold for the 'release' and next press. This creates a system that dynamically optimizes the signal-to-noise ratio for its environment.

## 1.1 Automatic Calibration

It measures the amount of capacitance on each sensor pin and chooses the best of three possible waveforms to capture a capacitive measurement.

It analyzes the two final settling voltages of the MTI0 pin to more closely match the waveform on the MTGRD0 pin.

The settling time for the waveform is calibrated to maximize sensitivity while minimizing the delay. This provides the best trade-off between signal and noise reduction.

Calibration results are stored in the on-board EEPROM for faster recovery time on next power-up. These memory locations are accessible for read/write through the I$^2$C communications to bypass the automatic calibration, if required.

## 1.2 Communications

- I$^2$C, Slave mode

## 1.3 Touch Configurations

- MTI0 is a dedicated capacitive sensor input
- MTI1/MTGRD0 can either be another capacitive sensor or a guard driver for MTI0

## 1.4 Signal Resolution

- 13 bits

## 1.5 Pin Description

### 1.5.1 MTI0/MTI1

Connect the sensor to this input. An additional resistor of at least 4.7 kΩ is recommended for best noise immunity. Sensors up to 40 pF in capacitance are supported. Sensors work best when the base capacitance is minimized. This will maximize the percentage change in capacitance when a finger is added to the circuit.

### 1.5.2 MTGRD0

When not scanning the pin for capacitance changes (MTI1 functionality), the pin will be driven in phase with MTI0 to minimize the voltage differential between the two pins. If the MTGRD0 pin's trace surrounds the MTI0 pin's trace, the waveform on MTGRD0 will shield (or guard) MTI0 from the effect of nearby noise sources or power planes.

### 1.5.3 MTO

The mTouch™ sensing output pin is always driven to either $V_{DD}$ or $V_{SS}$ by the device. The MTCH112 OUTCON register (see Register 3-1) determines the behavior of the MTO/INT pin. The pin is always active-low, but the states in which this output occurs can be adjusted in the device's OUTCON register. If no options are selected for output states, the MTO pin acts as an interrupt to a master device. The MTCH112 will pulse low for at least 1 ms if any state changes occur. Further information must be determined by communicating through I$^2$C with the device.

### 1.5.4 I$^2$C – SERIAL DATA PIN (SDA)

The SDA pin is the serial data pin of the I$^2$C interface. The SDA pin is used to write or read the registers and Configuration bits. The SDA pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the $V_{DD}$ line to the SDA pin. The recommended resistance value is 1.5 kΩ. Except for Start and Stop conditions, the data on the SDA pin must be stable during the high period of the clock. The high or low state of the SDA pin can only change when the clock signal on the SCL pin is low. Refer to **Section 2.1.2 "I2C Operation"** for more details on I$^2$C Serial Interface communication.

### 1.5.5 I²C – SERIAL CLOCK PIN (SCL)

The SCL pin is the serial clock pin of the I²C interface. The I²C interface only acts as a slave and the SCL pin accepts only external serial clocks. The input data from the master device is shifted into the SDA pin on the rising edges of the SCL clock, and output from the device occurs at the falling edges of the SCL clock. The SCL pin is an open-drain N-channel driver. Therefore, it needs an external pull-up resistor from the $V_{DD}$ line to the SCL pin. The recommended resistance value is 1.5 kΩ. Refer to **Section 2.1.2 "I2C Operation"** for more details on I²C Serial Interface communication.

For more details, see Figure 1 and Table 1.

## 1.6 Performance

### 1.6.1 PROXIMITY DISTANCE

The maximum proximity distance will be highly dependent on the level of noise in the environment. To maximize the robustness of the controller, the noise level is measured and used to define how much shift is required in the signal before a reliable change in state can be determined. These values were taken in a low-noise environment. For more details, see Figure 4-2.

### 1.6.2 RESPONSE TIME

The response time is defined as the maximum amount of time delay between the sensor's capacitance significantly changing and the output being updated based on the OUTCON register's configuration.

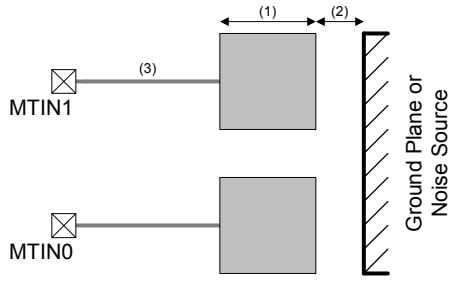
This amount of time will be dependent on the LPCON register, as it determines how long the device will sleep after detecting no significant changes. The fastest response time can be achieved by setting the LPCON register for the minimum Sleep time (see Register 3-6). The controller only sleeps when idle and no changes in the environment are detected. If a change occurs, the device will operate without sleeping until the disturbance or capacitance is removed. For more details, see Table 4-2.

### 1.6.3 HARDWARE

Capacitive sensors are areas of metal connected through a series resistor of 4.7 kΩ to one of the MTIx pins. The following diagrams show some example layout configurations along with the recommended design guidelines. For more information about the design of capacitive sensors, see AN1334, "*Techniques for Robust Touch Sensing Design*".

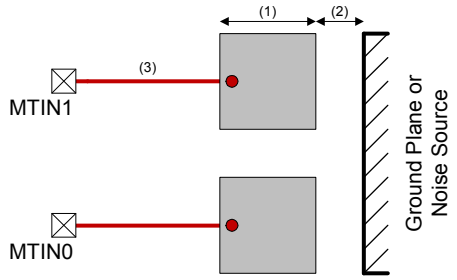
**FIGURE 1-1: TWO-SENSOR LAYOUTS — EXAMPLE**

Single Layer PCB, Two Sensors




**NOTE:** **1:** 15 mm x 15 mm recommended.
**2:** Maximize separation distance.
**3:** Thickness of traces to pin: 0.1 – 0.5 mm

Two Layer PCB, Two Sensors




**NOTE:** **1:** 15 mm x 15 mm recommended.
**2:** Maximize separation distance.
**3:** Thickness of traces to pin: 0.1 – 0.5 mm

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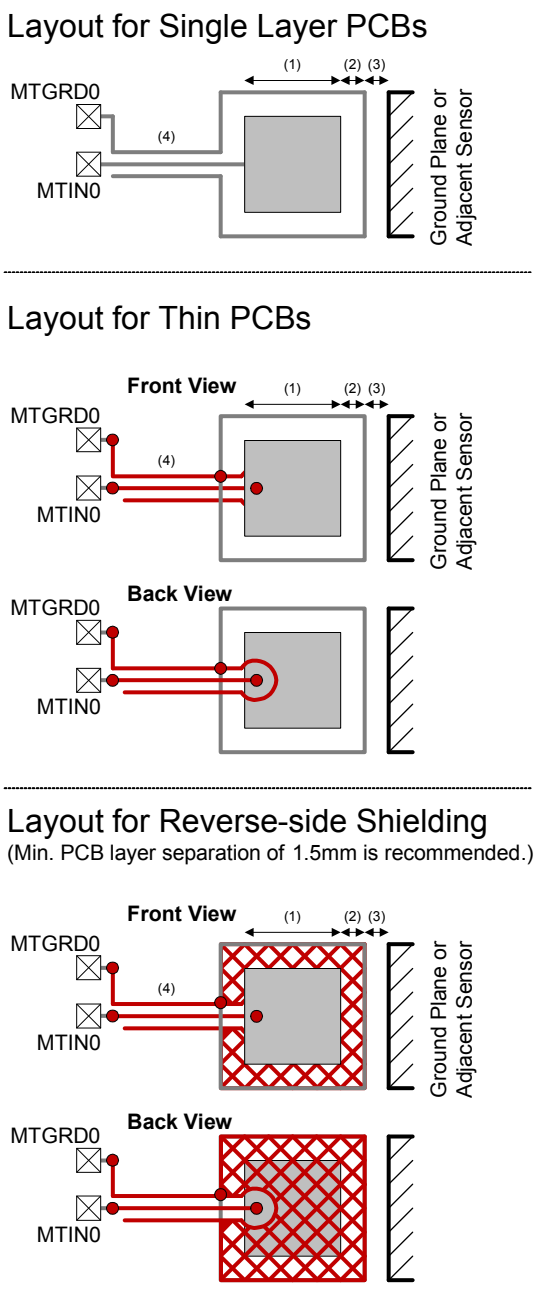
**FIGURE 1-2: GUARD LAYOUTS — EXAMPLE**




**NOTE:**
**1:** 15 mm x 15 mm recommended.
**2:** >2 mm separation recommended.
**3:** >2 mm separation recommended.
**4:** Thickness of traces to pin: 0.1 – 0.5 mm
>0.5 mm separation recommended.
**5:** Thickness of guard around sensor: 1 mm

## 2.0 I²C™ SERIAL INTERFACE

This device supports the I²C serial protocol. The I²C module operates in Slave mode, so it does not generate the serial clock.

### 2.1 Overview

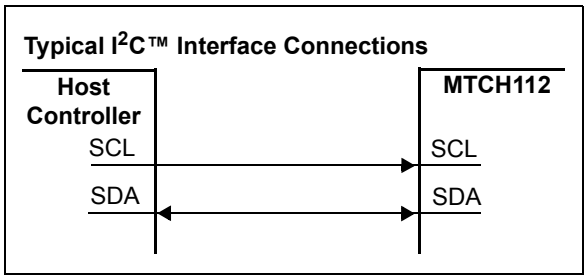
This I²C interface is a two-wire interface. Figure 2-1 shows a typical I²C Interface connection.

The I²C interface specifies different communication bit rates. These are referred to as Standard, Fast or High Speed modes. The MTCH112 device supports these three modes. The bit rates of these modes are:

- Standard Mode: Bit Rates up to 100 kbit/s
- Fast Mode: Bit Rates up to 400 kbit/s

A device that sends data onto the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions. The MTCH112 device works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated. Communication is initiated by the master (microcontroller) which sends the Start bit, followed by the slave address byte. The first byte transmitted is always the slave address byte, which contains the device code, the address bits and the R/$\overline{W}$ bit.

**FIGURE 2-1: TYPICAL I²C™ INTERFACE**




The I²C serial protocol only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. For details on the frame content (commands/data) refer to **Section 2.3 "I2C Commands"**.

Refer to the *NXP User Manual* (UM10204_3) for more details on the I²C specifications.

There was some concern as to the use of the Acknowledge bit to indicate a command error condition. From Section 3.6 of the *NXP User Manual (UM10204_3, Rev 03 - 19 June 2007)*, the description states:

"*The acknowledge takes place after every byte. The Acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses including the acknowledge 9th clock pulse are generated by the master.*"

From this we can state that the byte was not "*successfully received*" since it is an invalid combination of Address/Command.

#### 2.1.1 SIGNAL DESCRIPTIONS

The I²C interface uses up to two pins (signals). These are:

- SDA (Serial Data) (see **Section 1.5.4 "I2C – Serial Data Pin (SDA)"**)
- SCL (Serial Clock) (see **Section 1.5.5 "I2C – Serial Clock Pin (SCL)"**)

#### 2.1.2 I²C OPERATION

The MTCH112 device I²C module is compatible with the NXP I²C specification. The following lists some of the module's features:

- 7-bit Slave Addressing
- Supports Two Clock Rate modes:
  - Standard mode, clock rates up to 100 kHz
  - Fast mode, clock rates up to 400 kHz
- Support Multi-Master Applications

The I²C 10-bit addressing mode is not supported.

The NXP I²C specification only defines the field types, field lengths, timings, etc. of a frame. The frame content defines the behavior of the device. The frame content for this device is defined in **Section 2.3 "I2C Commands"**.

### I²C BIT STATES AND SEQUENCE

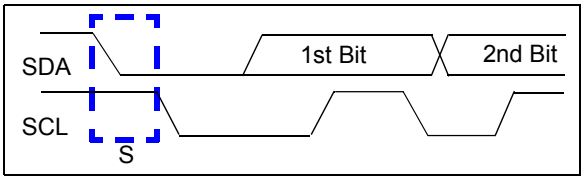
Figure 2-7 shows an I²C 8-bit transfer sequence, while Figure 2-8 shows the bit definitions. The serial clock is generated by the master. The following definitions are used for the bit states:

- Start bit (S)
- Data bit
- Acknowledge (A) bit (driven low) /
  No Acknowledge ($\overline{A}$) bit (not driven low)
- Repeated Start bit (Sr)
- Stop bit (P)

### START BIT

The Start bit (see Figure 2-2) indicates the beginning of a data transfer sequence. The Start bit is defined as the SDA signal falling when the SCL signal is high.

**FIGURE 2-2: START BIT**

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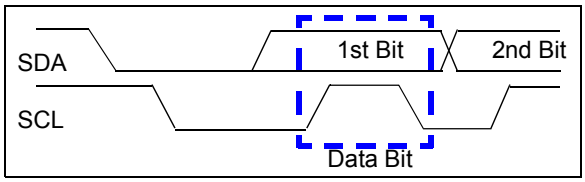
## DATA BIT

The SDA signal may change state while the SCL signal is low. While the SCL signal is high, the SDA signal MUST be stable (see Figure 2-3).

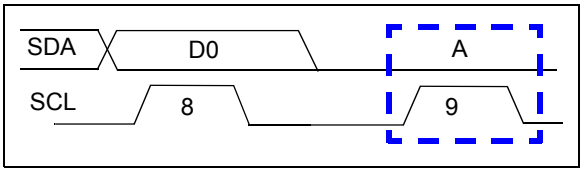
**FIGURE 2-3: DATA BIT**




## ACKNOWLEDGE (A) BIT

The A bit (see Figure 2-4) is typically a response from the receiving device to the transmitting device. Depending on the context of the transfer sequence, the A bit may indicate different things. Typically, the slave device will supply an A response after the Start bit and 8 data bits have been received. An A bit has the SDA signal low.

**FIGURE 2-4: ACKNOWLEDGE WAVEFORM**




### Not A ($\overline{A}$) Response

The $\overline{A}$ bit has the SDA signal high. Table 2-1 shows some of the conditions where the slave device will issue a Not A ($\overline{A}$).

If an error condition occurs (such as an $\overline{A}$ instead of A), then a Start bit must be issued to reset the command state machine.

**TABLE 2-1: MTCH112 A / $\overline{A}$ RESPONSES**

| Event | Acknowledge Bit Response | Comment |
|---|---|---|
| General Call | $\overline{A}$ | |
| Slave Address valid | A | |
| Slave Address not valid | $\overline{A}$ | |
| Communication during EEPROM Write cycle | $\overline{A}$ | The device will NACK after a valid write sequence until all bytes are executed. |
| Bus Collision | N/A | Treated as “Don’t Care” if the collision occurs on the Start bit. Otherwise, $I^2C$™ resets. |

## REPEATED START BIT

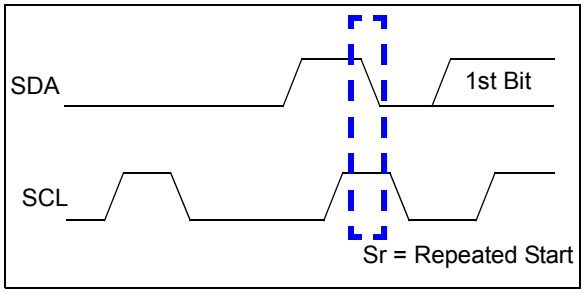
The Repeated Start bit (see Figure 2-5) indicates that the current master device wishes to continue communicating with the current slave device without releasing the I²C bus. The Repeated Start condition is the same as the Start condition, except that the Repeated Start bit follows a Start bit (with the data bits + A bit) and not a Stop bit.

The Start bit is the beginning of a data transfer sequence and is defined as the SDA signal falling when the SCL signal is high.

**Note 1:** A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

**FIGURE 2-5: REPEAT START CONDITION WAVEFORM**

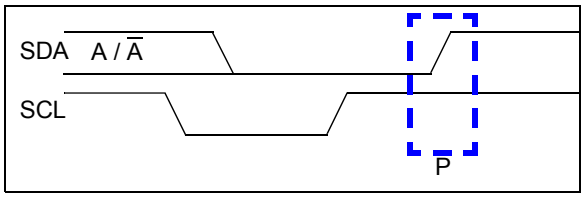



## STOP BIT

The Stop bit (see Figure 2-6) indicates the end of the I²C data transfer sequence. The Stop bit is defined as the SDA signal rising when the SCL signal is high.

A Stop bit resets the I²C interface of the MTCH112 device.

**FIGURE 2-6: STOP CONDITION RECEIVE OR TRANSMIT MODE**




2.1.2.1 Clock Stretching

Clock stretching is something that the receiving device can do to allow additional time to respond to the data that has been received.

This device will stretch the clock signal (SCL) after a Write command to allow the EEPROM write operation to complete.

2.1.2.2 Aborting a Transmission

If any part of the I²C transmission does not meet the command format, it is aborted. This can be intentionally accomplished with a Start or Stop condition. This is done so that noisy transmissions (usually an extra Start or Stop condition) are aborted before they corrupt the device.

**FIGURE 2-7: TYPICAL 8-BIT I²C™ WAVEFORM FORMAT**

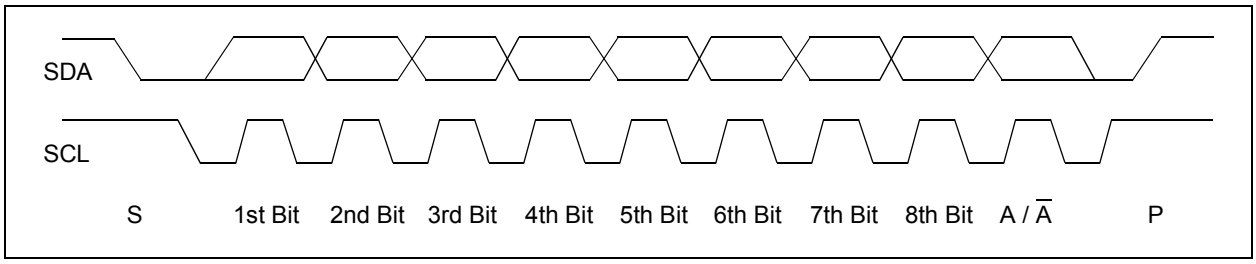
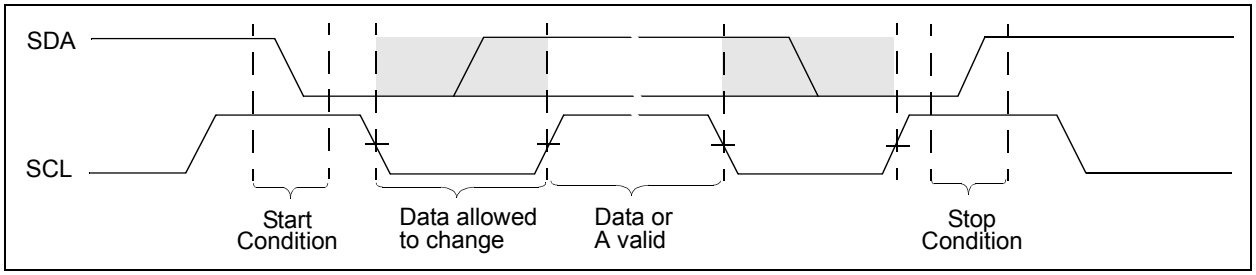



**FIGURE 2-8: I²C™ DATA STATES AND BIT SEQUENCE**

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#### 2.1.2.3 Slope Control

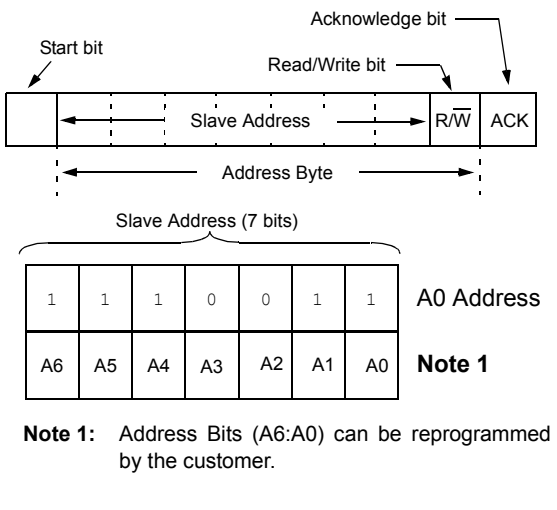
This device does not implement slope control on the SDA output.

#### 2.1.2.4 Device Addressing

The address byte is the first byte received following the Start condition from the master device. The full 7 bits of the $I^2C$ slave address is user programmable. The default address is "`1110011`".

Figure 2-9 shows the $I^2C$ slave address byte format, which contains the seven address bits and a Read/Write (R/$\overline{W}$) bit.

**FIGURE 2-9: SLAVE ADDRESS BITS IN THE $I^2C$™ CONTROL BYTE**




**Note 1:** Address Bits (A6:A0) can be reprogrammed by the customer.

## 2.2 Device Commands

This section documents the commands that the device supports.

The commands can be grouped into the following categories:

- Write Memory
- Read Memory

**TABLE 2-2: RESET TO FACTORY SETTINGS**

| Desc. | Start | Device | Write Protection | | Reset Command | | Checksum(1) | Stop |
|---|---|---|---|---|---|---|---|---|
| **Example** | S | 0xE6 | 0x55 | 0xAA | 0x00 | 0xFF | 0x00 | P |
| **Notes** | — | Write | Required | | Factory Settings | | — | — |

**Note 1:** Checksum is the binary XOR of all bytes except the device address.

**TABLE 2-3: WRITE TO REGISTER**

| Desc. | Start | Device | Write Protection | | Register | Value | Checksum(1) | Stop |
|---|---|---|---|---|---|---|---|---|
| **Example** | S | 0xE6 | 0x55 | 0xAA | 0x01 | 0x01 | 0xFF | P |
| **Notes** | — | Write | Required | | OUTCON | — | — | — |

**Note 1:** Checksum is the binary XOR of all bytes except the device address.

**TABLE 2-4: READ FROM REGISTER**

| Desc. | Start | Device | Register | Restart | Device | Data | Stop | Start | Device | Checksum(1) | Stop |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Example** | S | 0xE6 | 0x80 | S | 0xE7 | — | P | S | 0xE7 | 0xZZ | P |
| **Notes** | | Write | STATE | | Read | — | | | Read | — | |

**Note 1:** Read checksum is the binary XOR of all bytes in the Data column. This is an optional step. The checksum can be ignored if the master does not wish to read it.

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## 2.3 I²C COMMANDS

The I²C protocol does not specify how commands are formatted, so this section specifies the MTCH112 device's I²C command formats and operation.

The commands can be grouped into the following categories:

- Write Commands
- Read Commands

The supported commands are shown in Table 2-2, Table 2-3 and Table 2-4.

### 2.3.1 WRITE COMMANDS

Write commands are used to transfer data to the desired memory location (from the Host controller). The Write command form writes the device address, 0x55, 0xAA, the data address, the value to write and an XOR checksum.

### 2.3.2 READ COMMANDS

The Read command format writes two bytes, the control byte and the desired memory address byte, and then has a Restart condition. Then a second control byte is transmitted, but this control byte indicates a I²C read operation (R/$\overline{W}$ bit = `1`).

### 2.3.3 RESET TO FACTORY SETTINGS COMMAND

Resetting the device to factory settings is equivalent to writing the value 0xFF to the data address `0x00`. The proper write protocol must be followed, including the address byte with the Write bit set, 0x55, 0xAA and a binary XOR checksum at the end.

### 2.3.4 ABORTING A COMMAND TRANSMISSION

A Restart or Stop condition in an expected data bit position will abort the current command sequence and data will not be written to the MTCH112. Write commands are automatically aborted if the binary XOR checksum is not valid.

### 2.3.5 WRITE COMMAND (NORMAL AND HIGH VOLTAGE)

The format of the command is shown in Figure 2-10. The MTCH112 generates the A/$\overline{A}$ bits.

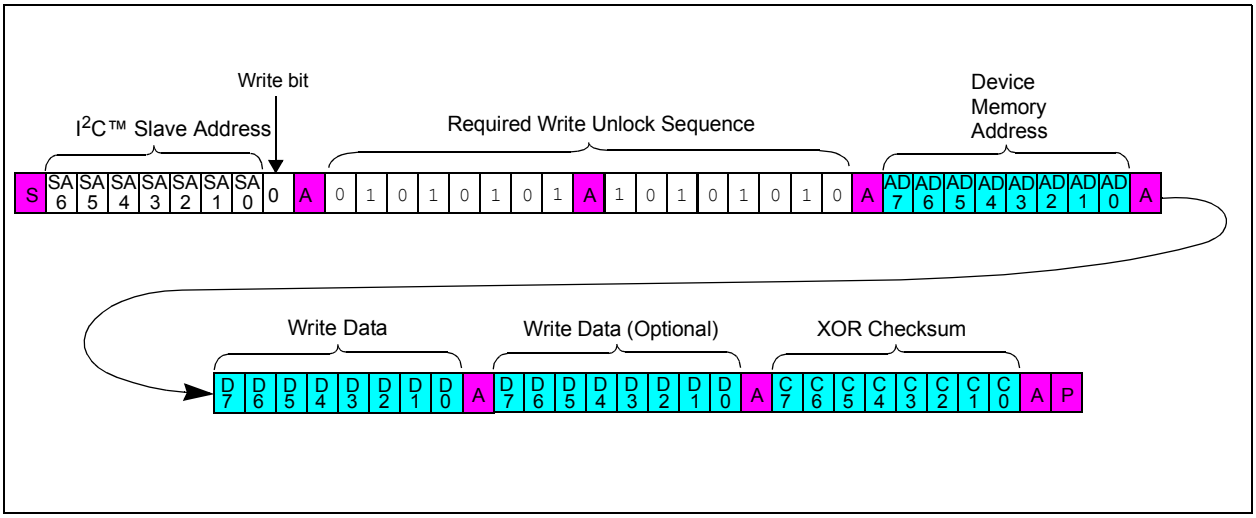
A Write command will only start a Write cycle after a properly formatted Write command has been received and the Stop condition has occurred.

#### 2.3.5.1 Writing to Memory

The protocol allows for a variable number of bytes to be written to the device at a time. Once the Stop bit has been sent, a time delay is required while the EEPROM write cycle stores each data byte. While the device is writing the EEPROM, the address will be changed (by toggling the Least Significant address bit of the device, then toggling back once finished) to prevent accidental double writes. An error may occur if a Write command is sent while the EEPROM is still storing the previous bytes. While the writing is being performed, reads to the normal device address will result in a NACK.

Figure 2-10 shows the waveform for a single write.

**FIGURE 2-10: WRITE RANDOM ADDRESS COMMAND**



### 2.3.6 READ COMMAND

The Read command can be issued to all memory locations. The format of the command (see Figure 2-11) includes the Start condition, I²C control byte (with R/$\overline{W}$ bit set to 0), A bit, the data address byte, A bit, followed by a Repeated Start bit, I²C control byte (with R/$\overline{W}$ bit set to 1) and the MTCH112 device transmitting the requested data bytes one at a time until the master sends a Stop condition.

The I²C control byte requires the R/$\overline{W}$ bit equal to a logic one (R/$\overline{W}$ = 1) to generate a read sequence. The memory location read will start at the requested data address and automatically increments by one after each byte request. Notice that the read operation packets do not include the 0x55 and 0xAA Write protection bytes.

After the Stop condition has been received, if a Start condition is followed by the device address, the device will send the XOR checksum of the data bytes from the previous read packet. This allows the checksum to be ignored by the master, if desired.

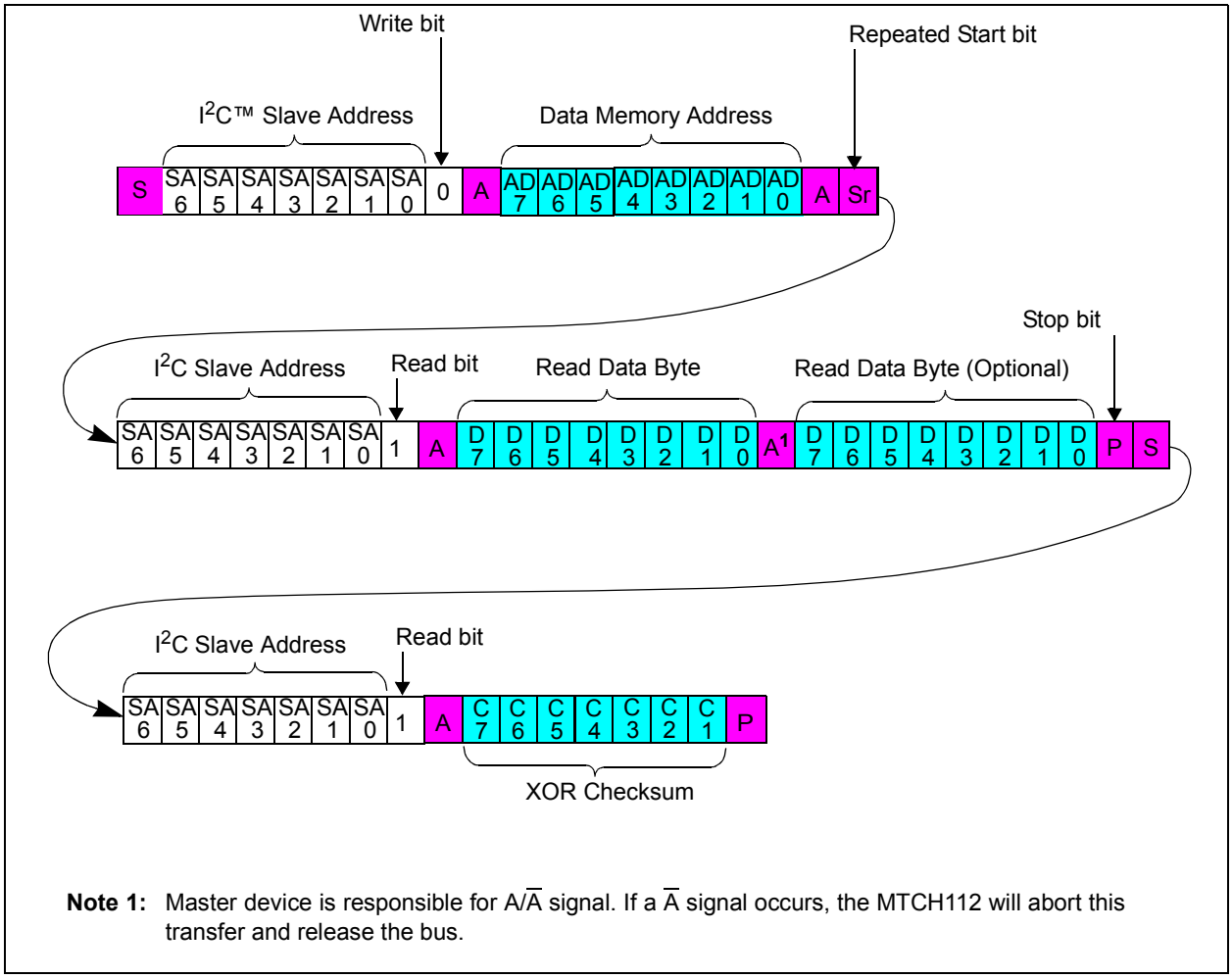
Read operations initially include the same address byte sequence as the write sequence (shown in Figure 2-10). This sequence is followed by another control byte (including the Start condition and Acknowledge) with the R/$\overline{W}$ bit equal to a logic one (R/$\overline{W}$ = 1) to indicate a read. The MTCH112 will then transmit the data contained in the addressed register. This is followed by the master generating an A bit in preparation for more data, or an $\overline{A}$ bit followed by a Stop. The sequence is ended with the master generating a Stop or Restart condition.

Figure 2-11 shows the waveforms for a single read.

#### 2.3.6.1 Ignoring an I²C Transmission and "Falling Off" the Bus

The MTCH112 device expects to receive complete, valid I²C commands and will assume any command not defined as a valid command is due to a bus corruption and will enter a passive high condition on the SDA signal. All signals will be ignored until the next valid Start condition and control byte are received.

**FIGURE 2-11: RANDOM READ COMMAND**




**Note 1:** Master device is responsible for A/$\overline{A}$ signal. If a $\overline{A}$ signal occurs, the MTCH112 will abort this transfer and release the bus.

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## 3.0 CONFIGURATION REGISTERS

The registers in the MTCH112 have been organized in two groups: the Configuration registers and the output registers. The output registers are in the `0x80` (and higher) address range and are read-only. They provide the current sensor data for each input. The Configuration registers are both writable and readable. They show the current scan options and define the systems behavior.

To restore the Configuration registers to their default states and force a recalibration of the sensors, perform a write operation of 0xFF to address `0x00`.

### 3.1 Output Control Register (OUTCON)

This register contains the control bits for the MTO/INT pin to determine its behavior. If multiple bits in this register are set, the states they represent are ORd before the output is determined. For example, if the S1BOE and S0BOE bits are set, the MTO pin will output low if either MTI0 or MTI1 detect a button touch. If the S1POE and S0POE bits are set, the MTO pin will output low if either MTI0 or MTI1 make a proximity detection. If none of the bits are set, the pin will perform as a 1 ms pulsed interrupt pin for the $I^2C$ master. (see Register 3-1)

**REGISTER 3-1: OUTCON: OUTPUT CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0/u | R/W-0/u | R/W-1/u | R/W-1/u |
|---|---|---|---|---|---|---|---|
| — | — | — | — | S1POE(1) | S0POE(1) | S1BOE(1) | S0BOE(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-4 **Unimplemented:** Read as ‘`0`’

bit 3 **S1POE:** Sensor 1 Proximity Output Enable bit
`1` = Output pin activates when Sensor 1 makes a proximity detection
`0` = Output pin does not change based on Sensor 1’s proximity detection

bit 2 **S0POE:** Sensor 0 Proximity Output Enable bit
`1` = Output pin activates when Sensor 0 makes a proximity detection
`0` = Output pin does not change based on Sensor 0’s proximity detection

bit 1 **S1BOE:** Sensor 1 Button Output Enable bit
`1` = Output pin activates when Sensor 1 makes a button press detection
`0` = Output pin does not change based on Sensor 1’s button press detection

bit 0 **S0BOE:** Sensor 0 Button Output Enable bit
`1` = Output pin activates when Sensor 0 makes a button press detection
`0` = Output pin does not change based on Sensor 0’s button press detection

**Note 1:** If all output enable bits are ‘`0`’, the output pin will behave as a wake-up signal to the master. It will be set active-low whenever new data becomes available.

## 3.2 Calibration Control Registers (CALCONx)

This register contains the calibration information for MTIx. It stores the chosen waveform type and whether or not the calibration has been completed. To recalibrate a sensor, clear its respective SxCAL bit in the CALCONx register (see Register 3-2 and Register 3-3).

**REGISTER 3-2: CALCON0: SENSOR 0'S CALIBRATION CONTROL REGISTER**

| R/W-0/u | R/W-0/u | U-0 | U-0 | U-0 | U-0 | R/W-0/u | U-1 |
|---|---|---|---|---|---|---|---|
| S0WS<1:0> | | — | — | — | — | S0CAL | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-6 **S0WS<1:0>:** Sensor 0 Waveform Selection bits
00 = Normal mTouch™ sensing CVD Waveform
01 = Double mTouch™ sensing CVD Waveform
10 = Half mTouch™ sensing CVD Waveform
11 = Reserved. Results in Double mTouch™ sensing CVD Waveform

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **S0CAL:** Sensor 0 Calibrated bit
1 = Sensor 0 calibration complete
0 = New Sensor 0 calibration requested

bit 0 **Unimplemented:** Read as '0'

**REGISTER 3-3: CALCON1: SENSOR 1'S CALIBRATION CONTROL REGISTER**

| R/W-0/u | R/W-0/u | U-0 | U-0 | U-0 | U-0 | R/W-0/u | R/W-1/u |
|---|---|---|---|---|---|---|---|
| S1WS<1:0> | | — | — | — | — | S1CAL | S1EN |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-6 **S1WS<1:0>:** Sensor 1 Waveform Selection bits
00 = Normal mTouch™ sensing CVD Waveform
01 = Double mTouch™ sensing CVD Waveform
10 = Half mTouch™ sensing CVD Waveform
11 = Reserved. Results in Double mTouch™ sensing CVD Waveform

bit 5-2 **Unimplemented:** Read as '0'

bit 1 **S1CAL:** Sensor 1 Calibrated bit
1 = Sensor 1 calibration complete
0 = New Sensor 1 calibration requested

bit 0 **S1EN:** Sensor 1 Enabled bit
1 = Sensor 1 is enabled. Scanning and decoding active.
0 = Sensor 1 is disabled. No scanning or decoding is performed.

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## 3.3 ADC Acquisition Time Registers (ADACQx)

This stores the settling delay time for the CVD waveform. This value is part of the recalibration process and will be overwritten if the SxCAL bit is cleared (see Register 3-4 and Register 3-5).

**REGISTER 3-4: ADACQ0: SENSOR 0'S ACQUISITION DELAY**

| U-0 | U-0 | U-0 | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u |
|---|---|---|---|---|---|---|---|
| — | — | — | S0ACQ<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **S0ACQ<4:0>:** Sensor 0 Acquisition Delay bits

**REGISTER 3-5: ADACQ1: SENSOR 1'S ACQUISITION DELAY**

| U-0 | U-0 | U-0 | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u |
|---|---|---|---|---|---|---|---|
| — | — | — | S1ACQ<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-5 **Unimplemented:** Read as '0'

bit 4-0 **S1ACQ<4:0>:** Sensor 1 Acquisition Delay bits

## 3.4 Low-Power Control Register (LPCON)

This register provides the low-power options for the MTCH112. It determines how long the device will sleep when no detections have been made, and how fast the internal oscillator will run. If the CLKSEL bit is set, the valid VDD operating range will decrease. See the bit description in Register 3-6 for more information.

**REGISTER 3-6: LPCON: LOW-POWER CONTROL REGISTER**

| U-0 | U-0 | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-1/u | R/W-1/u |
|---|---|---|---|---|---|---|---|
| — | — | SLEEP<4:0> | | | | | CLKSEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-1 **SLEEP<4:0>:** Sleep duration between scans when inactive
00000 = 1 ms, typical sleep duration
00001 = 2 ms, typical sleep duration
00010 = 4 ms, typical sleep duration
00011 = 8 ms, typical sleep duration
00100 = 16 ms, typical sleep duration
00101 = 32 ms, typical sleep duration
00110 = 64 ms, typical sleep duration
00111 = 128 ms, typical sleep duration
01000 = 256 ms, typical sleep duration
01001 = 512 ms, typical sleep duration
01010 = 1 sec, typical sleep duration
01011 = 2 sec, typical sleep duration
01100 = 4 sec, typical sleep duration
01101 = 8 sec, typical sleep duration
01110 = 16 sec, typical sleep duration
01111 = 32 sec, typical sleep duration
10000 = 64 sec, typical sleep duration
10001 = 128 sec, typical sleep duration
10010 = 256 sec, typical sleep duration

10011 = Reserved. Results in 1 ms sleep duration.
. . .
11111 = Reserved. Results in 1 ms sleep duration.

bit 0 CLKSEL: Oscillator Selection bit
1 = Internal oscillator runs at 32 MHz
Decreases response time
Increases power consumption
Valid VDD operating range when selected is 2.5V-3.6V
0 = Internal oscillator runs at 16 MHz
Decreases response time
Increases power consumption
Valid VDD operating range when selected is 1.8V-3.6V

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## 3.5 Press Threshold Register (PRESS_THRESH)

The register stores the minimum shift amount of the signal away from the baseline that is required to activate a sensor as "*touched*". The real-time threshold of the sensor is handled internally, based on current noise levels and the expected press amount. This value simply creates a lower bound. It is not mandatory unless the user wishes to ensure that the sensor is not too sensitive in low-noise environments (see Register 3-7).

**REGISTER 3-7: PRESS_THRESH: PRESS THRESHOLD REGISTER**

| R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u |
|---|---|---|---|---|---|---|---|
| PRESS_THSH<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-0 **PRESS_THSH<7:0>:** Absolute Minimum Press Threshold

## 3.6 Proximity Threshold Register (PROX_THRESH)

This register is identical to the Press Threshold register, except that it relates to the proximity detection. Increase this value to decrease the sensitivity of the sensor in low-noise environments (see Register 3-8).

**REGISTER 3-8: PROX_THRESH: PROXIMITY THRESHOLD REGISTER**

| R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u |
|---|---|---|---|---|---|---|---|
| PROX_THSH<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-0 **PROX_THSH<7:0>:** Absolute Minimum Proximity Threshold

## 3.7 16-bit Time-Out Register (TIMEOUT_L and TIMEOUT_H)

This set of registers determines how long the 'detected' state is able to remain activated before automatically being reset to a non-detected state. It also determines how long after no changes in the environment have occurred before setting the controller to its Idle state. When in Idle state, the system will sleep (see Register 3-6) between each reading (see Register 3-9 and Register 3-10).

**REGISTER 3-9: TIMEOUT_L: TIME-OUT COUNTER, LOW BYTE REGISTER**

| R/W-1/u | R/W-1/u | R/W-1/u | R/W-1/u | R/W-1/u | R/W-1/u | R/W-1/u | R/W-1/u |
|---|---|---|---|---|---|---|---|
| TIMEOUT<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-0 **TIMEOUT<7:0>:** Time-out Counter Reload Value, Low Byte

**REGISTER 3-10: TIMEOUT_H: TIME-OUT COUNTER, HIGH BYTE REGISTER**

| R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-0/u | R/W-1/u |
|---|---|---|---|---|---|---|---|
| TIMEOUT<15:8> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as '0' | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| '1' = Bit is set | '0' = Bit is cleared | W = Writable bit |

bit 7-0 **TIMEOUT<15:8>:** Time-out Counter Reload Value, High Byte

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## 3.8 I²C Address Register (I²CADDR)

This register determines the I²C address of the slave. After writing to this register, command immediately should begin using the new address value (see Register 3-11).

### Register 3-11: I²CADDR: I²C™ Address Register

| R/W-1/u | R/W-1/u | R/W-1/u | R/W-0/u | R/W-0/u | R/W-1/u | R/W-1/u | U-1 |
|---|---|---|---|---|---|---|---|
| I²CADDR<7:1> | | | | | | | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-1 **I²CADDR<7:1>:** I²C Address for communication with the MTCH112.

bit 0 **Unimplemented:** Read as ‘0’

## 3.9 State Register (STATE)

This register is read-only. It contains the current touch and proximity state of MTI0 and MTI1, and provides error information if a short is detected on any MTIx pin to VDD, VSS or the other MTIx pin (see Register 3-12).

**REGISTER 3-12: STATE: CURRENT SENSOR STATE REGISTER**

| U-0 | R-0/x | R-0/x | R-0/x | R-0/x | R-0/x | R-0/x | R-0/x |
|---|---|---|---|---|---|---|---|
| — | ERRSTATE<2:0> | | | S1PS | S0PS | S1BS | S0BS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **ERRSTATE<2:0>:** Error Status Information bits
000 = Both sensors floating correctly
001 = Sensor 0 is shorted to VDD
010 = Sensor 1 is shorted to VDD
011 = Sensor 0 is shorted to VSS
100 = Sensor 1 is shorted to VSS
101 = Sensors are shorted together
110 = Reserved
111 = Reserved

bit 3 **S1PS:** Sensor 1 Proximity Status bit
1 = Proximity detected on Sensor 1
0 = No proximity detected on Sensor 1

bit 2 **S0PS:** Sensor 0 Proximity Status bit
1 = Proximity detected on Sensor 0
0 = No proximity detected on Sensor 0

bit 1 **S1BS:** Sensor 1 Button Status bit
1 = Button press detected on Sensor 1
0 = No button press detected on Sensor 1

bit 0 **S0BS:** Sensor 0 Button Status bit
1 = Button press detected on Sensor 0
0 = No button press detected on Sensor 0

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## 3.10 Reading Registers (READINGxL and READINGxH)

These registers contain the current raw value of the MTIx pins. They are 13-bit values, but it is recommended to treat them as 16-bit values to more easily support future designs (see Register 3-13 to Register 3-16).

### REGISTER 3-13: READING0L: SENSOR 0 READING VALUE, LOW BYTE

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| READING0L<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-0 **READING0L<7:0>:** Sensor 0 Current Reading Value, Low Byte

### REGISTER 3-14: READING0H: SENSOR 0 READING VALUE, HIGH BYTE

| U-0 | U-0 | U-0 | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| — | — | — | READING0H<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **READING0H<4:0>:** Sensor 0 Current Reading Value, High Byte

### REGISTER 3-15: READING1L: SENSOR 1 READING VALUE, LOW BYTE

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| READING1L<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-0 **READING1L<7:0>:** Sensor 1 Current Reading Value, Low Byte

**REGISTER 3-16: READING1H: SENSOR 1 READING VALUE, HIGH BYTE**

| U-0 | U-0 | U-0 | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| — | — | — | READING1H<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **READING1H<4:0>:** Sensor 1 Current Reading Value, High Byte

## 3.11 Baseline Registers (BASELINExL and BASELINExH)

These registers contain the current baseline value of the MTIx pins. They are 13-bit values, but it is recommended to treat as unsigned 16-bit values to more easily support future designs (see Register 3-17 to Register 3-20).

**REGISTER 3-17: BASELINE0L: SENSOR 0 BASELINE VALUE, LOW BYTE**

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| BASELINE0L<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-0 **BASELINE0L<7:0>:** Sensor 0 Current Baseline Value, Low Byte

**REGISTER 3-18: BASELINE0H: SENSOR 0 BASELINE VALUE, HIGH BYTE**

| U-0 | U-0 | U-0 | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| — | — | — | BASELINE0H<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **BASELINE0H<4:0>:** Sensor 0 Current Baseline Value, High Byte

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### REGISTER 3-19: BASELINE1L: SENSOR 1 BASELINE VALUE, LOW BYTE

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| BASELINE1L<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-0 **BASELINE1L<7:0>:** Sensor 1 Current Baseline Value, Low Byte

### REGISTER 3-20: BASELINE1H: SENSOR 1 BASELINE VALUE, HIGH BYTE

| U-0 | U-0 | U-0 | R-x | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| — | — | — | BASELINE1H<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---|---|---|
| R = Readable bit | U = Unimplemented bit, read as ‘0’ | |
| u = Bit is unchanged | -n/n = Factory setting value/Value after all Resets | |
| ‘1’ = Bit is set | ‘0’ = Bit is cleared | W = Writable bit |

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **BASELINE1H<4:0>:** Sensor 1 Current Baseline Value, High Byte

**TABLE 3-1: REGISTER MAPPING**

| Address | Name | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | — | — | — | — | — | — | — | — | — |
| 0x01 | OUTCON | — | — | — | — | S1POE | S0POE | S1BOE | S0BOE |
| 0x02 | CALCON0 | S0WS | | — | — | — | — | S0CAL | — |
| 0x03 | CALCON1 | S1WS | | — | — | — | — | S1CAL | S1EN |
| 0x04 | ADACQ0 | | | | S0ACQ<4:0> | | | | |
| 0x05 | ADACQ1 | | | | S1ACQ<4:0> | | | | |
| 0x06 | LPCON | | | SLEEP<4:0> | | | | | CLKSEL |
| 0x07 | PRESS_THRESH | PRESS_THSH<7:0> | | | | | | | |
| 0x08 | PROX_THRESH | PROX_THSH<7:0> | | | | | | | |
| 0x09 | TIMEOUT_L | TIMEOUT<7:0> | | | | | | | |
| 0x0A | TIMEOUT_H | TIMEOUT<15:8> | | | | | | | |
| 0x0B | $I^2CADDR$ | $I^2CADDR$<7:1> | | | | | | | — |
| 0x0C | — | — | — | — | — | — | — | — | — |
| 0x0D | — | — | — | — | — | — | — | — | — |
| 0x0E | — | — | — | — | — | — | — | — | — |
| 0x0F | — | — | — | — | — | — | — | — | — |
| 0x80 | STATE | — | ERRSTATE<2:0> | | | S1PS | S0PS | S1BS | S0BS |
| 0x81 | READING0L | READING0L<7:0> | | | | | | | |
| 0x82 | READING0H | — | — | — | READING0H<4:0> | | | | |
| 0x83 | READING1L | READING1L<7:0> | | | | | | | |
| 0x84 | READING1H | — | — | — | READING1H<4:0> | | | | |
| 0x85 | BASELINE0L | BASE0L<7:0> | | | | | | | |
| 0x86 | BASELINE0H | — | — | — | BASE0H<4:0> | | | | |
| 0x87 | BASELINE1L | BASE1L<7:0> | | | | | | | |
| 0x88 | BASELINE1H | — | — | — | BASE1H<4:0> | | | | |

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## 4.0 ELECTRICAL SPECIFICATIONS

### Absolute Maximum Ratings(†)

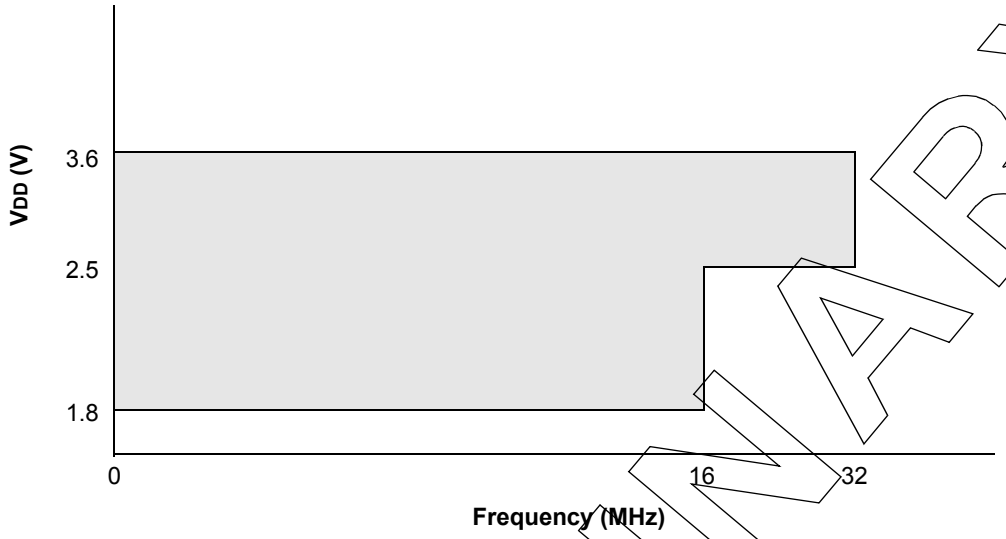
Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on $\overline{MCLR}$ with respect to Vss ..... -0.3V to +9.0V
Voltage on all other pins with respect to $V_{SS}$ ..... -0.3V to ($V_{DD}$ + 0.3V)
Total power dissipation(1) ..... 800 mW
Maximum current out of $V_{SS}$ pin, -40°C ≤ $T_A$ ≤ +85°C for industrial ..... 85 mA
Maximum current into $V_{DD}$ pin, -40°C ≤ $T_A$ ≤ +85°C for industrial ..... 80 mA
Clamp current, $I_K$ ($V_{PIN}$ < 0 or $V_{PIN}$ > $V_{DD}$) ..... ± 20 mA
Maximum output current sunk by any I/O pin ..... 25 mA
Maximum output current sourced by any I/O pin ..... 25 mA

**Note 1:** Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum\{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$.

† **NOTICE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

**FIGURE 4-1: VOLTAGE FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**




**Note 1:** The shaded region indicates the permissible combinations of voltage and frequency.

## 4.1 DC Characteristics: MTCH112

| MTCH112 | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| D001 | VDD | **Supply Voltage** | 1.8<br>2.5 | —<br>— | 3.6<br>3.6 | V<br>V | CLKSEL = 0<br>CLKSEL = 1 |
| D002* | VDR | **RAM Data Retention Voltage** (1) | 1.5 | — | — | V | Device in Sleep mode |
| | VPOR* | **Power-on Reset Release Voltage** | — | 1.6 | — | V | |
| | VPORR* | **Power-on Reset Rearm Voltage** | — | 0.8 | — | V | Device in Sleep mode |
| D004* | SVDD | **VDD Rise Rate** to ensure internal Power-on Reset signal | 0.05 | — | — | V/ms | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

PRELIMINARY

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**TABLE 4-1: CURRENT CONSUMPTION**

| CLKSEL | Sleep (s) | 1.8V | 3.0V | CLKSEL | Sleep (s) | 3.0V | 3.6V |
|---|---|---|---|---|---|---|---|
| | | Typ. (uA) | Typ. (uA) | | | Typ. (uA) | Typ. (uA) |
| **16 MHz** | **0** | 640 | 990 | **32 MHz** | **0** | 1952 | 2350 |
| | **0.001** | 580 | 900 | | **0.001** | 1780 | 2140 |
| | **0.002** | 540 | 830 | | **0.002** | 1630 | 1970 |
| | **0.004** | 460 | 710 | | **0.004** | 1400 | 1690 |
| | **0.008** | 360 | 560 | | **0.008** | 1090 | 1320 |
| | **0.016** | 250 | 390 | | **0.016** | 760 | 915 |
| | **0.032** | 160 | 240 | | **0.032** | 470 | 570 |
| | **0.064** | 89 | 140 | | **0.064** | 270 | 320 |
| | **0.128** | 48 | 74 | | **0.128** | 150 | 170 |
| | **0.256** | 25 | 38 | | **0.256** | 75 | 91 |
| | **0.512** | 13 | 20 | | **0.512** | 39 | 46 |
| | **1** | 6.8 | 11 | | **1** | 20 | 24 |
| | **2** | 3.6 | 5.5 | | **2** | 10 | 12 |
| | **4** | 1.9 | 3.0 | | **4** | 5 | 6 |
| | **8** | 1.1 | 1.8 | | **8** | 3 | 3 |
| | **16** | 0.7 | 1.1 | | **16** | 1.7 | 2 |
| | **32** | 0.5 | 0.8 | | **32** | 1 | 1 |
| | **64** | 0.4 | 0.7 | | **64** | 0.8 | 0.9 |
| | **128** | 0.3 | 0.6 | | **128** | 0.7 | 0.7 |
| | **256** | 0.3 | 0.5 | | **256** | 0.6 | 0.6 |

**TABLE 4-2: RESPONSE TIME(1)**

| CLKSEL | Min. | Max. |
|---|---|---|
| 1 (32 MHz) | 20 ms | 20 ms + LPCON |
| 0 (16 MHz) | 40 ms | 40 ms + LPCON |

**Note 1:** It assumes low and/or consistent environmental noise. Response times increase in high and/or erratic noise conditions.

PRELIMINARY

**FIGURE 4-2: MAXIMUM PROXIMITY DISTANCE vs. SENSOR DIAMETER**

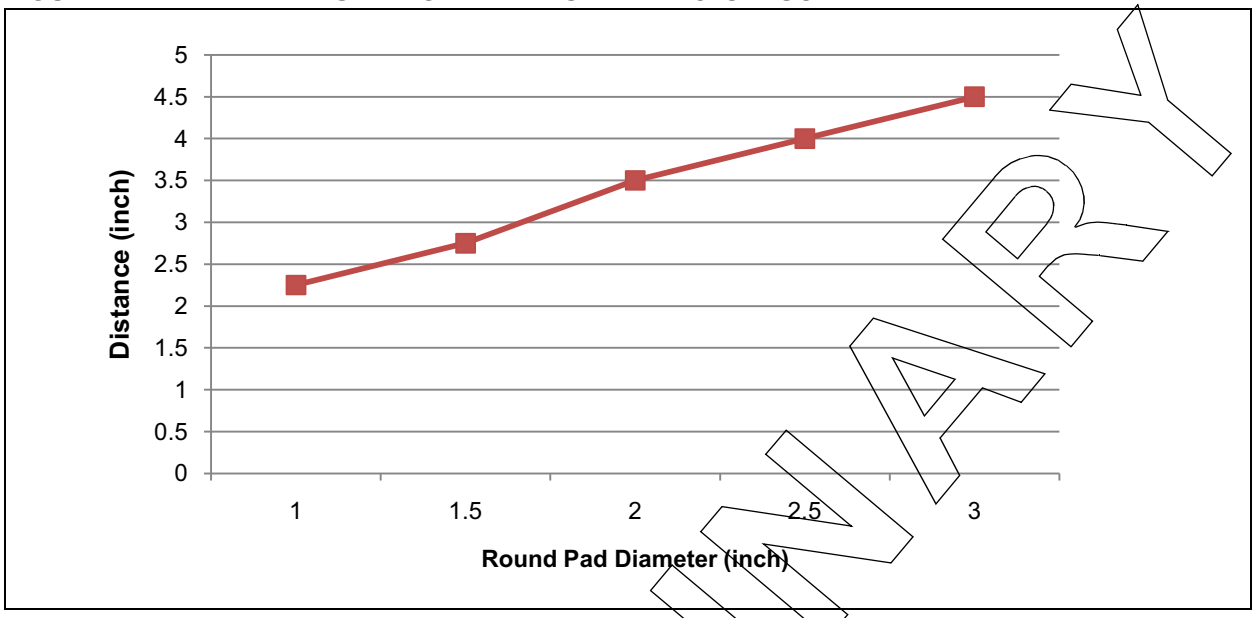
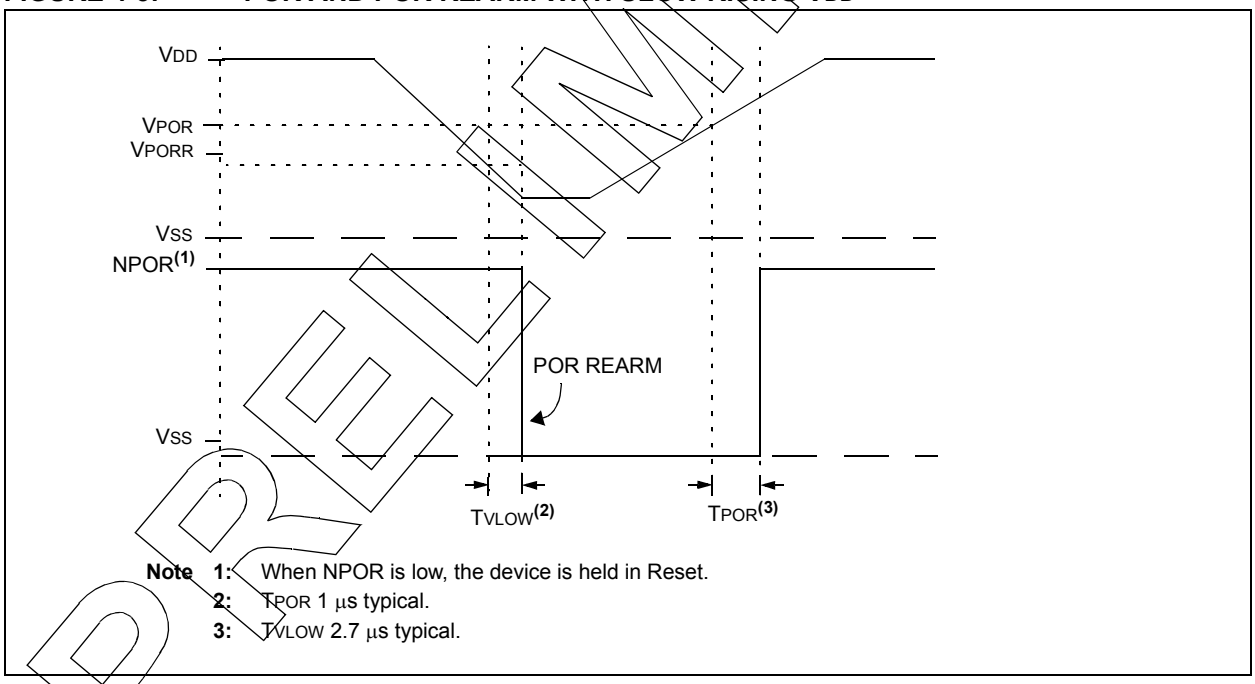



**FIGURE 4-3: POR AND POR REARM WITH SLOW RISING VDD**




**Note 1:** When NPOR is low, the device is held in Reset.
**2:** TPOR 1 µs typical.
**3:** TVLOW 2.7 µs typical.

PRELIMINARY

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## 4.2 DC Characteristics: MTCH112-I/E

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature-40°C ≤ TA ≤ +85°C for industrial | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| | | I/O PORT: | | | | | |
| D030A | | with TTL buffer | — | — | 0.15 VDD | V | 1.8V ≤ VDD ≤ 4.5V |
| D031 | | with I²C™ levels | — | — | 0.3 VDD | V | |
| D032 | | $\overline{\text{MCLR}}$ | — | — | 0.2 VDD | V | |
| | VIH | **Input High Voltage** | | | | | |
| | | I/O ports: | | — | — | | |
| D040A | | with TTL buffer | 0.25 VDD + 0.8 | — | — | V | 1.8V ≤ VDD ≤ 4.5V |
| D041 | | with I²C™ levels | 0.7 VDD | — | — | V | |
| D042 | | $\overline{\text{MCLR}}$ | 0.8 VDD | — | — | V | |
| | IIL | **Input Leakage Current(1)** | | | | | |
| D060 | | I/O ports | — | ± 5 | ± 125 | nA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance at 85°C |
| | | | — | ± 5 | ± 1000 | nA | 125°C |
| D061 | | $\overline{\text{MCLR}}$(2) | — | ± 50 | ± 200 | nA | VSS ≤ VPIN ≤ VDD at 85°C |
| | VOL | **Output Low Voltage(3)** | | | | | |
| D080 | | I/O ports | — | — | 0.6 | V | IOL = 6 mA, VDD = 3.3V<br>IOL = 1.8 mA, VDD = 1.8V |
| | VOH | **Output High Voltage(3)** | | | | | |
| D090 | | I/O ports | VDD - 0.7 | — | — | V | IOH = 3 mA, VDD = 3.3V<br>IOH = 1 mA, VDD = 1.8V |
| | | **Capacitive Loading Specs on Output Pins** | | | | | |
| D101A* | CIO | All I/O pins | — | — | 50 | pF | |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** Negative current is defined as current sourced by the pin.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Including OSC2 in CLKOUT mode.

PRELIMINARY

## 4.3 Memory Programming Requirements

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| | | **Data EEPROM Memory** | | | | | |
| D116 | ED | Byte Endurance | 100K | — | — | E/W | -40°C to +85°C |
| D117 | VDRW | VDD for Read/Write | VDDMIN | — | VDDMAX | V | |
| D118 | TDEW | Erase/Write Cycle Time | — | 4.0 | 5.0 | ms | |
| D119 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated |

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 4-4: LOAD CONDITIONS**

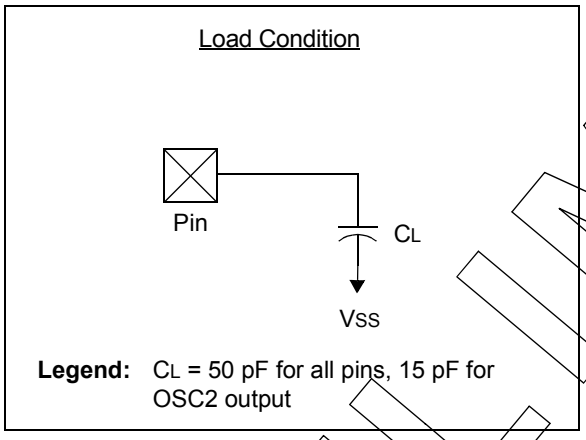


**TABLE 4-3: CLKOUT AND I/O TIMING PARAMETERS**

| Standard Operating Conditions (unless otherwise stated)<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| OS18* | TioR | Port output rise time | —<br>— | 90<br>55 | 140<br>80 | ns | VDD = 1.8V<br>VDD = 3.0-5.0V |
| OS19* | TioF | Port output fall time | —<br>— | 60<br>44 | 80<br>60 | ns | VDD = 1.8V<br>VDD = 3.0-5.0V |

* These parameters are characterized but not tested.
† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

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**FIGURE 4-5: BROWN-OUT RESET TIMING AND CHARACTERISTICS**

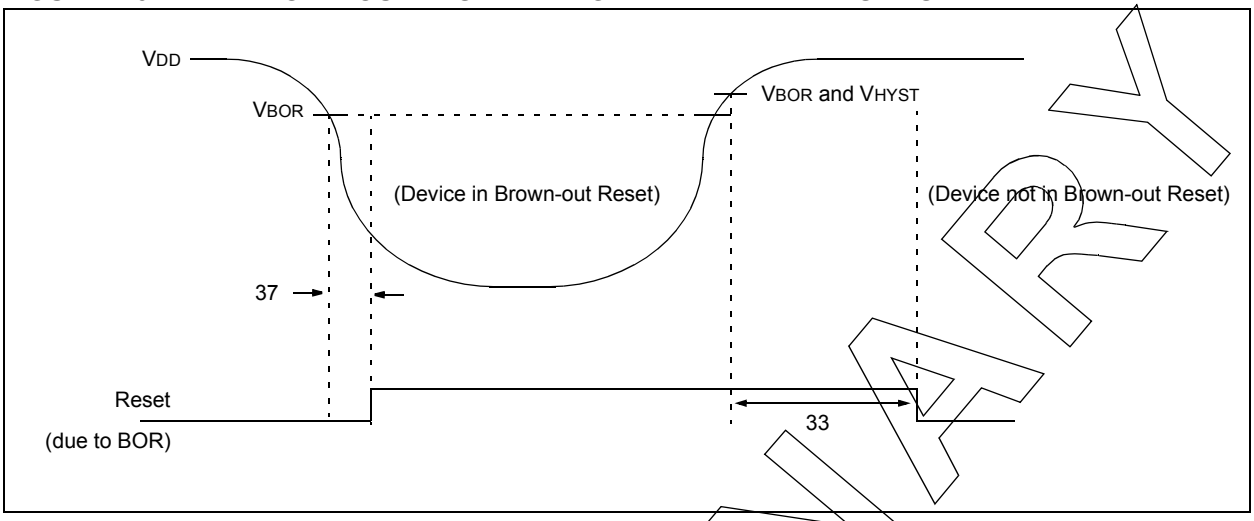



**TABLE 4-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET PARAMETERS**

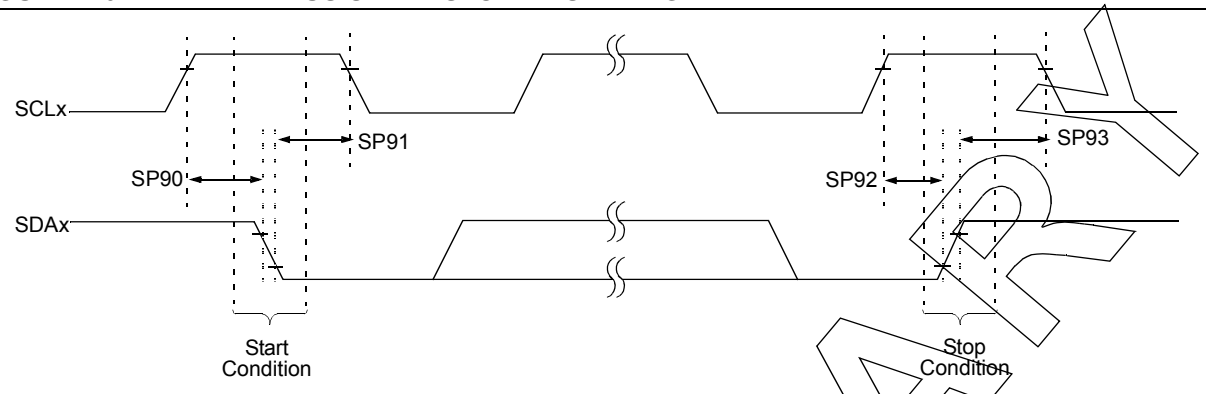
| **Standard Operating Conditions (unless otherwise stated)**<br>Operating Temperature -40°C ≤ TA ≤ +125°C | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Sym.** | **Characteristic** | **Min.** | **Typ†** | **Max.** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{\text{RESET}}$ Pulse Width (low) | 2<br>5 | —<br>— | —<br>— | μs<br>μs | VDD = 3.3-5V, -40°C to +85°C<br>VDD = 3.3-5V |
| 31 | TWDTLP | Watchdog Timer Time-out Period | 10 | 16 | 27 | ms | VDD = 3.3V-5V,<br>1:16 Prescaler used |
| 33* | TPWRT | Power-up Timer Period | 40 | 65 | 140 | ms | |
| 34* | TIOZ | I/O High-impedance from $\overline{\text{RESET}}$ Low or Watchdog Timer Reset | — | — | 2.0 | μs | |
| 35 | VBOR | Brown-out Reset Voltage | 1.80 | 1.9 | 2.05 | V | BORV=1.9V |
| 37* | VHYST | Brown-out Reset Hysteresis | 0 | 25 | 50 | mV | -40°C to +85°C |
| 38* | TBORDC | Brown-out Reset DC Response Time | 0 | 1 | 40 | μs | VDD ≤ VBOR |

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

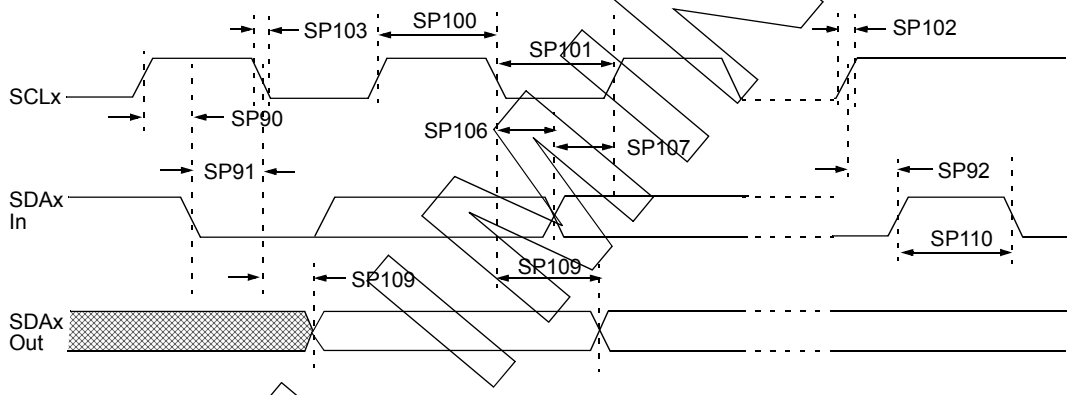
PRELIMINARY

**FIGURE 4-6: I²C™ BUS START/STOP BITS TIMING**




**Note**: Refer to Figure 4-4 for load conditions.

**FIGURE 4-7: I²C™ BUS DATA TIMING**




**Note:** Refer to Figure 4-4 for load conditions.

PRELIMINARY

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**TABLE 4-5: I²C™ BUS DATA REQUIREMENTS**

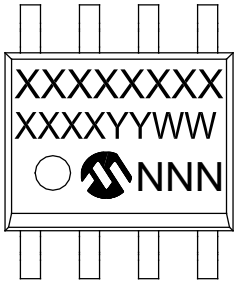
| Param. No. | Symbol | Characteristic | | Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| SP100* | THIGH | Clock high time | 400 kHz mode | 0.6 | — | μs | Device must operate at a minimum of 10 MHz |
| | | | SSPx module | 1.5TCY | — | — | |
| SP101* | TLOW | Clock low time | 400 kHz mode | 1.3 | — | μs | Device must operate at a minimum of 10 MHz |
| SP102* | TR | SDAx and SCLx rise time | 400 kHz mode | 20 + 0.1CB | 300 | ns | CB is specified to be from 10-400 pF |
| SP103* | TF | SDAx and SCLx fall time | 400 kHz mode | 20 + 0.1CB | 250 | ns | CB is specified to be from 10-400 pF |
| SP106* | THD:DAT | Data input hold time | 400 kHz mode | 0 | 0.9 | μs | |
| SP107* | TSU:DAT | Data input setup time | 400 kHz mode | 100 | — | ns | |
| SP109* | TAA | Output valid from clock | 400 kHz mode | — | — | ns | |
| SP110* | TBUF | Bus free time | 400 kHz mode | 1.3 | — | μs | Time the bus must be free before a new transmission can start |
| SP111 | CB | Bus capacitive loading | | — | 400 | pF | |

* These parameters are characterized but not tested.

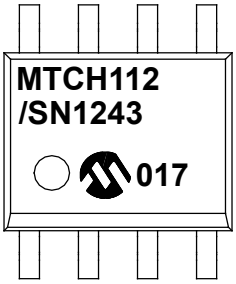
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

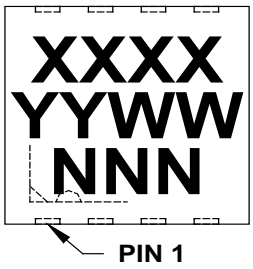
8-Lead SOIC (3.90 mm)



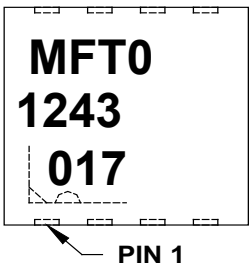

Example




8-Lead DFN (3x3x0.9 mm)




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |
| **Note**: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. | |

* Standard PIC® device marking consists of Microchip part number, year code, week code, and traceability code. For PIC device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

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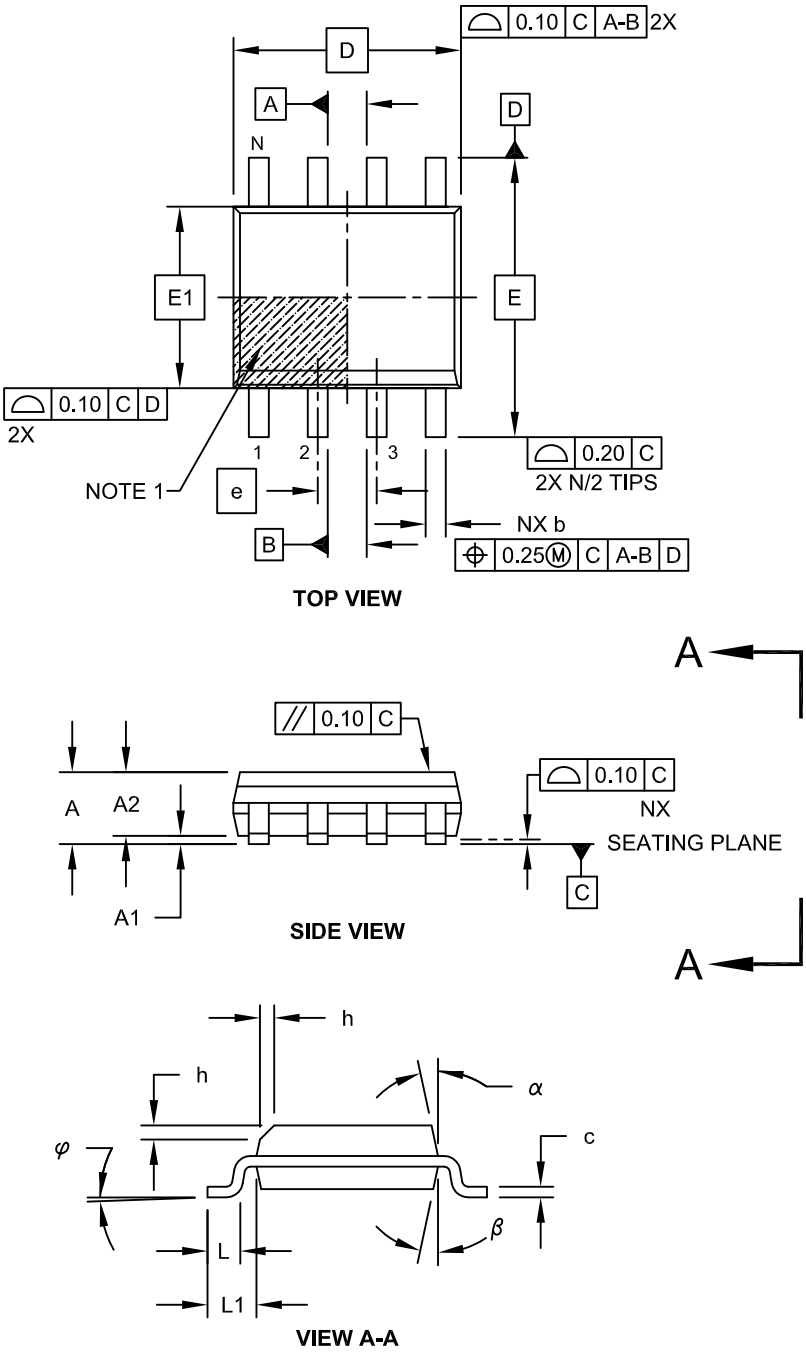
## 5.2 Package Details

The following sections give the technical details of the packages.

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

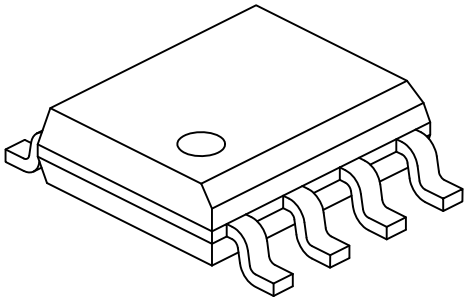
| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |




Microchip Technology Drawing No. C04-057C Sheet 1 of 2

### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | - | - | 1.75 |
| Molded Package Thickness | A2 | 1.25 | - | - |
| Standoff § | A1 | 0.10 | - | 0.25 |
| Overall Width | E | 6.00 BSC | | |
| Molded Package Width | E1 | 3.90 BSC | | |
| Overall Length | D | 4.90 BSC | | |
| Chamfer (Optional) | h | 0.25 | - | 0.50 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | 1.04 REF | | |
| Foot Angle | $\varphi$ | 0° | - | 8° |
| Lead Thickness | c | 0.17 | - | 0.25 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | $\alpha$ | 5° | - | 15° |
| Mold Draft Angle Bottom | $\beta$ | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

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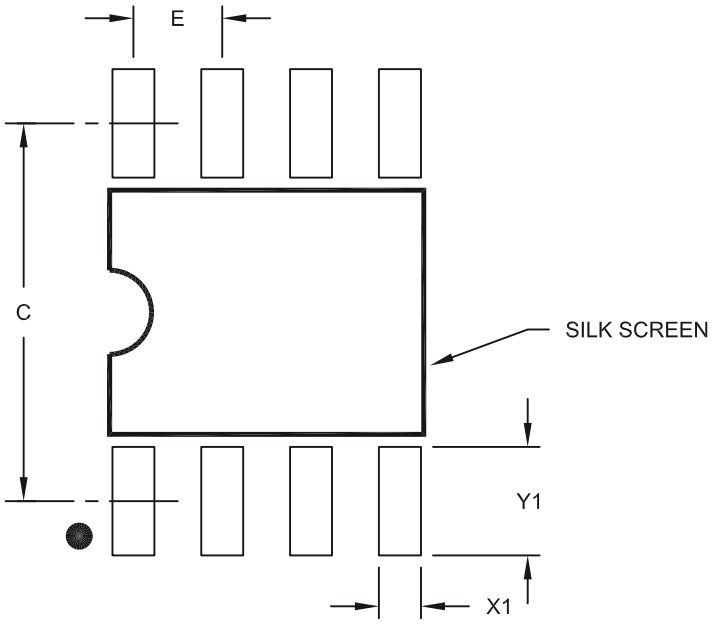
## 8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 5.40 | |
| Contact Pad Width (X8) | X1 | | | 0.60 |
| Contact Pad Length (X8) | Y1 | | | 1.55 |

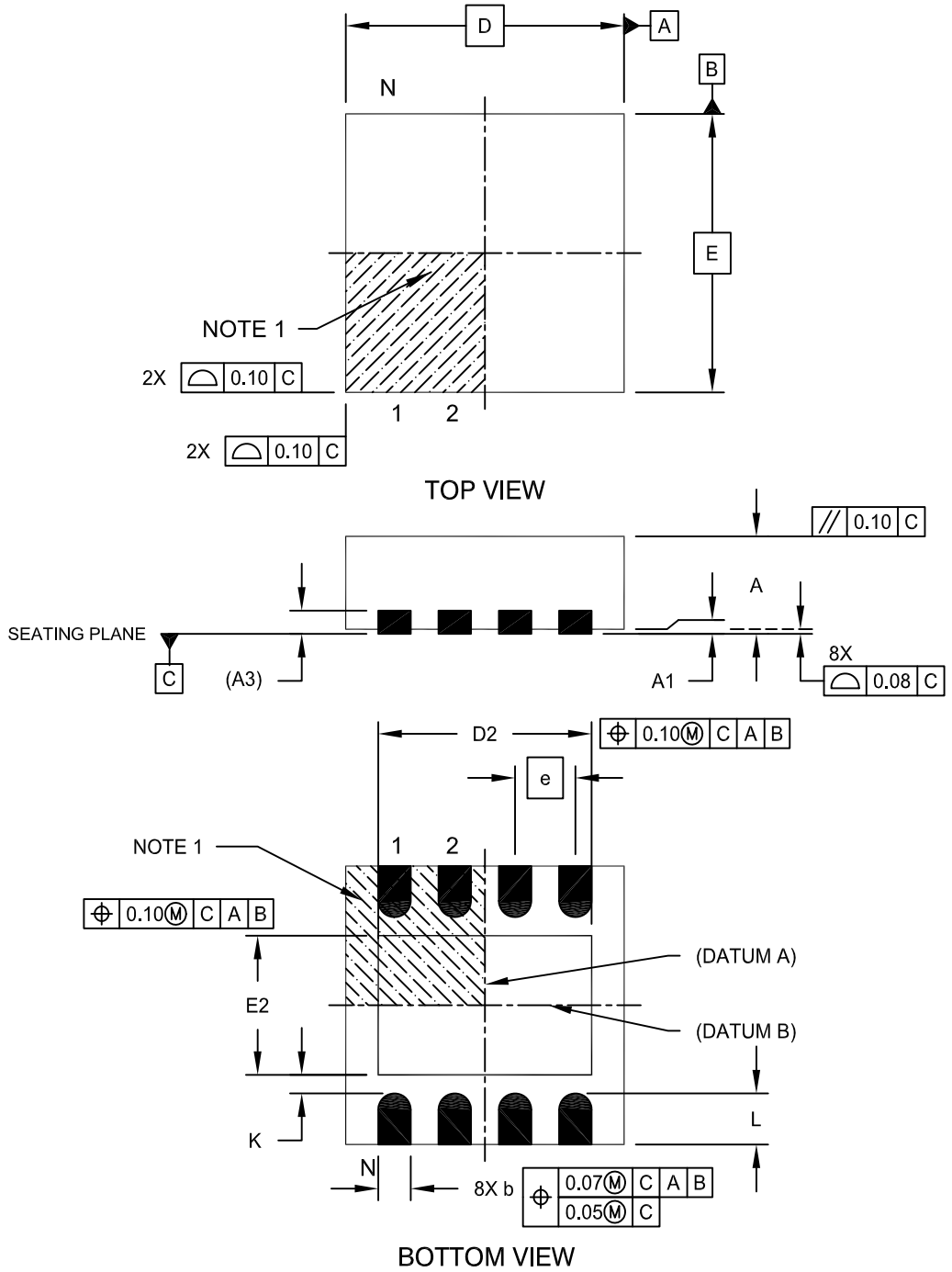
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

### 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing No. C04-062C Sheet 1 of 2

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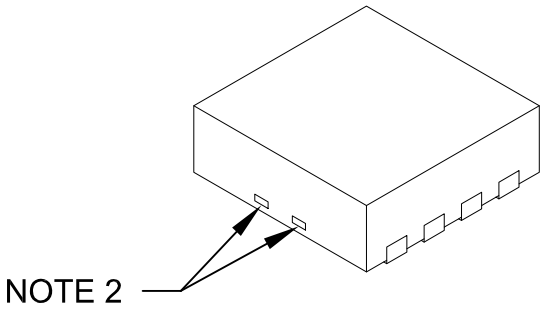
## 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | 8 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Length | D | 3.00 BSC | | |
| Exposed Pad Width | E2 | 1.34 | - | 1.60 |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Length | D2 | 1.60 | - | 2.40 |
| Contact Width | b | 0.25 | 0.30 | 0.35 |
| Contact Length | L | 0.20 | 0.30 | 0.55 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

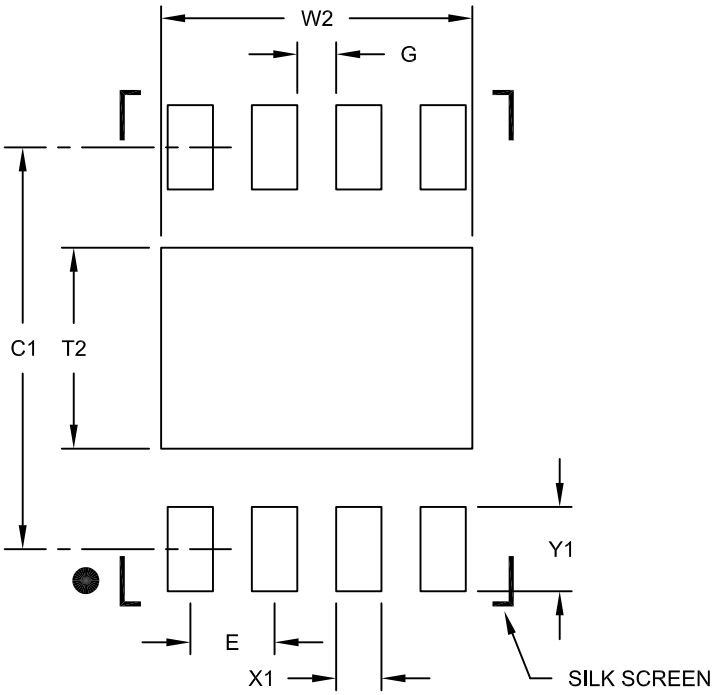
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-062C Sheet 2 of 2

### 8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 2.40 |
| Optional Center Pad Length | T2 | | | 1.55 |
| Contact Pad Spacing | C1 | | 3.10 | |
| Contact Pad Width (X8) | X1 | | | 0.35 |
| Contact Pad Length (X8) | Y1 | | | 0.65 |
| Distance Between Pads | G | 0.30 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2062B

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# APPENDIX A: DATA SHEET REVISION HISTORY

## Revision A (11/2012)

Initial release of this data sheet.

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_____

_____

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_____

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_____

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7. How would you improve this document?

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| PART NO. | [X][1] | - | X | /XX | XXX |
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| | |
|---|---|
| **Device:** | MTCH112 |
| **Tape and Reel Option:** | Blank = Standard packaging (tube or tray)<br>T = Tape and Reel[1] |
| **Temperature Range:** | I = -40°C to +85°C (Industrial) |
| **Package:**[2] | SN = SOIC<br>MF = DFN |
| **Pattern:** | QTP, SQTP, Code or Special Requirements (blank otherwise) |

**Examples:**

a) MTCH112 - I/MF
Industrial temperature,
DFN package

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