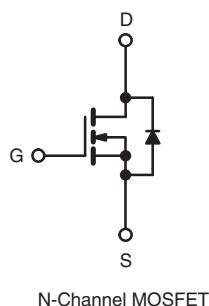
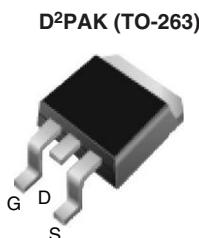


Power MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	400
R _{DSD(on)} (Ω)	V _{GS} = 10 V 0.55
Q _g (Max.) (nC)	63
Q _{gs} (nC)	9.0
Q _{gd} (nC)	32
Configuration	Single



ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHF740S-GE3	SiHF740STR-GE3 ^a	SiHF740STRR-GE3 ^a
Lead (Pb)-free	IRF740SPbF	IRF740STRLPbF ^a	IRF740STRRPPbF ^a
	SiHF740S-E3	SiHF740STL-E3 ^a	SiHF740STR-E3 ^a

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	400	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current	I _D	10 6.3	A
Pulsed Drain Current ^a	I _{DM}	40	
Linear Derating Factor		1.0 0.025	W/C
Linear Derating Factor (PCB Mount) ^e		0.025	
Single Pulse Avalanche Energy ^b	E _{AS}	520	mJ
Avalanche Current ^a	I _{AR}	10	A
Repetitive Avalanche Energy ^a	E _{AR}	13	mJ
Maximum Power Dissipation	P _D	125 3.1	W
Maximum Power Dissipation (PCB Mount) ^e		3.1	
Peak Diode Recovery dV/dt ^c	dV/dt	4.0	V/ns
Operating Junction and Storage Temperature Range	T _J , T _{Stg}	- 55 to + 150	
Soldering Recommendations (Peak Temperature)		300 ^d	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 9.1 mH, R_G = 25 Ω, I_{AS} = 10 A (see fig. 12).

c. I_{SD} ≤ 10A, dI/dt ≤ 120 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.

d. 1.6 mm from case.

e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply



FEATURES

- Halogen-free According to IEC 61249-2-21
- Definition
- Surface Mount
- Available in Tape and Reel
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Parallelizing
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.0	

Note

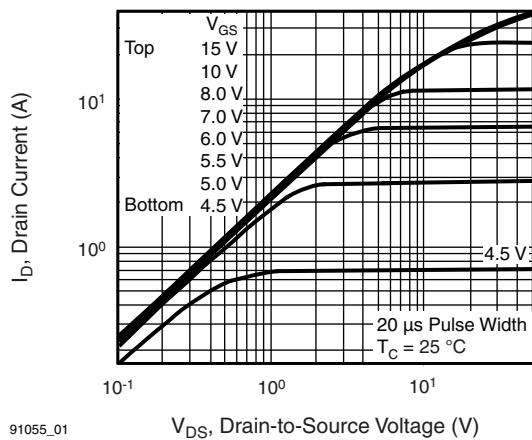
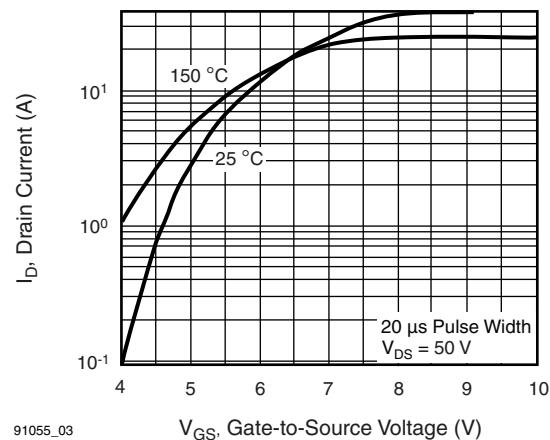
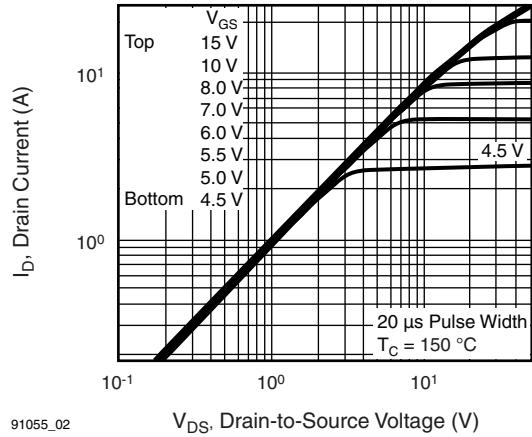
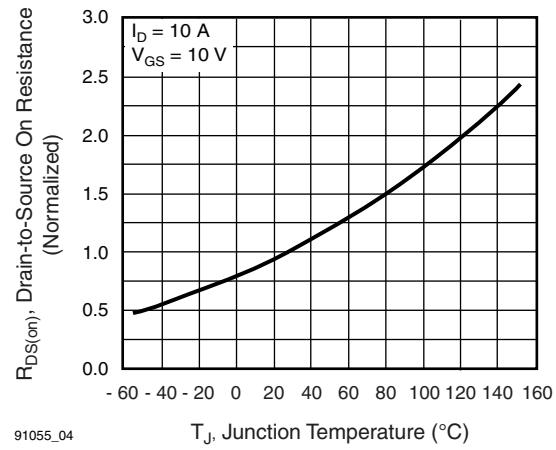
- a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS ($T_J = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$, $I_D = 250$ µA		400	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 1$ mA		-	0.49	-	V/°C	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ µA		2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20$ V		-	-	± 100	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 400$ V, $V_{GS} = 0$ V		-	-	25	µA	
		$V_{DS} = 320$ V, $V_{GS} = 0$ V, $T_J = 125$ °C		-	-	250		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 6.0$ A ^b	-	-	0.55	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50$ V, $I_D = 6.0$ A ^b		5.8	-	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0$ V, $V_{DS} = 25$ V, $f = 1.0$ MHz, see fig. 5		-	1400	-	pF	
Output Capacitance	C_{oss}			-	330	-		
Reverse Transfer Capacitance	C_{rss}			-	120	-		
Total Gate Charge	Q_g	$V_{GS} = 10$ V	$I_D = 10$ A, $V_{DS} = 320$ V, see fig. 6 and 13 ^b	-	-	63	nC	
Gate-Source Charge	Q_{gs}			-	-	9.0		
Gate-Drain Charge	Q_{gd}			-	-	32		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 200$ V, $I_D = 10$ A, $R_g = 9.1$ Ω, $R_D = 20$ Ω, see fig. 10 ^b		-	14	-	ns	
Rise Time	t_r			-	27	-		
Turn-Off Delay Time	$t_{d(off)}$			-	50	-		
Fall Time	t_f			-	24	-		
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH	
Internal Source Inductance	L_S			-	7.5	-		
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	10	A	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	40		
Body Diode Voltage	V_{SD}	$T_J = 25$ °C, $I_S = 10$ A, $V_{GS} = 0$ V ^b		-	-	2.0	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25$ °C, $I_F = 10$ A, $dI/dt = 100$ A/µs ^b		-	370	790	ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	3.8	8.2	µC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)						

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25 \text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150 \text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

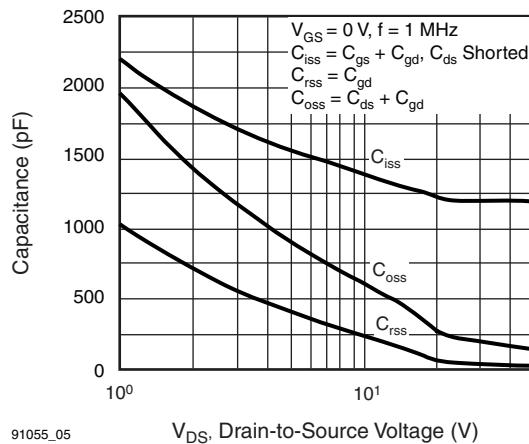


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

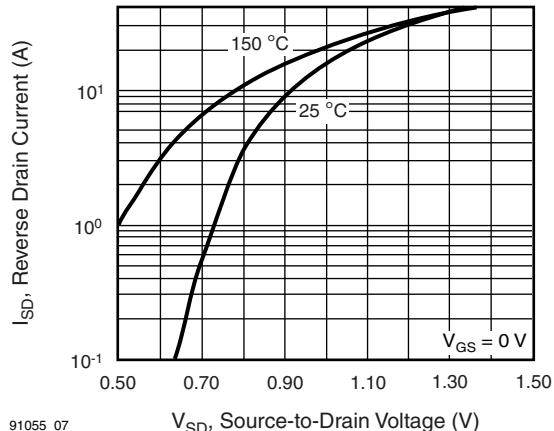


Fig. 7 - Typical Source-Drain Diode Forward Voltage

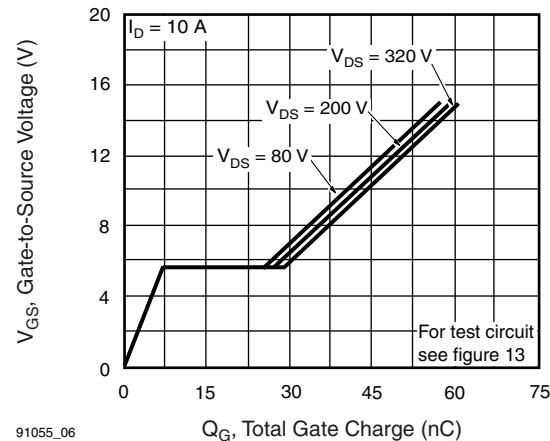


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

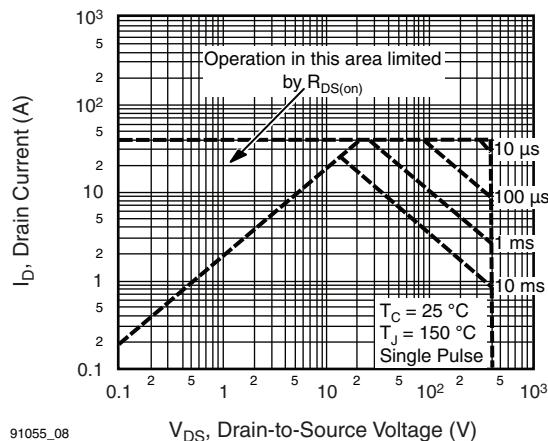


Fig. 8 - Maximum Safe Operating Area

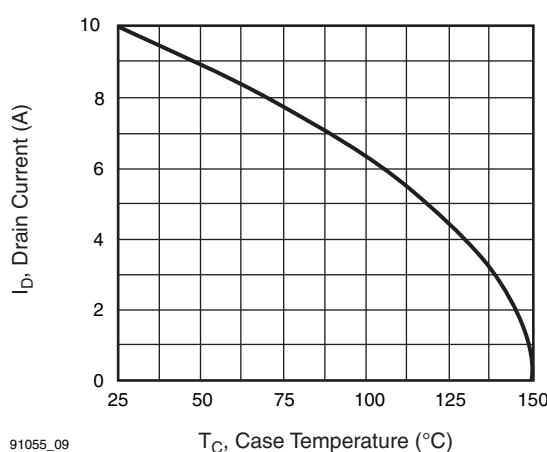


Fig. 9 - Maximum Drain Current vs. Case Temperature

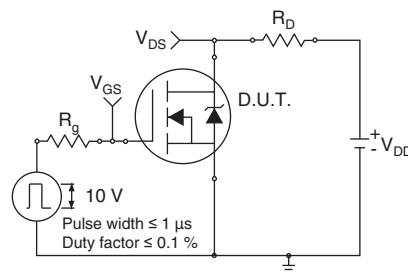


Fig. 10a - Switching Time Test Circuit

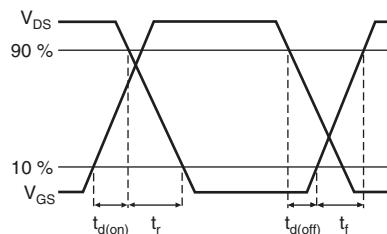


Fig. 10b - Switching Time Waveforms

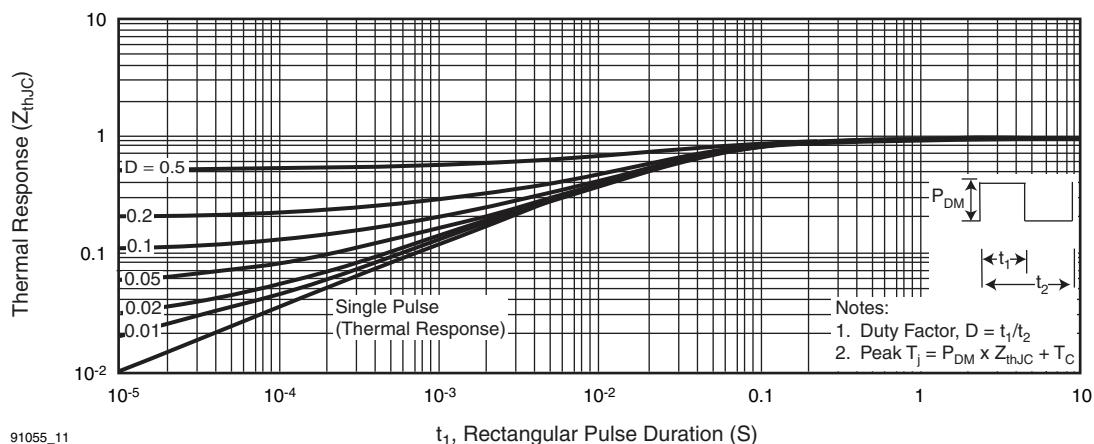


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

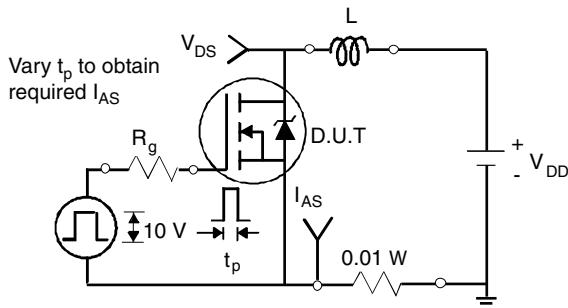


Fig. 12a - Unclamped Inductive Test Circuit

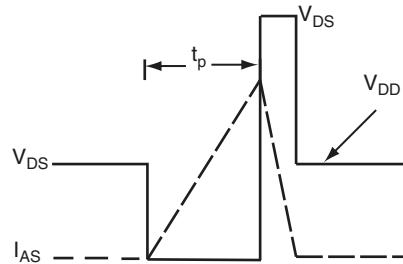


Fig. 12b - Unclamped Inductive Waveforms

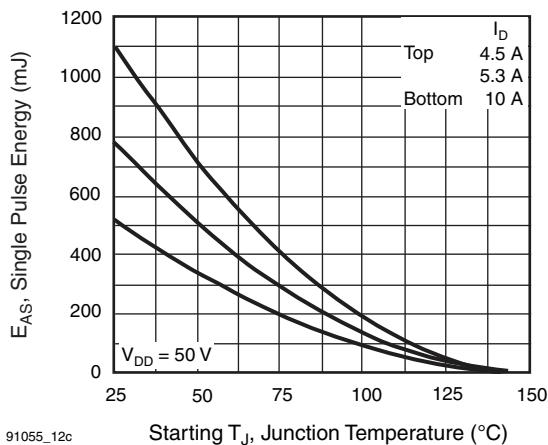


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

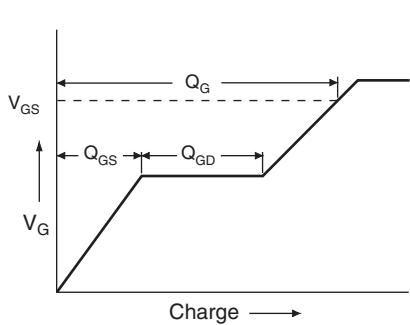


Fig. 13a - Basic Gate Charge Waveform

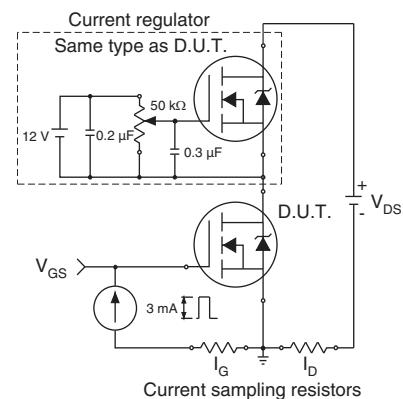
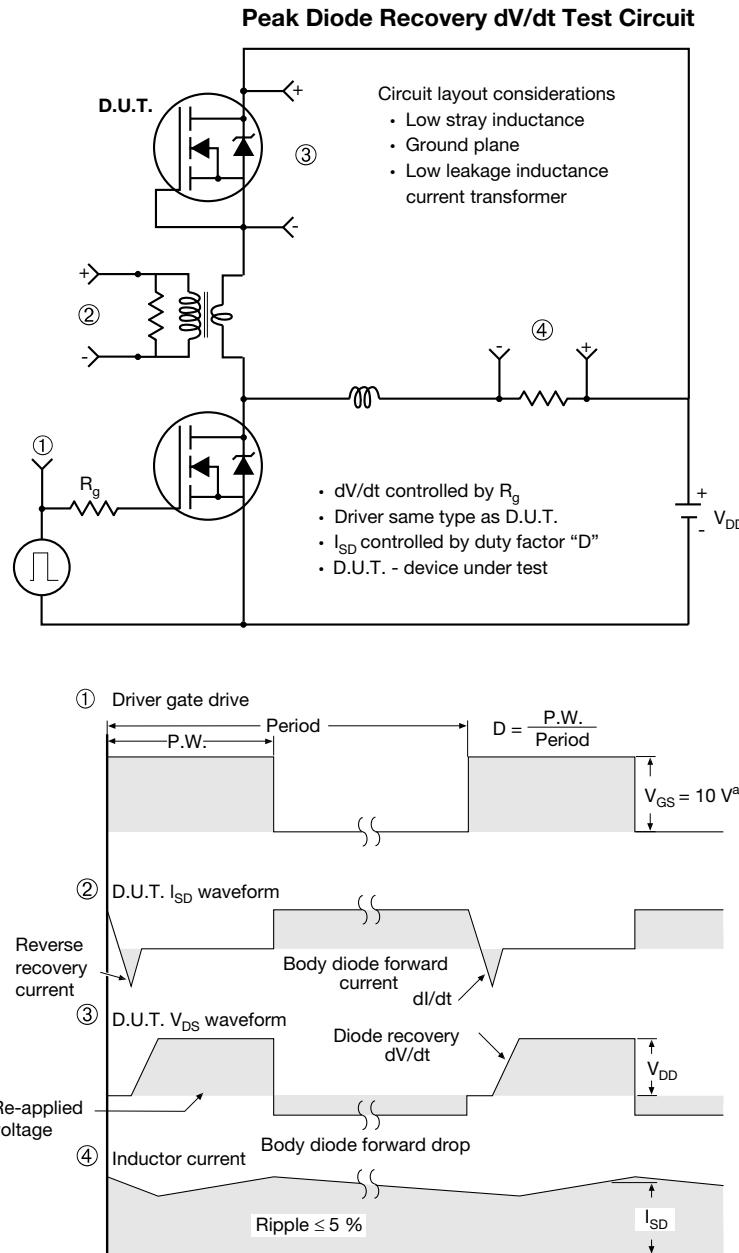


Fig. 13b - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



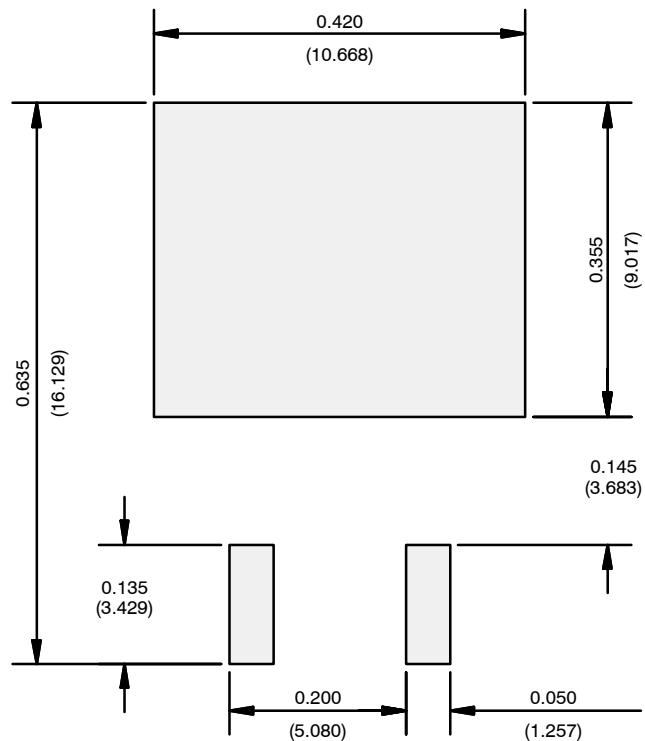
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994.
- Dimensions are shown in millimeters (inches).
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- Thermal PAD contour optional within dimension E, L1, D1 and E1.
- Dimension b1 and c1 apply to base metal only.
- Datum A and B to be determined at datum plane H.
- Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead

Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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