

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A) ^{a, e}	Q _g (Typ.)
- 20	0.076 at V _{GS} = - 4.5 V	- 2.9	7.5 nC
	0.100 at V _{GS} = - 2.5 V	- 2.5	
	0.145 at V _{GS} = - 1.8 V	- 2.1	
	0.320 at V _{GS} = - 1.5 V	- 0.5	

FEATURES

- TrenchFET[®] Power MOSFET
- Small 0.8 mm x 0.8 mm outline area
- Low 0.4 mm max. profile
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912

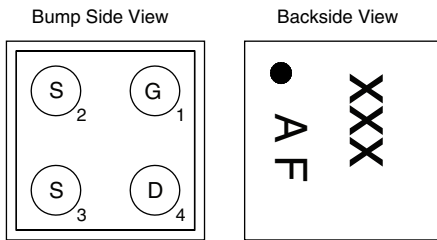


RoHS
COMPLIANT
HALOGEN
FREE

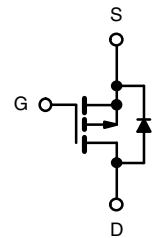
APPLICATIONS

- Load switches and chargers switches
- Battery management
- DC/DC converters
- For smart phones and tablet PCs

MICRO FOOT



Device Marking: A F
xxx = Date/Lot Traceability Code



P-Channel MOSFET

Ordering Information: Si8817DB-T2-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	- 20	V
Gate-Source Voltage	V _{GS}	± 8	
Continuous Drain Current (T _J = 150 °C)	I _D	T _A = 25 °C	- 2.9 ^a
		T _A = 70 °C	- 2.3 ^a
		T _A = 25 °C	- 2.1 ^b
		T _A = 70 °C	- 1.7 ^b
Pulsed Drain Current (t = 300 μs)	I _{DM}	- 15	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	- 0.4 ^b
Maximum Power Dissipation	P _D	T _A = 25 °C	0.9 ^a
		T _A = 70 °C	0.6 ^a
		T _A = 25 °C	0.5 ^b
		T _A = 70 °C	0.3 ^b
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Package Reflow Conditions ^c	VPR	260	
	IR/Convection	260	

Notes:

- Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
- Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
- Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
- Based on T_A = 25 °C.

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t = 5 s	R _{thJA}	105	135	°C/W
Maximum Junction-to-Ambient ^{c, d}	t = 5 s		200	260	

Notes:

- a. Surface mounted on 1" x 1" FR4 board with full copper.
b. Maximum under steady state conditions is 185 °C/W.
c. Surface mounted on 1" x 1" FR4 board with minimum copper.
d. Maximum under steady state conditions is 330 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 12		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J		2.5			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	μA
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 70 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 1 A		0.061	0.076	Ω
		V _{GS} = - 2.5 V, I _D = - 1 A		0.080	0.100	
		V _{GS} = - 1.8 V, I _D = - 0.5 A		0.110	0.145	
		V _{GS} = - 1.5 V, I _D = - 0.5 A		0.165	0.320	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 10 V, I _D = - 1 A		5		S
Dynamic^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		615		pF
Output Capacitance	C _{oss}		90			
Reverse Transfer Capacitance	C _{rss}		75			
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 8 V, I _D = - 1 A		12.5	19	nC
		V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 1 A		7.5	12	
Gate-Source Charge	Q _{gs}			1		
Gate-Drain Charge	Q _{gd}		1.9			
Gate Resistance	R _g	V _{GS} = - 0.1 V, f = 1 MHz		14		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 10 Ω I _D ≅ - 1 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		20	40	ns
Rise Time	t _r			20	40	
Turn-Off Delay Time	t _{d(off)}			52	100	
Fall Time	t _f			22	45	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 10 Ω I _D ≅ - 1 A, V _{GEN} = - 8 V, R _g = 1 Ω		6	15	
Rise Time	t _r			10	20	
Turn-Off Delay Time	t _{d(off)}			60	120	
Fall Time	t _f			23	45	



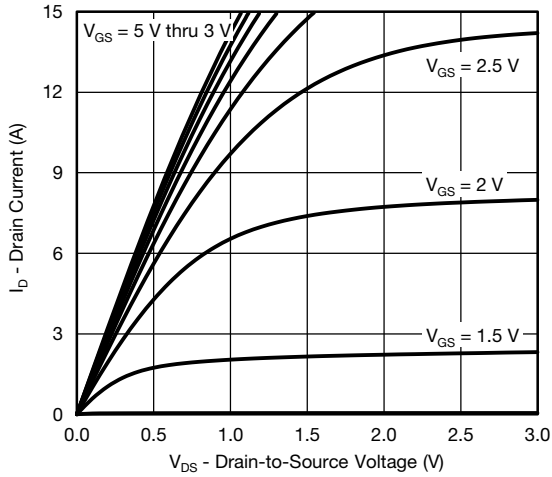
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_A = 25\text{ }^\circ\text{C}$			- 0.7	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	$I_S = -1\text{ A}, V_{GS} = 0\text{ V}$		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = -1\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	30	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			17		

Notes:

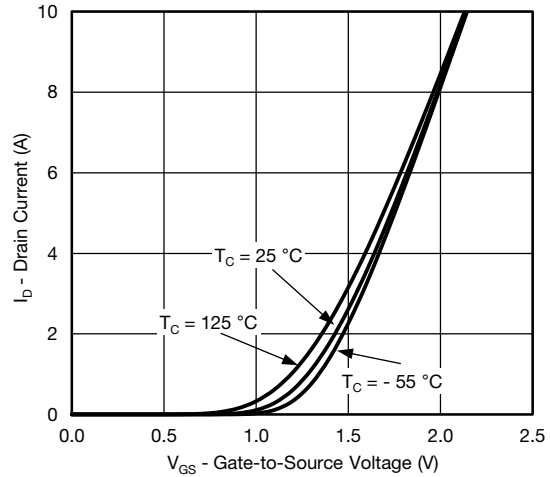
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

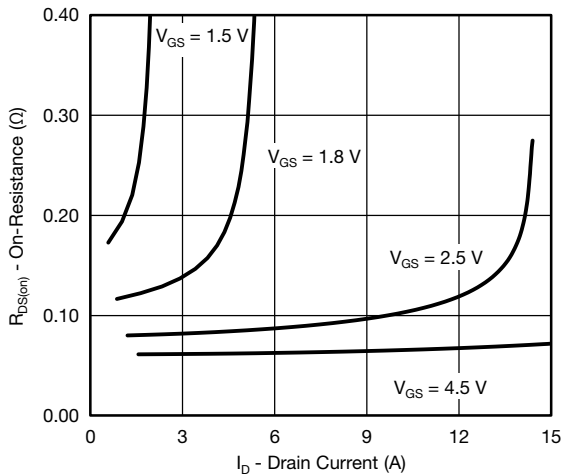
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



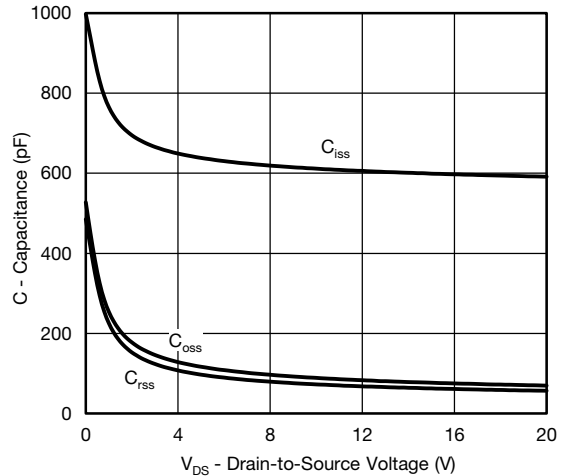
Output Characteristics



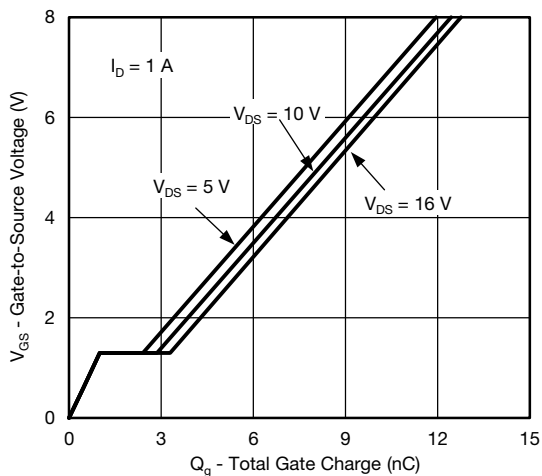
Transfer Characteristics



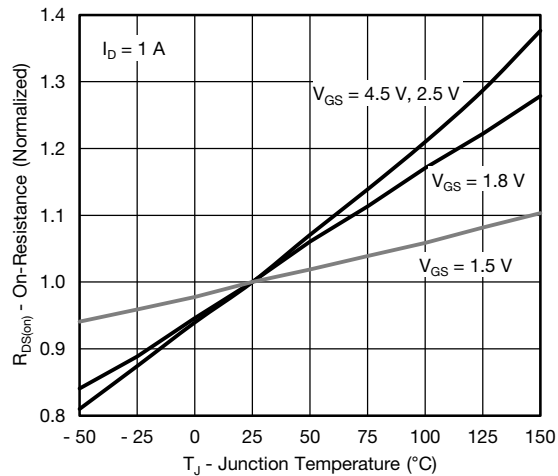
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

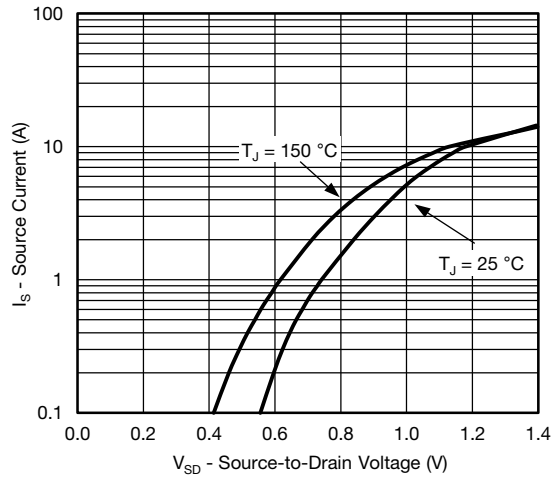


Gate Charge

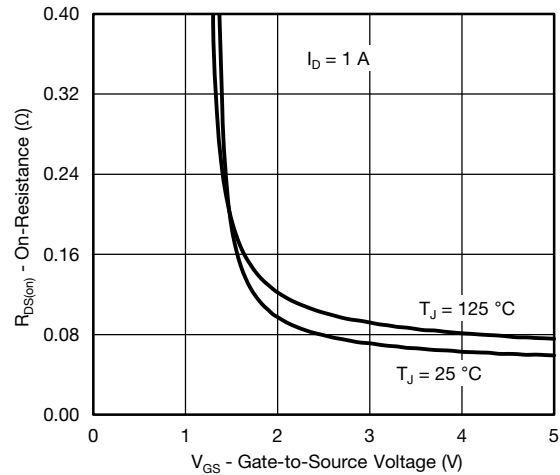


On-Resistance vs. Junction Temperature

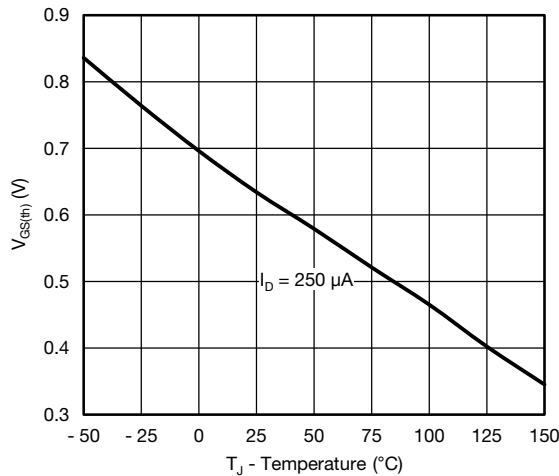
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



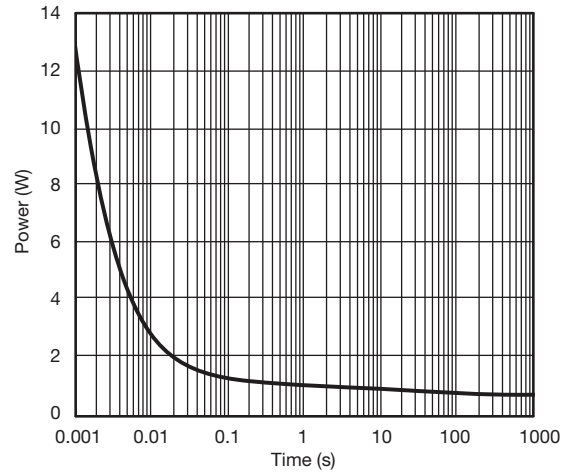
Source-Drain Diode Forward Voltage



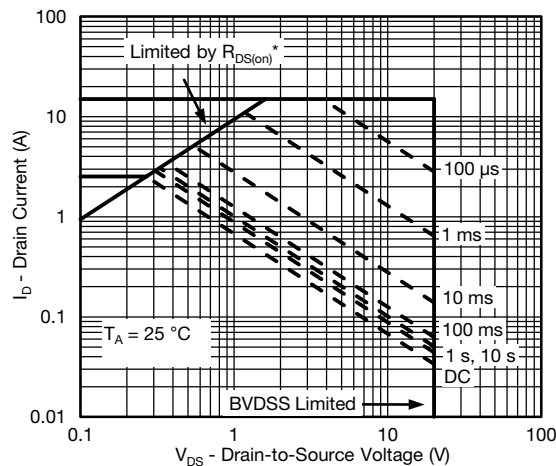
On-Resistance vs. Gate-to-Source Voltage



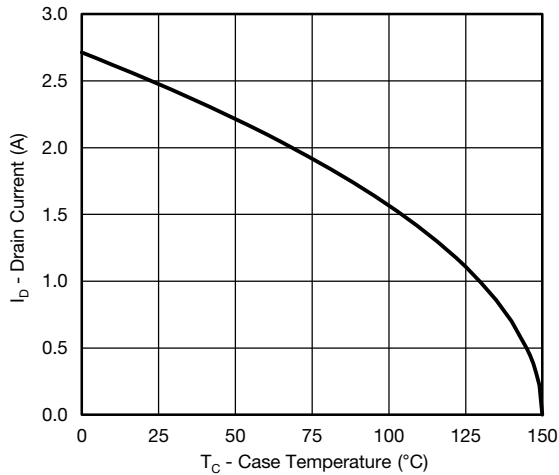
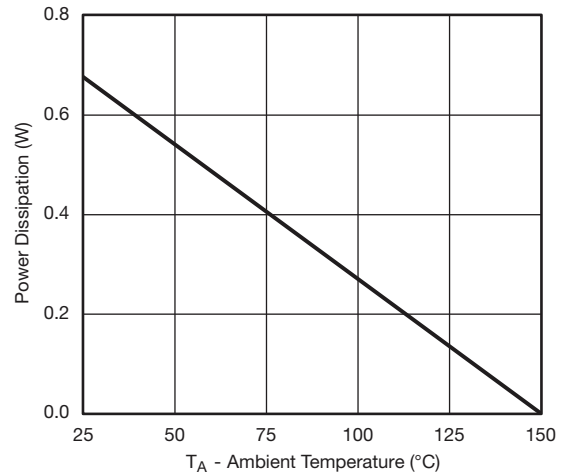
Threshold Voltage



Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

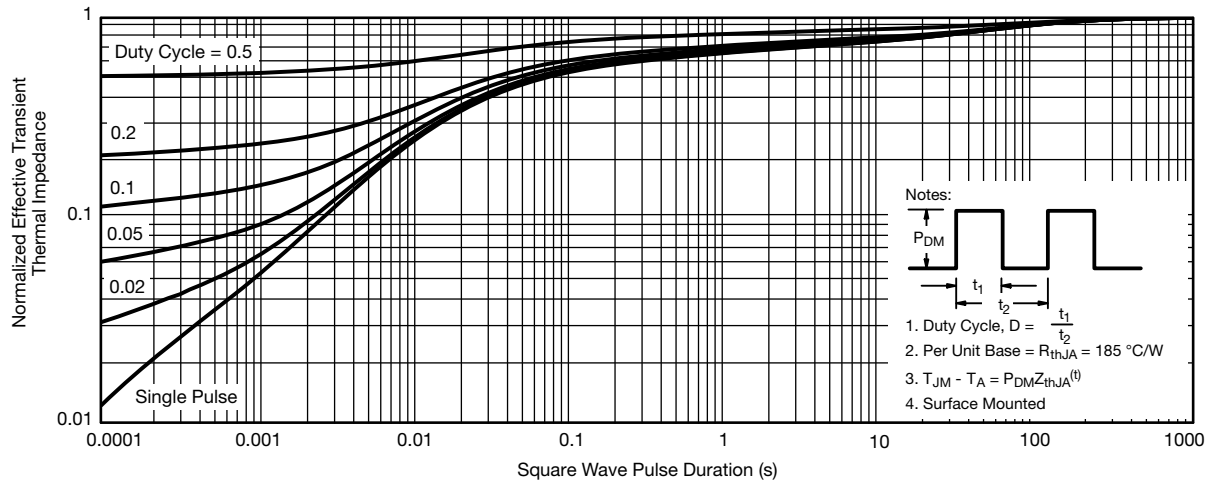
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating*

Power Derating

Note:

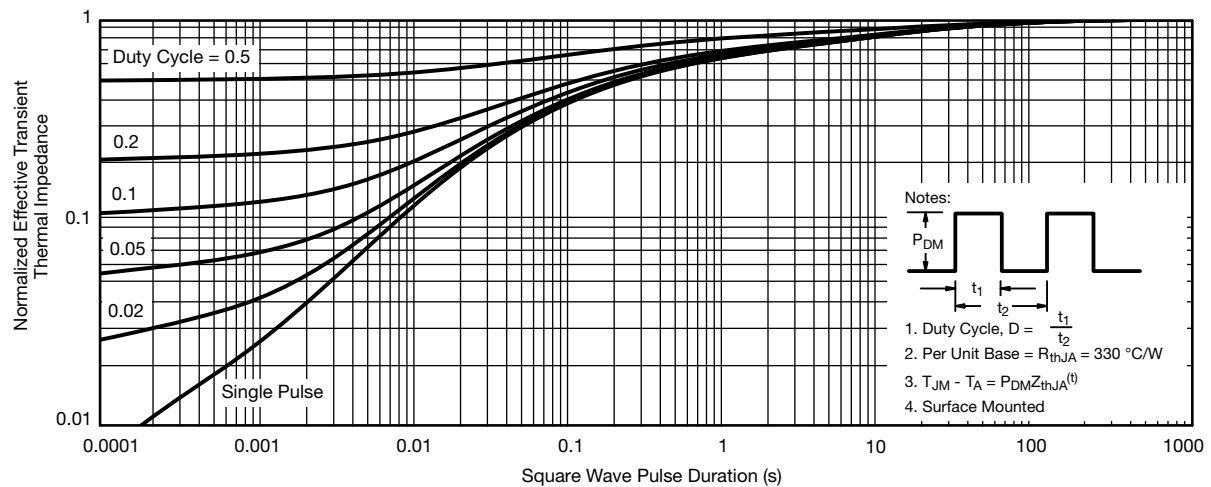
When mounted on 1" x 1" FR4 with full copper.

* The power dissipation P_D is based on $T_{J(max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



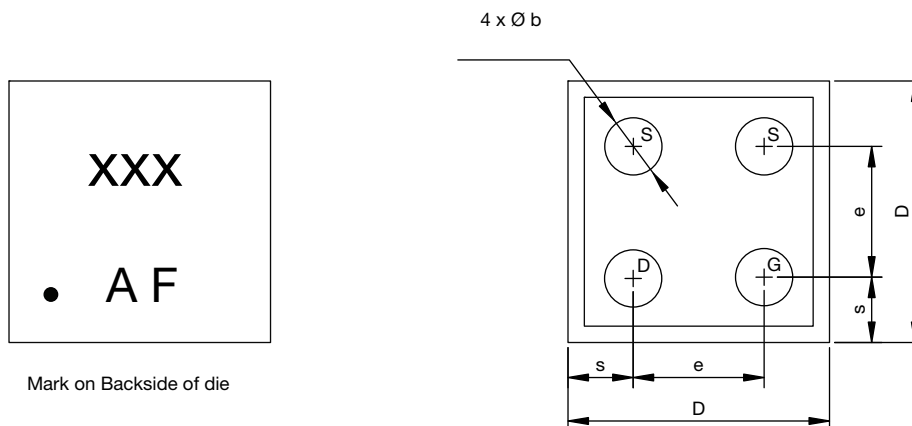
Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with maximum Copper)



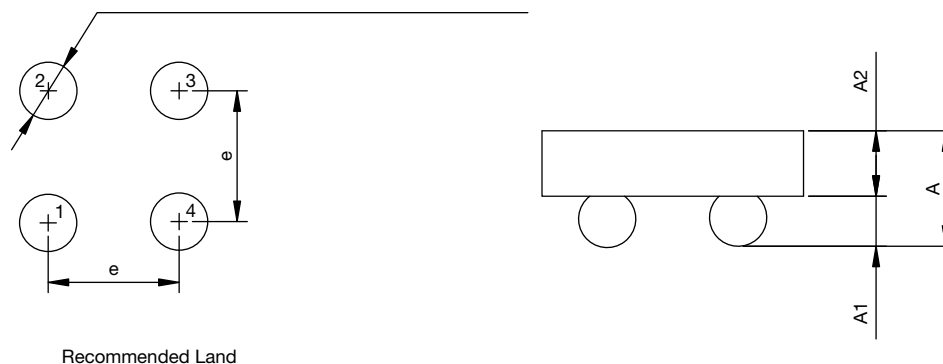
Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 Board with minimum Copper)

PACKAGE OUTLINE

MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



4 x Ø 0.205 to 0.225 Note 4
Solder Mask ~ Ø 0.215



Notes (Unless otherwise specified):

- All dimensions are in millimeters.
- Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.
- Backside surface is coated with a Ti/Ni/Ag layer.
- Non-solder mask defined copper landing pad.
- is location of pin 1.

Dim.	Millimeters ^a			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.314	0.357	0.400	0.0124	0.0141	0.0157
A ₁	0.127	0.157	0.187	0.0050	0.0062	0.0074
A ₂	0.187	0.200	0.213	0.0074	0.0079	0.0084
b	0.165	0.175	0.185	0.0064	0.0068	0.0072
e	0.400			0.0157		
s	0.180	0.200	0.220	0.0070	0.0078	0.0086
D	0.760	0.800	0.840	0.0299	0.0314	0.0330

Notes:

- Use millimeters as the primary measurement.

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- Техническая поддержка проекта;
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