

32-Bit

TC1736

32-Bit Single-Chip Microcontroller

Data Sheet

V1.1 2009-08

Microcontrollers

Edition 2009-08

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Revision History: V1.1, 2009-08

Previous Version: V1.0

| Page | Subjects (major changes since last revision) |
|-------------------|---|
| Page 5-95 | I_{DD} for 40 MHz variant and the test condition is updated. |
| Page 5-115 | The thermal resistance values are updated, the method used for the specified thermal resistances is included. |
| Page 5-116 | The package name is corrected. |

Previous Version: V0.2

| | |
|-------------------|---|
| Page 2-25 | Text which describes the endurance of PFlash and DFlash is enhanced. |
| Page 3-56 | Input spike-filter info is added to $\overline{\text{PORST}}$. |
| Page 3-56 | A footnote is added to V_{DDMF} . |
| Page 5-82 | The spike-filters parameters are included, t_{SF1} , t_{SF2} . |
| Page 5-85 | The maximum limit for I_{OZ1} is updated. |
| Page 5-93 | The temperature sensor measurement time parameter is added. |
| Page 5-95 | I_{DD} for 40 MHz variant is added. |
| Page 5-101 | The condition for HWCFG is deleted from hold time from $\overline{\text{PORST}}$ rising edge. |
| Page 5-102 | The power, pad, reset timing figure is updated. |
| Page 5-103 | The notes under the PLL sections are updated. |

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1 Summary of Features

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
 - Superior real-time performance
 - Strong bit handling
 - Fully integrated DSP capabilities
 - Single precision Floating Point Unit (FPU)
 - Up to 80 MHz operation at full temperature range
- Multiple on-chip memories
 - Up to 36 Kbyte Data Memory (LDRAM)
 - 8 Kbyte Code Scratchpad Memory (SPRAM)
 - Up to 1 Mbyte Program Flash Memory (PFlash)
 - 32 Kbyte Data Flash Memory (DFlash, represents 8Kbyte EEPROM)
 - Instruction Cache: up to 8Kbyte (ICACHE, configurable)
 - 4 Kbyte Overlay Memory (OVRAM)
 - 16 Kbyte BootROM (BROM)
- 8-Channel DMA Controller
- Sophisticated interrupt system with 255 hardware priority arbitration levels serviced by CPU
- High performing on-chip bus structure
 - 64-bit Local Memory Buses between CPU, Flash and Data Memory
 - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
 - One bus bridges (LFI Bridge)
- Versatile On-chip Peripheral Units
 - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
 - Two High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
 - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
 - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
 - One MultiCAN Module with 2CAN nodes and 64 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer
 - One General Purpose Timer Array Modules (GPTA) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 24 analog input lines for ADC
 - 2 independent kernels (ADC0, ADC1)
 - Analog supply voltage range from 3.3 V to 5 V (single supply)
 - Performance for 12 bit resolution ($@f_{\text{ADCI}} = 10 \text{ MHz}$)
- 2 different FADC input channels
- Extreme fast conversion, 21 cycles of f_{FADC} clock (262.5 ns @ $f_{\text{FADC}} = 80 \text{ MHz}$)

Summary of Features

- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 70 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1736ED)
 - multi-core debugging, real time tracing, and calibration
 - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL
- Core supply voltage of 1.5 V
- I/O voltage of 3.3 V
- Full automotive temperature range: -40° to +125°C
- Package variants:
 - PG-LQFP-144-10

Summary of Features

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1736 please refer to the “**Product Catalog Microcontrollers**”, which summarizes all available microcontroller variants.

This document describes the derivatives of the device. The [Table 1](#) enumerates these derivatives and summarizes the differences.

Table 1 TC1736 Derivative Synopsis

| Derivative | Ambient Temperature Range | PFlash | LDRAM | CPU frequency |
|---------------------|---|-----------|----------|---------------|
| SAK-TC1736-128F80HL | $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | 1 Mbyte | 36 Kbyte | 80 MHz |
| SAK-TC1736-96F40HL | $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ | 768 Kbyte | 32 Kbyte | 40 MHz |

2 Introduction

The TC1736 32-Bit Single-Chip Microcontroller is a cost-optimized version of the TC1767 32-Bit Single-Chip Microcontroller with less pin count and less functionalities. In comparison to the TC1767, the TC1736 provides:

- Less memories in general
- No PCP
- Reduced functionality of the GPTA with less I/Os
- Two CAN nodes only
- Less analog inputs
- Reduced CPU clock frequency
- No LVDS capability for MSC0 output lines

The TC1736 Emulation Device is implemented as a TC1767 emulation device in a QFP-144 package variant.

2.1 About this Document

This document is designed to be read primarily by design engineers and software engineers who need a detailed description of the interactions of the TC1736 functional units, registers, instructions, and exceptions.

This TC1736 Data Sheet describes the features of the TC1736 with respect to the TriCore Architecture. Where the TC1736 directly implements TriCore architectural functions, this manual simply refers to those functions as features of the TC1736. In all cases where this manual describes a TC1736 feature without referring to the TriCore Architecture, this means that the TC1736 is a direct implementation of the TriCore Architecture.

Where the TC1736 implements a subset of TriCore architectural features, this manual describes the TC1736 implementation, and then describes how it differs from the TriCore Architecture. The differences between the TC1736 and the TriCore Architecture are documented in the section for each subject.

2.1.1 Related Documentations

A complete description of the TriCore architecture is found in the document entitled "TriCore Architecture Manual". The architecture of the TC1736 is described separately this way because of the configurable nature of the TriCore specification: Different versions of the architecture may contain a different mix of systems components. The TriCore architecture, however, remains constant across all derivative designs in order to maintain compatibility.

This Data Sheets together with the "TriCore Architecture Manual" are required to understand the complete functionalities of the TC1736 microcontroller .

2.1.2 Text Conventions

This document uses the following text conventions for named components of the TC1736:

- Functional units of the TC1736 are given in plain UPPER CASE. For example: “The SSC supports full-duplex and half-duplex synchronous communication”.
- Pins using negative logic are indicated by an overline. For example: “The external reset pin, $\overline{\text{ESR0}}$, has dual-functionality.”.
- Bit fields and bits in registers are in general referenced as “Module_Register name.Bit field” or “Module_Register name.Bit”. For example: “The Current CPU Priority Number bit field CPU_ICR.CCPN is cleared”. Most of the register names contain a module name prefix, separated by an underscore character “_” from the actual register name (for example, “ASC0_CON”, where “ASC0” is the module name prefix, and “CON” is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.
- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name “MSGCFGn” refers to multiple “MSGCFG” registers with variable n. The boundary of the variables are always given where the register expression is first used (for example, “n = 0-31”), and may be repeated when necessary.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter “H”, as in 100_H. Binary constants are suffixed with a subscript letter “B”, as in: 111_B.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as “NAME[A:B]”, which defines a range for the named group from B to A. Individual bits, signals, or pins are given as “NAME[C]” where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].
- Units are abbreviated as follows:
 - **MHz** = Megahertz
 - **μs** = Microseconds
 - **kBaud, kbit** = 1000 characters/bits per second
 - **MBaud, Mbit** = 1,000,000 characters/bits per second
 - **Kbyte, KB** = 1024 bytes of memory
 - **Mbyte, MB** = 1048576 bytes of memory

In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576, and μ scales by .000001. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits

Introduction

per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.

- Data format quantities are defined as follows:
 - **Byte** = 8-bit quantity
 - **Half-word** = 16-bit quantity
 - **Word** = 32-bit quantity
 - **Double-word** = 64-bit quantity

2.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in [Table 2-1](#).

Table 2-1 Bit Function Terminology

| Function of Bits | Description |
|--------------------------------|---|
| Unimplemented, Reserved | <p>Register bit fields named 0 indicate unimplemented functions with the following behavior.</p> <ul style="list-style-type: none"> • Reading these bit fields returns 0. • These bit fields should be written with 0 if the bit field is defined as r or rh. • These bit fields have to be written with 0 if the bit field is defined as rw. <p>These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.</p> |
| rw | The bit or bit field can be read and written. |
| rwh | As rw, but bit or bit field can be also set or reset by hardware. |
| r | The bit or bit field can only be read (read-only). |
| w | The bit or bit field can only be written (write-only). A read to this register will always give a default value back. |
| rh | This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field. |

Introduction

Table 2-1 Bit Function Terminology (cont'd)

| Function of Bits | Description |
|------------------|---|
| s | Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”. |
| f | Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values. |

2.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in [Table 2-2](#) are used.

Table 2-2 Access Terms

| Symbol | Description |
|--------|--|
| U | Access Mode: Access permitted in User Mode 0 or 1. Reset Value: Value or bit is not changed by a reset operation. |
| SV | Access permitted in Supervisor Mode. |
| R | Read-only register. |
| 32 | Only 32-bit word accesses are permitted to this register/address range. |
| E | Endinit-protected register/address. |
| PW | Password-protected register/address. |
| NC | No change, indicated register is not changed. |
| BE | Indicates that an access to this address range generates a Bus Error. |
| nBE | Indicates that no Bus Error is generated when accessing this address range, even though it is either an access to an undefined address or the access does not follow the given rules. |
| nE | Indicates that no Error is generated when accessing this address or address range, even though the access is to an undefined address or address range. True for CPU accesses (MTCR/MFCR) to undefined addresses in the CSFR range. |

2.1.5 Abbreviations and Acronyms

The following acronyms and terms are used in this document:

| | |
|--------|--|
| ADC | Analog-to-Digital Converter |
| AGPR | Address General Purpose Register |
| ALU | Arithmetic and Logic Unit |
| ASC | Asynchronous/Synchronous Serial Controller |
| BCU | Bus Control Unit |
| BROM | Boot ROM & Test ROM |
| CAN | Controller Area Network |
| CISC | Complex Instruction Set Computing |
| CPS | CPU Slave Interface |
| CPU | Central Processing Unit |
| CSA | Context Save Area |
| CSFR | Core Special Function Register |
| DAP | Device Access Port |
| DAS | Device Access Server |
| DFLASH | Data Flash Memory |
| DGPR | Data General Purpose Register |
| DMA | Direct Memory Access |
| DMI | Data Memory Interface |
| ERU | External Request Unit |
| EMI | Electro-Magnetic Interference |
| FADC | Fast Analog-to-Digital Converter |
| FAM | Flash Array Module |
| FCS | Flash Command State Machine |
| FIM | Flash Interface and Control Module |
| FPI | Flexible Peripheral Interconnect (Bus) |
| FPU | Floating Point Unit |
| GPIO | General Purpose Input/Output |
| GPR | General Purpose Register |
| GPTA | General Purpose Timer Array |

| | |
|--------|--------------------------------------|
| ICACHE | Instruction Cache |
| I/O | Input / Output |
| JTAG | Joint Test Action Group = IEEE1149.1 |
| LBCU | Local Memory Bus Control Unit |
| LDRAM | Local Data RAM |
| LFI | Local Memory-to-FPI Bus Interface |
| LMB | Local Memory Bus |
| LTC | Local Timer Cell |
| MLI | Micro Link Interface |
| MMU | Memory Management Unit |
| MSB | Most Significant Bit |
| MSC | Micro Second Channel |
| NC | Non-Connected |
| NMI | Non-Maskable Interrupt |
| OCDS | On-Chip Debug Support |
| OVRAM | Overlay Memory |
| PMU | Program Memory Unit |
| PLL | Phase Locked Loop |
| PFLASH | Program Flash Memory |
| PMI | Program Memory Interface |
| PMU | Program Memory Unit |
| RAM | Random Access Memory |
| RISC | Reduced Instruction Set Computing |
| SBCU | System Peripheral Bus Control Unit |
| SCU | System Control Unit |
| SFR | Special Function Register |
| SPB | System Peripheral Bus |
| SPRAM | Scratch-Pad RAM |
| SRAM | Static Data Memory |
| SRN | Service Request Node |
| SSC | Synchronous Serial Controller |

| | |
|-----|----------------|
| STM | System Timer |
| WDT | Watchdog Timer |

2.2 System Architecture of the TC1736

The TC1736 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional High-level features of the TC1736 include:

- Program Memory Unit – instruction memory and instruction cache
- Serial communication interfaces – flexible synchronous and asynchronous modes
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

System Features

- Maximum CPU clock frequency: 80 MHz
- Maximum System Peripheral Bus frequency: 80 MHz

The TC1736 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a DMA controller and several on-chip peripherals. The TC1736 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1736 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1736, all these peripheral units are connected to the TriCore CPU/system via the System Peripheral Bus (SPB) and the Local Memory Bus (LMB). Several I/O lines on the TC1736 ports are reserved for these peripheral units to communicate with the external world.

2.2.1 Block Diagram

Figure 2-1 shows the block diagram of the TC1736.

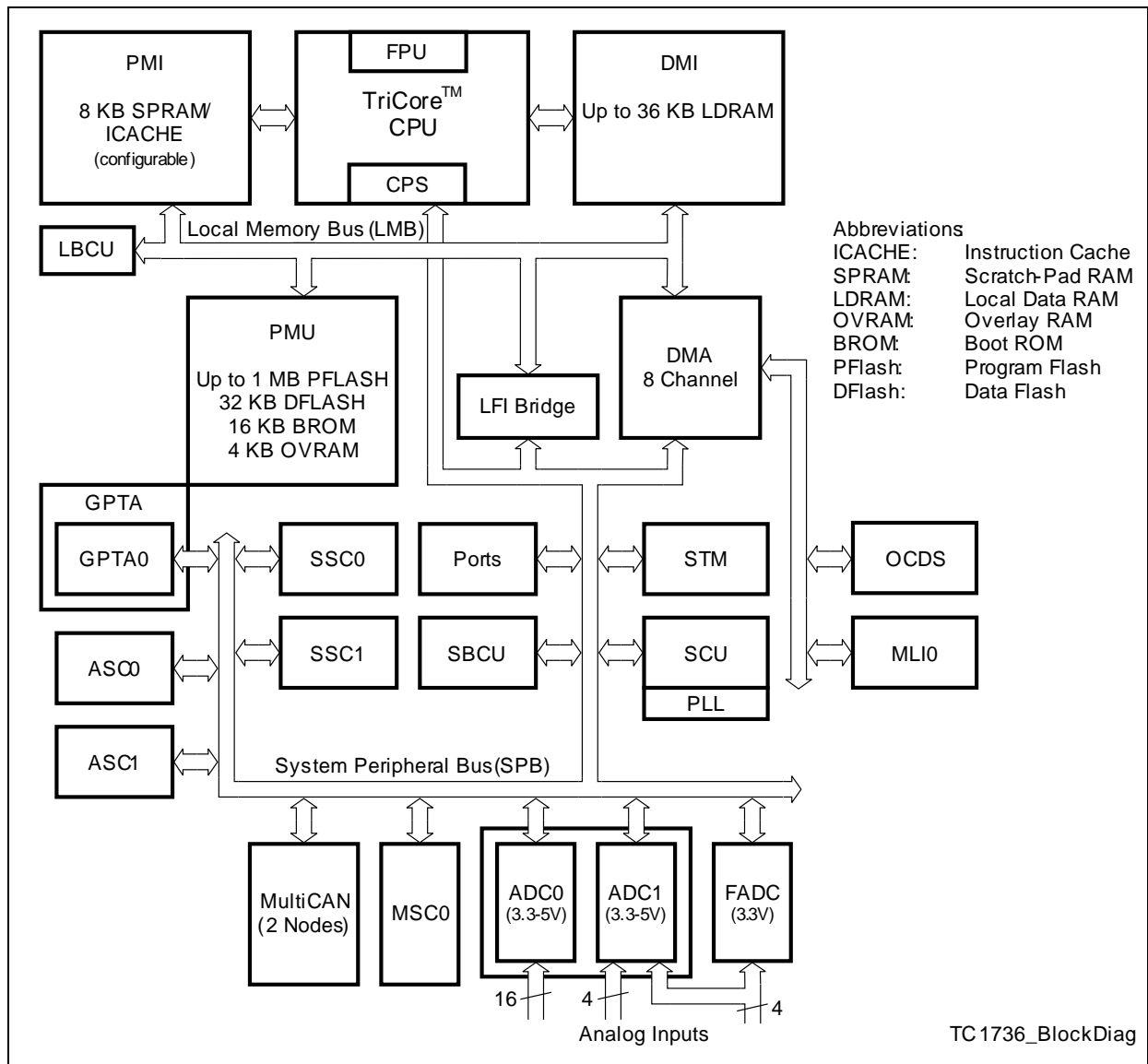


Figure 2-1 TC1736 Block Diagram

2.2.2 System Features of the TC1736 device

The TC1736 has the following features:

Packages

- PG-LQFP-144-10 package, 0.5 mm pitch

Clock Frequencies

- Maximum CPU clock frequency: 80 MHz
- Maximum SPB clock frequency: 80 MHz

2.3 High-Performance 32-Bit TriCore CPU

TriCore (TC1.3.1) Architectural Highlights

- Unified RISC MCU/DSP
- 32-bit architecture with 4 Gbytes unified data, program, and input/output address space
- Fast automatic context-switching
- Multiply-accumulate unit
- Floating point unit
- Saturating integer arithmetic
- High-performance on-chip peripheral bus (FPI Bus)
- Register based design with multiple variable register banks
- Bit handling
- Packed data operations
- Zero overhead loop
- Precise exceptions
- Flexible power management

High-Efficiency TriCore Instruction Set

- 16/32-bit instructions for reduced code size
- Data types include: Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double-word integers, and IEEE-754 single-precision floating point
- Data formats include: Bit, 8-bit byte, 16-bit half-word, 32-bit word, and 64-bit double-word data formats
- Powerful instruction set
- Flexible and efficient addressing mode for high code density

Integrated CPU related On-Chip Memories

- 8 KB instruction memory
 - configurable as SPRAM and ICACHE in 4 KB granularity
- Up to 36 KB data memory (LDRAM)
- On-chip SRAMs with parity error detection

2.4 On-Chip System Units

The TC1736 32-Bit Single-Chip Microcontroller offers several versatile on-chip system peripheral units such as DMA controller, embedded Flash module, interrupt system and ports.

2.4.1 Flexible Interrupt System

The TC1736 includes a programmable interrupt system with the following features:

Features

- Fast interrupt response
- Hardware arbitration
- Programmable service request nodes (SRNs)
- Flexible interrupt-prioritizing scheme with 255 interrupt priority levels per SRN to choose from
- Each SRN is mapped to the CPU interrupt system

2.4.2 Direct Memory Access Controller

The TC1736 includes a fast and flexible DMA controller with 8 independent DMA channels (one DMA engine).

Features

- independent DMA channels
 - Up to 16 selectable request inputs per DMA channel
 - 2-level programmable priority of DMA channels within the DMA Sub-Block
 - Software and hardware DMA request
 - Hardware requests by selected on-chip peripherals and external inputs
- 3-level programmable priority of the DMA Sub-Block at the on-chip bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
 - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
 - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
 - Programmable address modification
 - Two shadow register modes (with or without automatic re-set and direct write access).
- Full 32-bit addressing capability of each DMA channel
 - 4 Gbyte address range
 - Data block move supports > 32 Kbyte per DMA transaction
 - Circular buffer addressing mode with flexible circular buffer sizes

Introduction

- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel
 - Source and destination address register
 - Channel control and status register
 - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channel is also implemented in the DMA module)
- DMA module is working on FPI frequency, LMB interface on LMB frequency.
- Dependant on the target/destination address, Read/write requests from the Move Engine are directed to the FPI, LMB, MLI or to the the Cerberus.

2.4.3 System Timer

The TC1736's STM is designed for global system timing applications requiring both high precision and long range.

Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by maximum 80 MHz ($= f_{\text{SYS}}$, default after reset $= f_{\text{SYS}}/2$)
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM registers are not reset.¹⁾
- STM can be halted in debug/suspend mode

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum clock period is $2^{56} \times f_{\text{STM}}$. At $f_{\text{STM}} = 80$ MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1736 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The STM can also be read in sections from seven registers, STM_TIM0 through STM_TIM6, that select increasingly higher-order 32-bit ranges of the STM. These can be viewed as individual 32-bit timers, each with a different resolution and timing range.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Service requests

1) "STM registers" means all registers except STM_CLC, STM_SRC0, and STM_SRC1.

Introduction

can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

Figure 2-2 provides an overview on the STM module. It shows the options for reading parts of STM content.

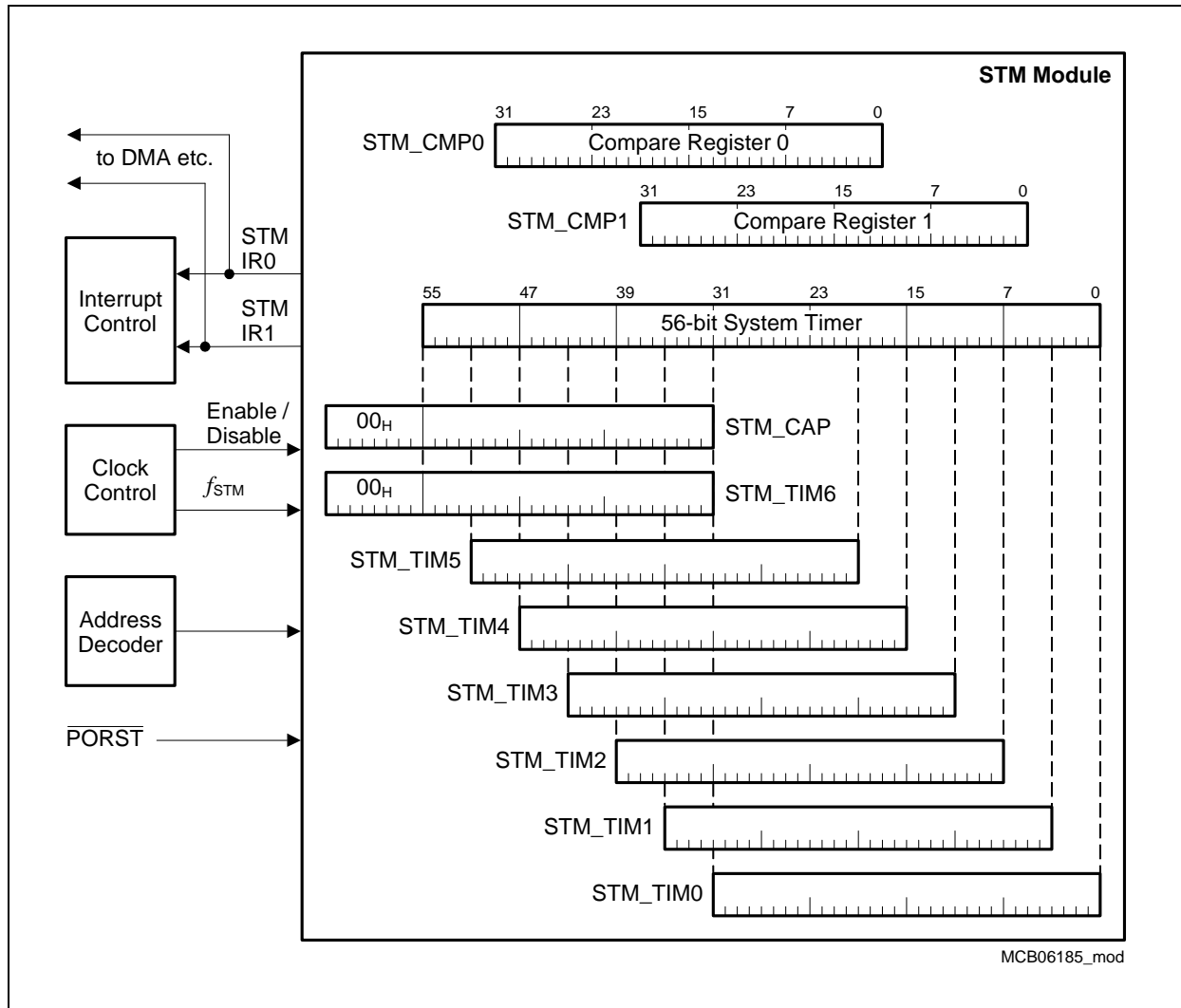


Figure 2-2 General Block Diagram of the STM Module Registers

2.4.4 System Control Unit

The following SCU introduction gives an overview about the TC1736 System Control Unit (SCU).

2.4.4.1 Clock Generation Unit

The Clock Generation Unit (CGU) allows a very flexible clock generation for the TC1736. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption.

2.4.4.2 Features of the Watchdog Timer

The main features of the WDT are summarized here.

- 16-bit Watchdog counter
- Selectable input frequency: $f_{FPI}/256$ or $f_{FPI}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1736 is held in reset until a system / class 0 reset occurs.

2.4.4.3 Reset Operation

The following reset request triggers are available:

- 1 External power-on hardware reset request trigger; $\overline{\text{PORST}}$, (cold reset)
- 2 External System Request reset triggers; $\overline{\text{ESR0}}$ and $\overline{\text{ESR1}}$ (warm reset)
- Watchdog Timer (WDT) reset request trigger, (warm reset)
- Software reset (SW), (warm reset)
- Debug (OCDS) reset request trigger, (warm reset)
- JTAG reset (special reset)

Introduction

There are two basic types of reset request triggers:

- Trigger sources that do not depend on a clock, such as the $\overline{\text{PORST}}$. This trigger force the device into an asynchronous reset assertion independently of any clock. The activation of an asynchronous reset is asynchronous to the system clock, whereas its de-assertion is synchronized.
- Trigger sources that need a clock in order to be asserted, such as the input signals ESR0 and ESR1 , the WDT trigger, the parity trigger, or the SW trigger.

2.4.4.4 External Interface

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can be shared with other functions. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

2.4.5 General Purpose I/O Ports and Peripheral I/O Lines

The TC1736 includes a flexible Ports structure with the following features:

Features

- 70 digital General-Purpose Input/Output (GPIO) port lines
- Input/output functionality individually programmable for each port line
- Programmable input characteristics (pull-up, pull-down, no pull device)
- Programmable output driver strength for EMI minimization (weak, medium, strong)
- Programmable output characteristics (push-pull, open drain)
- Programmable alternate output functions
- Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

2.4.6 Program Memory Unit (PMU)

The devices of the AudoF family contain at least one Program Memory Unit. This is named "PMU0". Some devices contain additional PMUs which are named "PMU1", ...

In the TC1736, the PMU0 contains the following submodules:

- The Flash command and fetch control interface for Program Flash and Data Flash.
- The Overlay RAM interface with Online Data Acquisition (OLDA) support.
- The Boot ROM interface.
- The Emulation Memory interface.
- The Local Memory Bus LMB slave interface.

Following memories are controlled by and belong to the PMU0:

- 1 Mbyte of Program Flash memory (PFlash)
- 32 Kbyte of Data Flash memory (DFlash, represents 8 Kbyte EEPROM)
- 16 Kbyte of Boot ROM (BROM)
- 4 Kbyte Overlay RAM (OVRAM)

The following figure shows the block diagram of the PMU0:

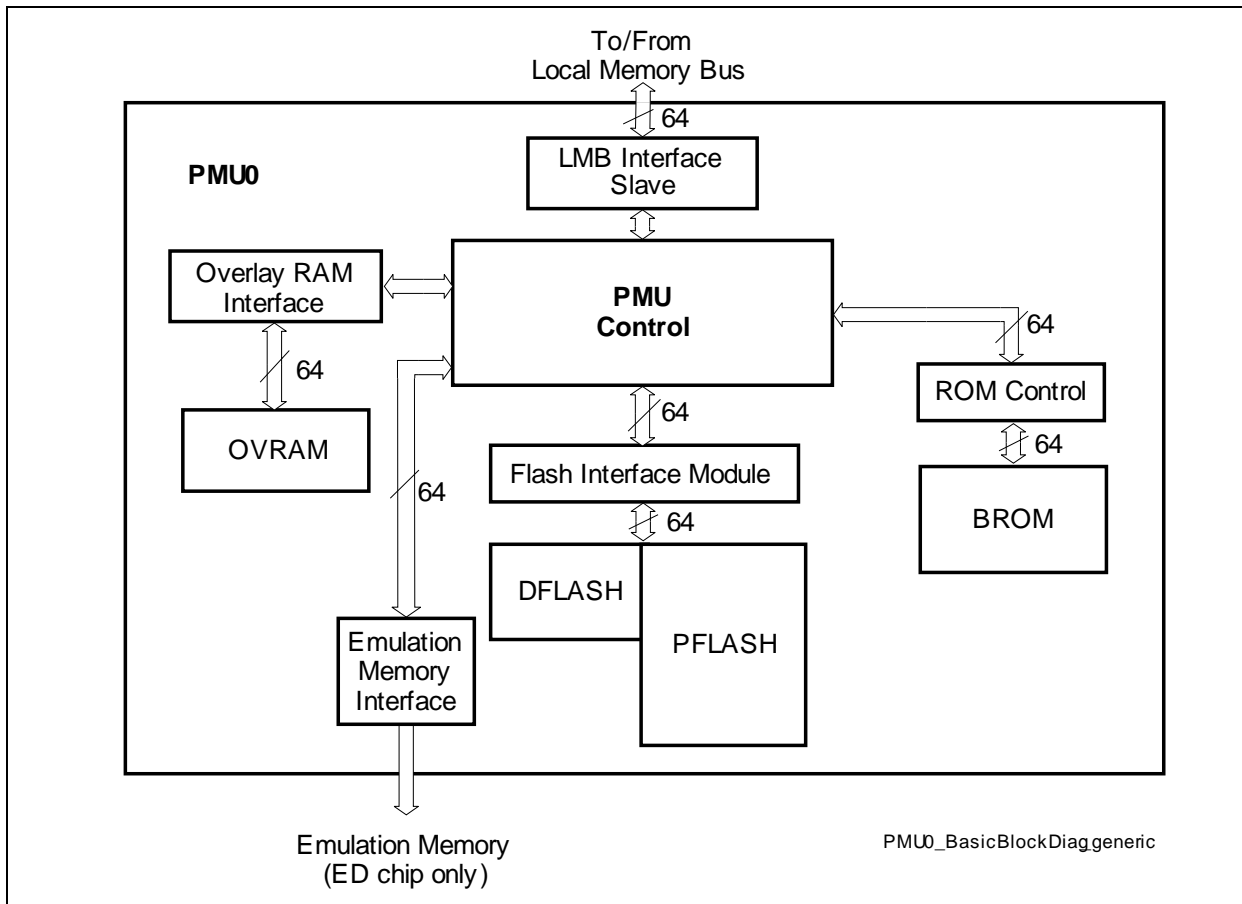


Figure 2-3 PMU0 Basic Block Diagram

2.4.6.1 Boot ROM

The internal 16 Kbyte Boot ROM (BROM) is divided into two parts, used for:

- firmware (Boot ROM), and
- factory test routines (Test ROM).

The different sections of the firmware in Boot ROM provide startup and boot operations after reset. The TestROM is reserved for special routines, which are used for testing, stressing and qualification of the component.

2.4.6.2 Overlay RAM and Data Acquisition

The overlay memory OVRAM is provided in the PMU especially for redirection of data accesses to program memory to the OVRAM by using the data overlay function. The data overlay functionality itself is controlled in the DMI module.

Introduction

For online data acquisition (OLDA) of application or calibration data a virtual 32 KB memory range is provided which can be accessed without error reporting. Accesses to this OLDA range can also be redirected to an overlay memory.

2.4.6.3 Emulation Memory Interface

In TC1736 Emulation Device, an Emulation Memory (EMEM) is provided, which can fully be used for calibration via program memory or OLDA overlay. The Emulation Memory interface shown in **Figure 2-3** is a 64-bit wide memory interface that controls the CPU-accesses to the Emulation Memory in the TC1736 Emulation Device. In the TC1736 production device, the EMEM interface is always disabled.

2.4.6.4 Tuning Protection

Tuning protection is required by the user to absolutely protect control data (e.g. for engine control), serial number and user software, stored in the Flash, from being manipulated, and to safely detect changed or disturbed data. For the internal Flash, these protection requirements are excellently fulfilled in the TC1736 with

- Flash read and write protection with user-specific protection levels, and with
- dedicated HW and firmware, supporting the internal Flash read protection, and with
- the Alternate Boot Mode.

Special tuning protection support is provided for external Flash, which must also be protected.

2.4.6.5 Program and Data Flash

The embedded Flash modules of PMU0 includes 1 Mbyte of Flash memory for code or constant data (called Program Flash) and additionally 32 Kbyte of Flash memory used for emulation of EEPROM data (called Data Flash). The Program Flash is realized as one independent Flash bank, whereas the Data Flash is built of two Flash banks, allowing the following combinations of concurrent Flash operations:

- Read code or data from Program Flash, while one bank of Data Flash is busy with a program or erase operation.
- Read data from one bank of Data Flash, while the other bank of Data Flash is busy with a program or erase operation.
- Program one bank of Data Flash while erasing the other bank of Data Flash, read from Program Flash.

Both, the Program Flash and the Data Flash, provide error correction of single-bit errors within a 64-bit read double-word, resulting in an extremely low failure rate. Read accesses to Program Flash are executed in 256-bit width, to Data Flash in 64-bit width (both plus ECC). Single-cycle burst transfers of up to 4 double-words and sequential prefetching with control of prefetch hit are supported for Program Flash.

Introduction

The minimum programming width is the page, including 256 bytes in Program Flash and 128 bytes in Data Flash. Concurrent programming and erasing in Data Flash is performed using an automatic erase suspend and resume function.

A basic block diagram of the Flash Module is shown in the following figure.

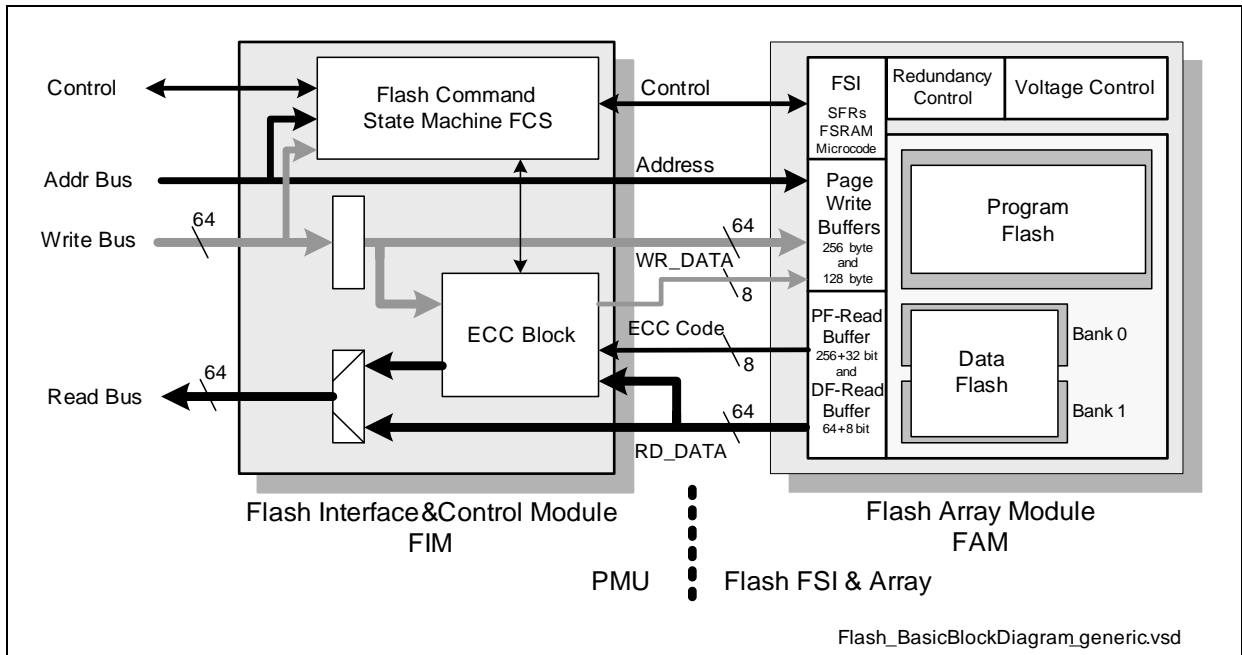


Figure 2-4 Basic Block Diagram of Flash Module

All Flash operations are controlled simply by transferring command sequences to the Flash which are based on JEDEC standard. This user interface of the embedded Flash is very comfortable, because all operations are controlled with high level commands, such as "Erase Sector". State transitions, such as termination of command execution, or errors are reported to the user by maskable interrupts. Command sequences are normally written to Flash by the CPU, but may also be issued by the DMA controller (or OCDS).

The Flash also features an advanced read/write protection architecture, including a read protection for the whole Flash array (optionally without Data Flash) and separate write protection for all sectors (only Program Flash). Write protected sectors can be made re-programmable (enabled with passwords), or they can be locked for ever (ROM function). Each sector can be assigned to up to three different users for write protection. The different users are organized hierarchically.

Program Flash Features and Functions

- 1 Mbyte on-chip Program Flash in PMU0.
- Any use for instruction code or constant data.
- 256 bit read interface (burst transfer operation).

Introduction

- Dynamic correction of single-bit errors during read access.
- Transfer rate in burst mode: One 64-bit double-word per clock cycle.
- Sector architecture:
 - Eight 16 Kbyte, one 128 Kbyte and three 256 Kbyte sectors.
 - Each sector separately erasable.
 - Each sector lockable for protection against erase and program (write protection).
- One additional configuration sector (not accessible to the user).
- Optional read protection for whole Flash, with sophisticated read access supervision. Combined with whole Flash write protection — thus supporting protection against Trojan horse programs.
- Sector specific write protection with support of re-programmability or locked forever.
- Comfortable password checking for temporary disable of write or read protection.
- User controlled configuration blocks (UCB) in configuration sector for keywords and for sector-specific lock bits (one block for every user; up to three users).
- Pad supply voltage (V_{DDP}) also used for program and erase (no VPP pin).
- Efficient 256 byte page program operation.
- All Flash operations controlled by CPU per command sequences (unlock sequences) for protection against unintended operation.
- End-of-busy as well as error reporting with interrupt and bus error trap.
- Write state machine for automatic program and erase, including verification of operation quality.
- Support of margin check.
- Delivery in erased state (read all zeros).
- Global and sector status information.
- Overlay support with SRAM for calibration applications.
- Configurable wait state selection for different CPU frequencies.
- Endurance = 1000; minimum 1000 program/erase cycles per physical sector; reduced endurance of 100 per 16 KB sector.
- Operating lifetime (incl. Retention): 20 years with endurance=1000.
- For further operating conditions see data sheet section “Flash Memory Parameters”.

Data Flash Features and Functions

- 32 Kbyte on-chip Flash, configured in two independent Flash banks of equal size.
- 64 bit read interface.
- Erase/program one bank while data read access from the other bank.
- Programming one bank while erasing the other bank using an automatic suspend/resume function.
- Dynamic correction of single-bit errors during read access.
- Sector architecture:
 - Two sectors of equal size.
 - Each sector separately erasable.
- 128 byte pages to be written in one step.

Introduction

- Operational control per command sequences (unlock sequences, same as those of Program Flash) for protection against unintended operation.
- End-of-busy as well as error reporting with interrupt and bus error trap.
- Write state machine for automatic program and erase.
- Margin check for detection of problematic Flash bits.
- Endurance = 30000 (can be device dependent); i.e. 30000 program/erase cycles per sector are allowed, with a retention of min. 5 years.
- Dedicated DFlash status information.
- Other characteristics: Same as Program Flash.

2.4.7 Data Access Overlay

The data overlay functionality provides the capability to redirect data accesses by the TriCore to program memory (internal Program Flash or external memory) to the Overlay SRAM in the PMU, or to the Emulation Memory in Emulation Device ED. This functionality makes it possible, for example, to modify the application's test and calibration parameters (which are typically stored in the program memory) during run time of a program. Note that read and write data accesses from/to program memory are redirected.

Attention: As the address translation is implemented in the DMI, it is only effective for data accesses by the TriCore. Instruction fetches by the TriCore or accesses by any other master (including the debug interface) are not affected!

Summary of Features and Functions

- 16 overlay ranges ("blocks") configurable for Program Flash and external memory
- Support of 4 Kbyte embedded Overlay SRAM (OVRAM) in PMU
- Support of up to 256 Kbyte overlay/calibration memory in Emulation Device (EMEM)
- Support of Online Data Acquisition into range of up to 32 KB and of its overlay
- Support of different overlay memory selections for every enabled overlay block
- Sizes of overlay blocks selectable from 16 byte to 2 Kbyte for redirection to OVRAM
- Sizes of overlay blocks selectable from 1 Kbyte to 128 Kbyte for redirection to EMEM
- All configured overlay ranges can be enabled with only one register write access

2.4.8 TC1736 Development Support

Overview about the TC1736 development environment:

Complete Development Support

A variety of software and hardware development tools for the 32-bit microcontroller TC1736 are available from experienced international tool suppliers. The development environment for the Infineon 32-bit microcontroller includes the following tools:

- Embedded Development Environment for TriCore Products
- The TC1736 On-chip Debug Support (OCDS) provides a JTAG port for communication between external hardware and the system
- The System Timer (STM) with high-precision, long-range timing capabilities
- The TC1736 includes a power management system, a watchdog timer as well as reset logic

2.5 On-Chip Peripheral Units

The TC1736 micro controller offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Several I/O lines on the TC1736 ports are reserved for these peripheral units to communicate with the external world.

On-Chip Peripheral Units

- Two Asynchronous/Synchronous Serial Channels (ASC0, ASC1) with baud rate generator, parity, framing and overrun error detection
- Two Synchronous Serial Channels (SSC0, SSC1) with programmable data length and shift direction
- One Micro Second Bus Interface (MSC0) for serial communication
- One CAN Module with two CAN nodes (MultiCAN) for high-efficiency data handling via FIFO buffering and gateway data transfer
- One Micro Link Serial Bus Interfaces (MLI0) for serial multiprocessor communication
- One General Purpose Timer Array (GPTA0) with a powerful set of digital signal filtering and timer functionality to accomplish autonomous and complex Input/Output management
- Two Analog-to-Digital Converter Units (ADC0, ADC1) with 8-bit, 10-bit, or 12-bit resolution.
- One fast Analog-to-Digital Converter Unit (FADC)

2.5.1 Asynchronous/Synchronous Serial Interfaces

The TC1736 includes two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1. Both ASC modules have the same functionality.

Figure 2-5 shows a global view of the Asynchronous/Synchronous Serial Interface (ASC).

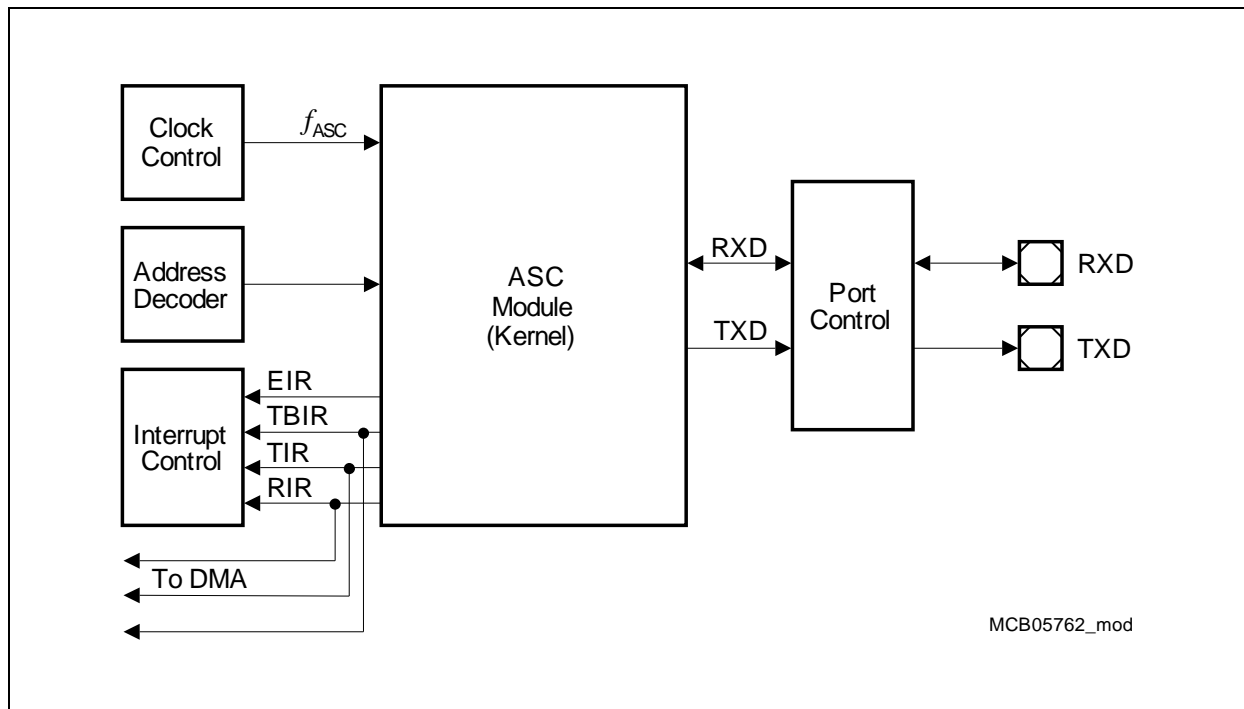


Figure 2-5 General Block Diagram of the ASC Interface

The ASC provides serial communication between the TC1736 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full-duplex asynchronous operating modes
 - 8-bit or 9-bit data frames, LSB first
 - Parity-bit generation/checking
 - One or two stop bits
 - Baud rate from 5.0 Mbit/s to 1.19 bit/s (@ 80 MHz module clock)
 - Multiprocessor mode for automatic address/data byte detection
 - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
 - Baud rate from 10.0 Mbit/s to 813.8 bit/s (@ 80 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
 - On a transmit buffer empty condition
 - On a transmit last bit of a frame condition
 - On a receive buffer full condition
 - On an error condition (frame, parity, overrun error)
- Implementation features
 - Connections to DMA Controller
 - Connections of receiver input to GPTA (LTC) for baud rate detection and LIN break signal measuring

2.5.2 High-Speed Synchronous Serial Interfaces

The TC1736 includes two High-Speed Synchronous Serial Interfaces, SSC0 and SSC1. Both SSC modules have the same functionality.

Figure 2-6 shows a global view of the Synchronous Serial interface (SSC).

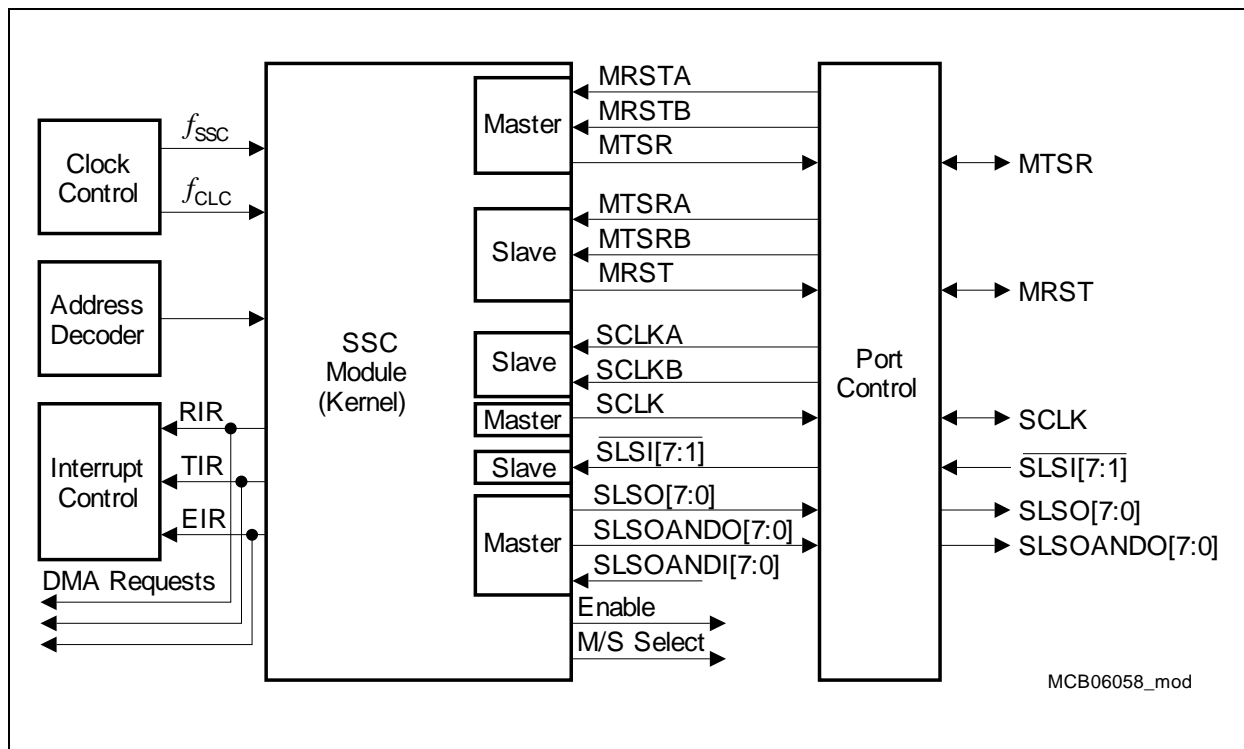


Figure 2-6 General Block Diagram of the SSC Interface

The SSC supports full-duplex and half-duplex serial synchronous communication up to 40 Mbit/s (@ 80 MHz module clock, Master Mode). The serial clock signal can be generated by the SSC itself (Master Mode) or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. One slave select input is available for slave mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode.

Features

- Master and Slave Mode operation
 - Full-duplex or half-duplex operation
 - Automatic pad control possible
- Flexible data format
 - Programmable number of data bits: 2 to 16 bits
 - Programmable shift direction: LSB or MSB shift first
 - Programmable clock polarity: Idle low or idle high state for the shift clock
 - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Baud rate generation
 - Master Mode: 40.0 Mbit/s to 610.36 bit/s (@ 80 MHz module clock)
 - Slave Mode: 20 Mbit/s to 610.36 bit/s (@ 80 MHz module clock)
- Interrupt generation
 - On a transmitter empty condition
 - On a receiver full condition
 - On an error condition (receive, phase, baud rate, transmit error)
- Flexible SSC pin configuration
- Seven slave select inputs SLSI[7:1] in Slave Mode
- Eight programmable slave select outputs SLSO in Master Mode
 - Automatic SLSO generation with programmable timing
 - Programmable active level and enable control
 - Combinable with SLSO output signals from other SSC modules

2.5.3 Micro Second Channel Interface

The Micro Second Channel (MSC) interface provides serial communication links typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 2-7** shows a global view of the interface signals of the MSC interface.

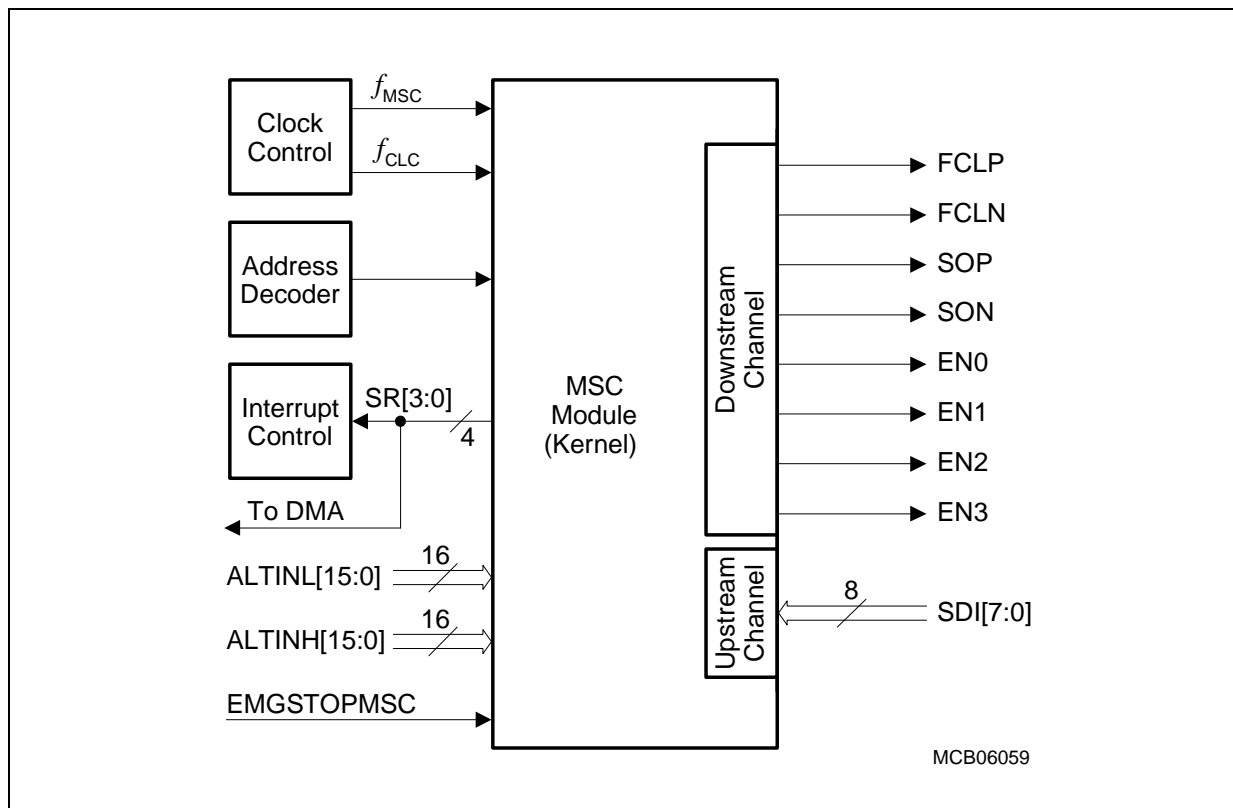


Figure 2-7 General Block Diagram of the MSC Interface

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines **SDI[7:0]** is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided on the **ALTINL/ALTINH** input lines. These input lines are typically connected with other on-chip peripheral units (for example with a timer unit such as the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in an emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
 - Serial output clock frequency: $f_{\text{FCL}} = f_{\text{MSC}}/2$ ($f_{\text{MSCmax}} = 80 \text{ MHz}$)
 - Fractional clock divider for precise frequency control of serial clock f_{MSC}
 - Command, data, and passive frame types
 - Start of serial frame: Software-controlled, timer-controlled, or free-running
 - Programmable upstream data frame length (16 or 12 bits)
 - Transmission with or without SEL bit
 - Flexible chip select generation indicates status during serial frame transmission
 - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
 - Baud rate: f_{MSC} divided by 4, 8, 16, 32, 64, 128, or 256 ($f_{\text{MSCmax}} = 80 \text{ MHz}$)
 - Standard asynchronous serial frames
 - Parity error checker
 - 8-to-1 input multiplexer for SDI lines
 - Built-in spike filter on SDI lines

2.5.4 MultiCAN Controller

The MultiCAN module provides two independent CAN nodes, representing two serial communication interfaces. The number of available message objects 64.

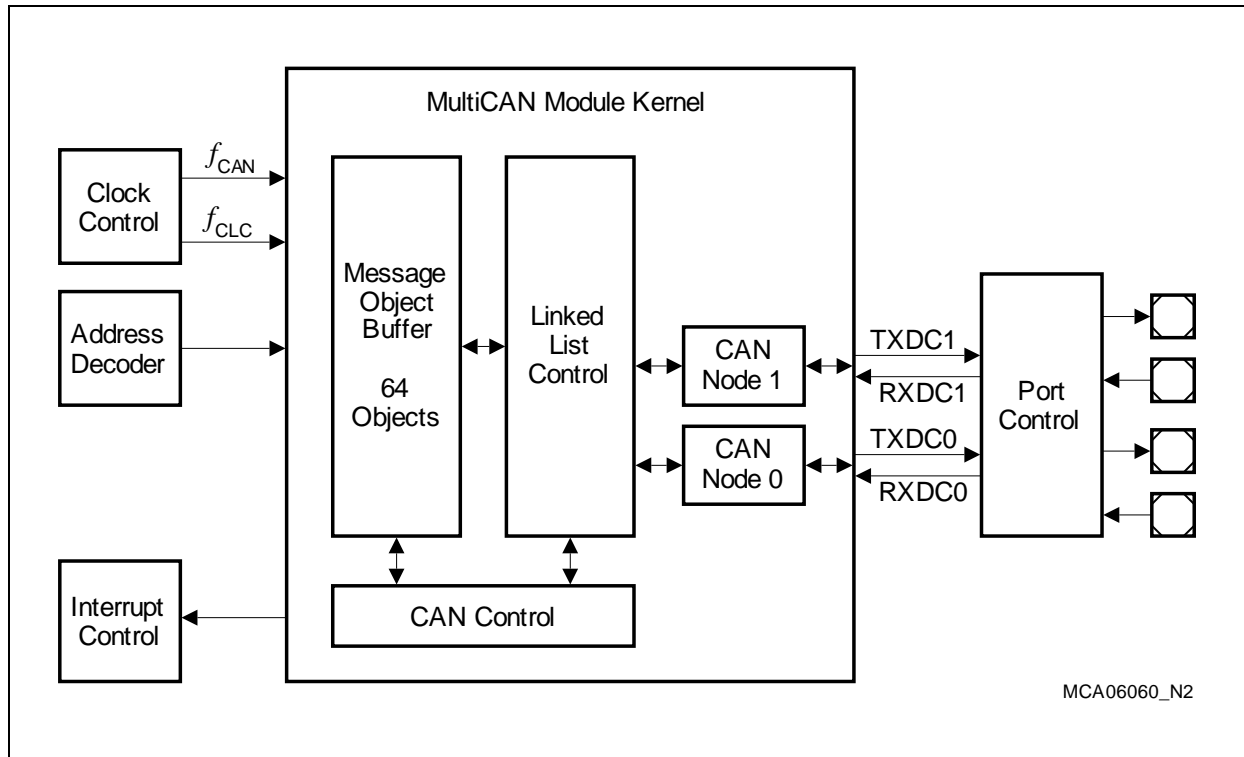


Figure 2-8 Overview of the MultiCAN Module

The MultiCAN module contains two independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All two CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

Features

- Compliant with ISO 11898
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of 64 message objects can be individually
 - Allocated (assigned) to any CAN node
 - Configured as transmit or receive object
 - Setup to handle frames with 11-bit or 29-bit identifier
 - Identified by a timestamp via a frame counter
 - Configured to remote monitoring mode
- Advanced Acceptance Filtering
 - Each message object provides an individual acceptance mask to filter incoming frames.
 - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames.
 - Message objects can be grouped into four priority classes for transmission and reception.
 - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or on its order in the list.
- Advanced message object functionality
 - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects.
 - Message objects can be linked to form a gateway that automatically transfers frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined.
- Advanced data management
 - The message objects are organized in double-chained lists.
 - List reorganizations can be performed at any time, even during full operation of the CAN nodes.
 - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list.
 - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
 - Static allocation commands offer compatibility with MultiCAN applications that are not list-based.
- Advanced interrupt handling

Introduction

- Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines.
- Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits.

2.5.5 Micro Link Interface

This TC1736 contains one Micro Link Interface, MLI0.

The Micro Link Interface (MLI) is a fast synchronous serial interface to exchange data between microcontrollers or other devices, such as stand-alone peripheral components.

Figure 2-9 shows how two microcontrollers are typically connected together via their MLI interfaces.

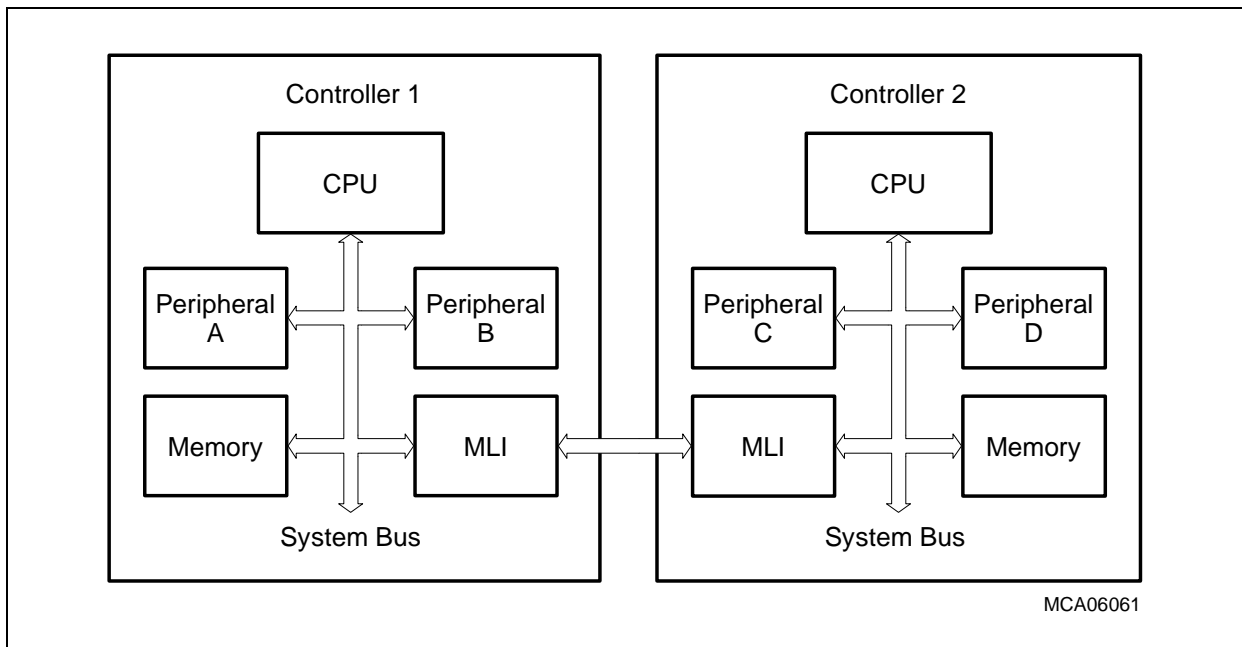


Figure 2-9 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds supported in MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target device available
- Specific frame protocol to transfer commands, addresses and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rates
 - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 40 Mbit/s @ 80 MHz module clock)
 - MLI receiver baud rate: max. f_{MLI}
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

Figure 2-10 shows a general block diagram of the MLI module.

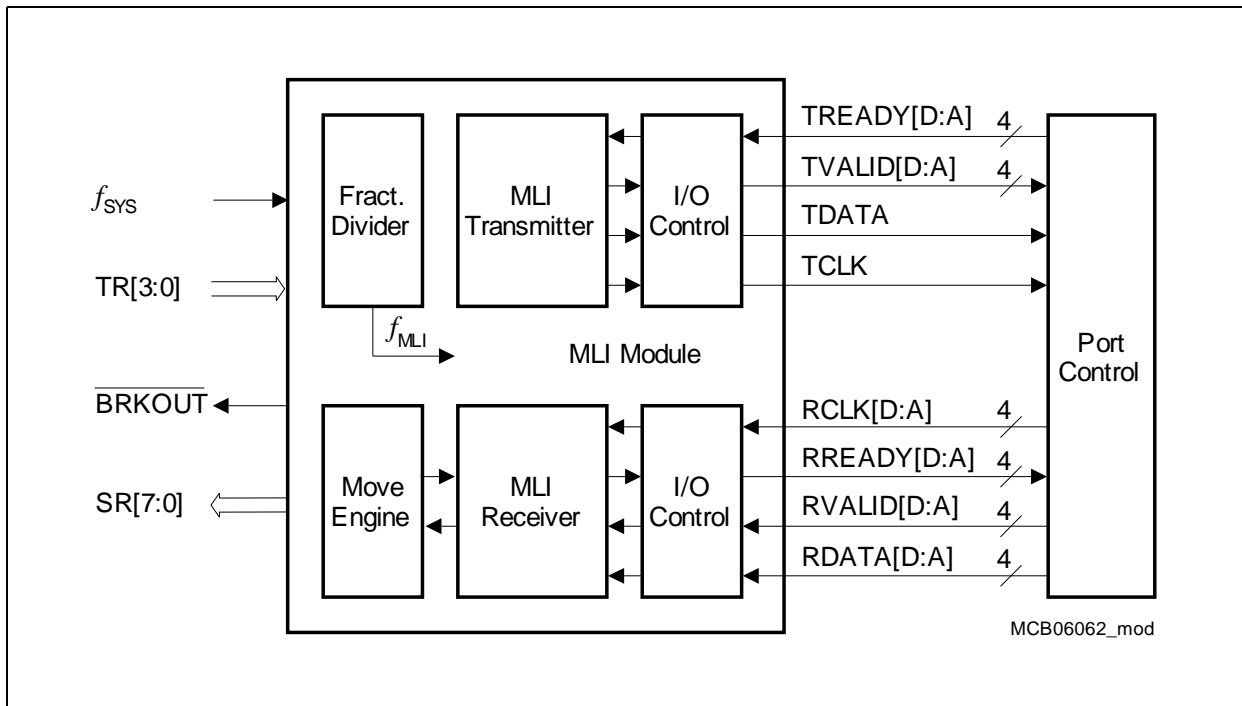


Figure 2-10 General Block Diagram of the MLI Modules

The MLI transmitter and MLI receiver communicate with other MLI receivers and MLI transmitters via a four-line serial connection each. Several I/O lines of these connections are available outside the MLI module kernel as a four-line output or input vector with index numbering A, B, C and D. The MLI module internal I/O control blocks define which signal of a vector is actually taken into account and also allow polarity inversions (to adapt to different physical interconnection means).

2.5.6 General Purpose Timer Array (GPTAv5)

The TC1736 contains the General Purpose Timer Array (GPTA0). **Figure 2-11** shows a global view of the GPTA module.

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms required for other industrial applications.

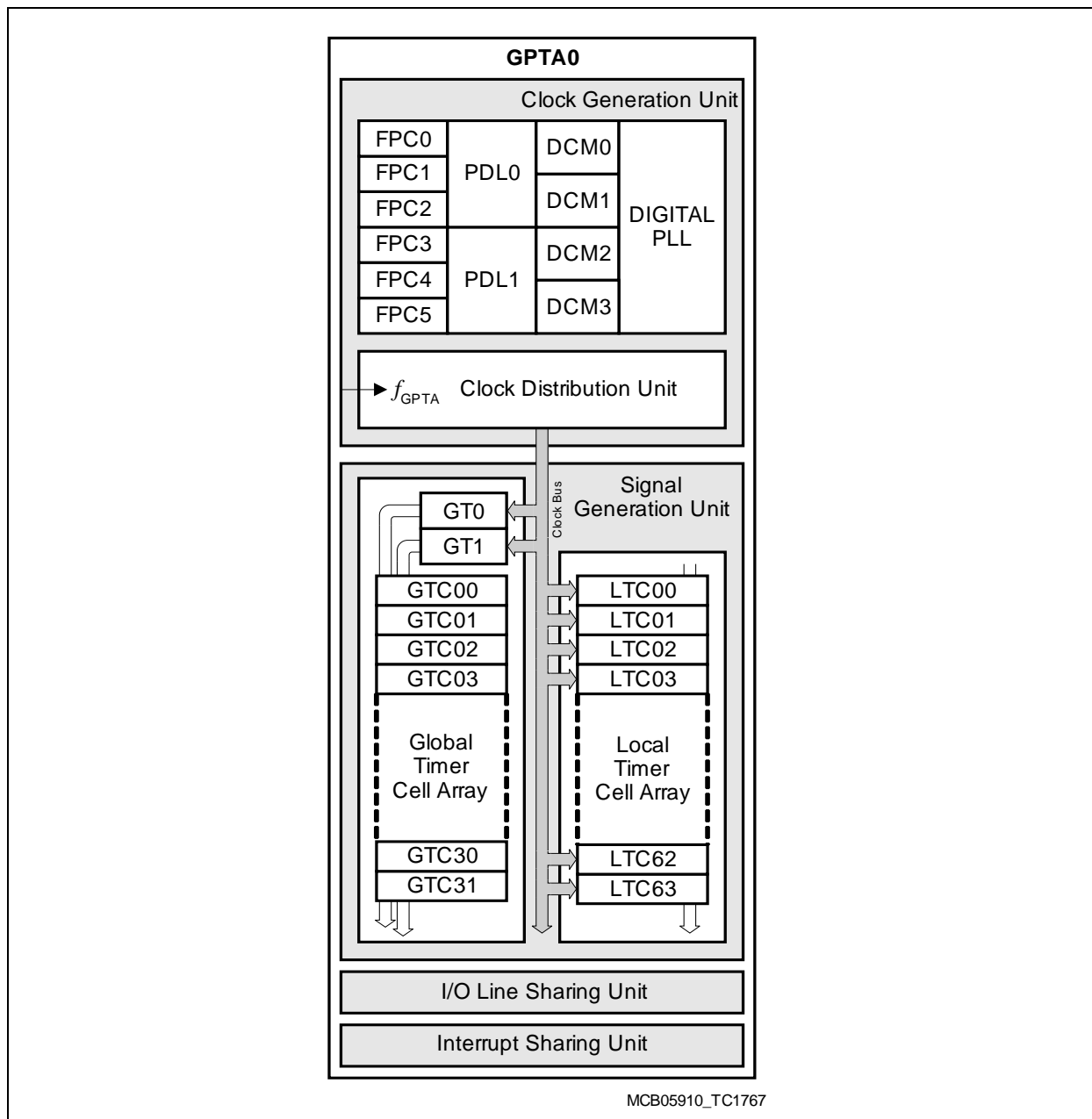


Figure 2-11 General Block Diagram of the GPTA Module in the TC1736

2.5.6.1 Functionality of GPTA0

The General Purpose Timer Array (GPTA0) provides a set of hardware modules required for high-speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.
- On-chip Trigger and Gating Signals (OTGS) can be configured to provide trigger or gating signals to integrated peripherals.

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes the specific features of the GPTA units.

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
 - Six independent units
 - Three basic operating modes:
Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
 - Selectable input sources:
Port lines, GPTA module clock, FPC output of preceding FPC cell
 - Selectable input clocks:
GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock.
 - $f_{\text{GPTA}}/2$ maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
 - Two independent units
 - Two operating modes (2- and 3- sensor signals)

Introduction

- $f_{\text{GPTA}}/4$ maximum input signal frequency in 2-sensor Mode, $f_{\text{GPTA}}/6$ maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
 - Four independent units
 - 0 - 100% margin and time-out handling
 - f_{GPTA} maximum resolution
 - $f_{\text{GPTA}}/2$ maximum input signal frequency
- Digital Phase Locked Loop (PLL)
 - One unit
 - Arbitrary multiplication factor between 1 and 65535
 - f_{GPTA} maximum resolution
 - $f_{\text{GPTA}}/2$ maximum input signal frequency
- Clock Distribution Unit (CDU)
 - One unit
 - Provides nine clock output signals:
 f_{GPTA} , divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
 - Two independent units
 - Two operating modes (Free-Running Timer and Reload Timer)
 - 24-bit data width
 - f_{GPTA} maximum resolution
 - $f_{\text{GPTA}}/2$ maximum input signal frequency
- Global Timer Cell (GTC)
 - 32 units related to the Global Timers
 - Two operating modes (Capture, Compare and Capture after Compare)
 - 24-bit data width
 - f_{GPTA} maximum resolution
 - $f_{\text{GPTA}}/2$ maximum input signal frequency
- Local Timer Cell (LTC)
 - 64 independent units
 - Three basic operating modes (Timer, Capture and Compare) for 63 units
 - Special compare modes for one unit
 - 16-bit data width
 - f_{GPTA} maximum resolution
 - $f_{\text{GPTA}}/2$ maximum input signal frequency

Interrupt Sharing Unit

- 111 interrupt sources, generating up to 38 service requests

On-chip Trigger Unit

- 16 on-chip trigger signals

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

2.5.7 Analog-to-Digital Converter (ADC0, ADC1)

The analog to digital converter module (ADC) allows the conversion of analog input values into discrete digital values based on the successive approximation method.

The module contains 2 independent kernels (ADC0, ADC1) that can operate autonomously or can be synchronized to each other. An ADC kernel is a unit used to convert an analog input signal (done by an analog part) and provides means for triggering conversions, data handling and storage (done by a digital part).

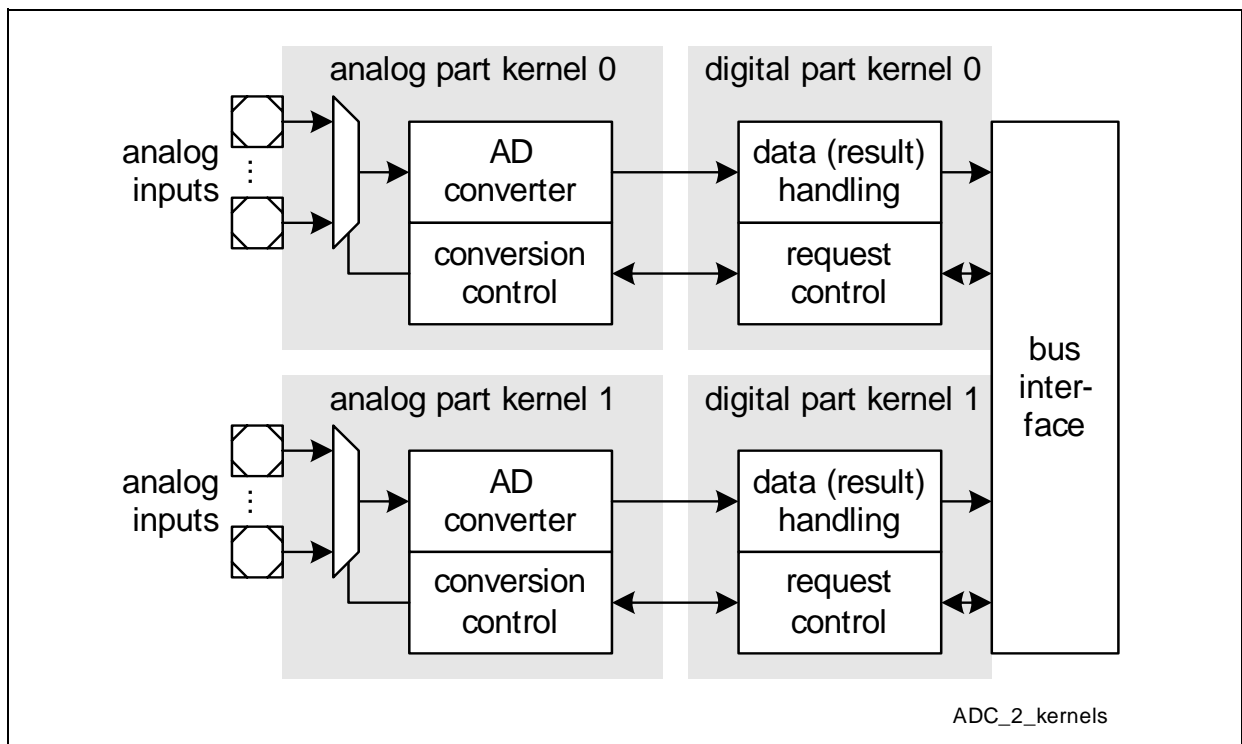


Figure 2-12 ADC Module with two ADC Kernels

Features of the Analog Part of each ADC Kernel

- Input voltage range from 0V to analog supply voltage
- Analog supply voltage range from 3.3 V to 5 V (single supply)
(5 V nominal supply voltage, performance degradation accepted for lower voltages)

Introduction

- Input multiplexer width of 16 possible analog input channels (not all of them are necessarily available on pins)
- V_{AREF} and 1 alternative reference input at channel 0
- Programmable sample time (in periods of f_{ADCI})
- Wide range of accepted analog clock frequencies f_{ADCI}
- Multiplexer test mode (channel 7 input can be connected to ground via a resistor for test purposes during run time by specific control bit)
- Power saving mechanisms

Features of the Digital Part of each ADC Kernel

- Independent result registers (16 independent registers)
- 5 conversion request sources (e.g. for external events, auto-scan, programmable sequence, etc.)
- Synchronization of the ADC kernels for concurrent conversion starts
- Control an external analog multiplexer, respecting the additional set up time
- Programmable sampling times for different channels
- Possibility to cancel running conversions on demand with automatic restart
- Flexible interrupt generation (possibility of DMA support)
- Limit checking to reduce interrupt load
- Programmable data reduction filter by adding conversion results
- Support of conversion data FIFO
- Support of suspend and power down modes
- Individually programmable reference selection for each channel (with exception of dedicated channels always referring to V_{AREF})

2.5.8 Fast Analog to Digital Converter (FADC)

General Features

- Extreme fast conversion, 21 cycles of f_{FADC} clock (262.5 ns @ $f_{FADC} = 80$ MHz)
- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- Successive approximation conversion method
- Two differential input channels with impedance control overlaid with ADC1 inputs
- Each differential input channel can also be used as single-ended input
- Offset and gain calibration support for each channel
- Programmable gain of 1, 2, 4, or 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable digital anti-aliasing and data reduction filter block with four independent filter units

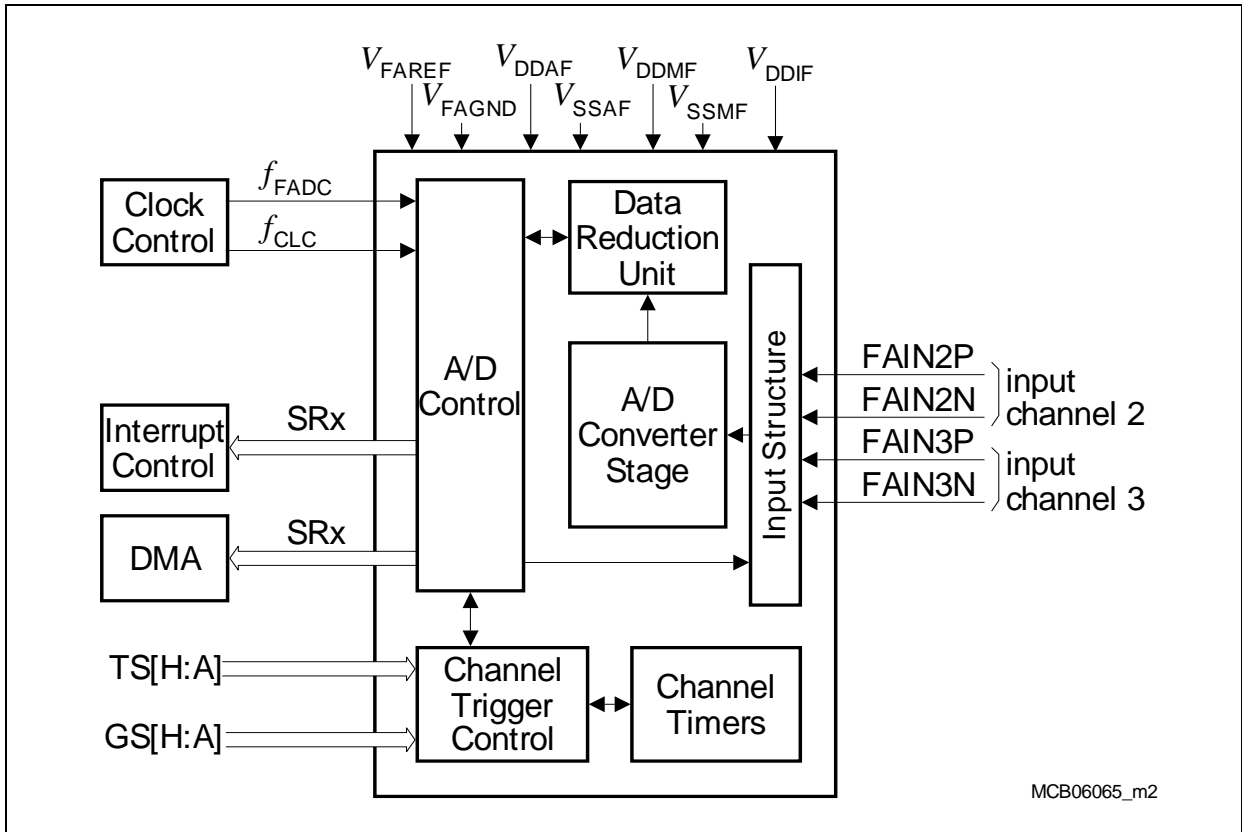


Figure 2-13 Block Diagram of the FADC Module with 2 Input Channels

Introduction

As shown in **Figure 2-13**, the main FADC functional blocks are:

- An Input Structure containing the differential inputs and impedance control.
- An A/D Converter Stage responsible for the analog-to-digital conversion including an input multiplexer to select between the channel amplifiers
- A Data Reduction Unit containing programmable anti-aliasing and data reduction filters
- A Channel Trigger Control block determining the trigger and gating conditions for the FADC channels
- A Channel Timer for each channel to independently trigger the conversions
- An A/D Control block responsible for the overall FADC functionality

FADC Power Supply and References

The FADC module is supplied by the following power supply and reference voltage lines:

- V_{DDMF} / V_{SSMF} : FADC Analog Channel Amplifier Power Supply (3.3 V)
- V_{DDIF} / V_{SSMF} : FADC Analog Input Stage Power Supply (3.3 - 5 V), the V_{DDIF} supply does not appear as supply pin, because it is internally connected to the V_{DDM} supply of the ADC that is sharing the FADC input pins.
- V_{DDAF} / V_{SSAF} : FADC Analog Part Power Supply (1.5 V), to be fed in externally
- V_{FAREF} / V_{FAGND} : FADC Reference Voltage (3.3 V max.) and FADC Reference Ground

Input Structure

The input structure of the FADC in the TC1736 contains:

- A differential analog input stage for each input channel to select the input impedance (differential or single-ended measurement) and to decouple the FADC input signal from the pins.
- Input channels 2 and 3 are overlaid with ADC1 input signals (AN28, AN29, AN30, AN31).
- A channel amplifier for each input channel with a settling time (about 5 μ s) when changing the characteristics of an input stage (changing between unused, differential, single-ended N, or single-ended P mode).

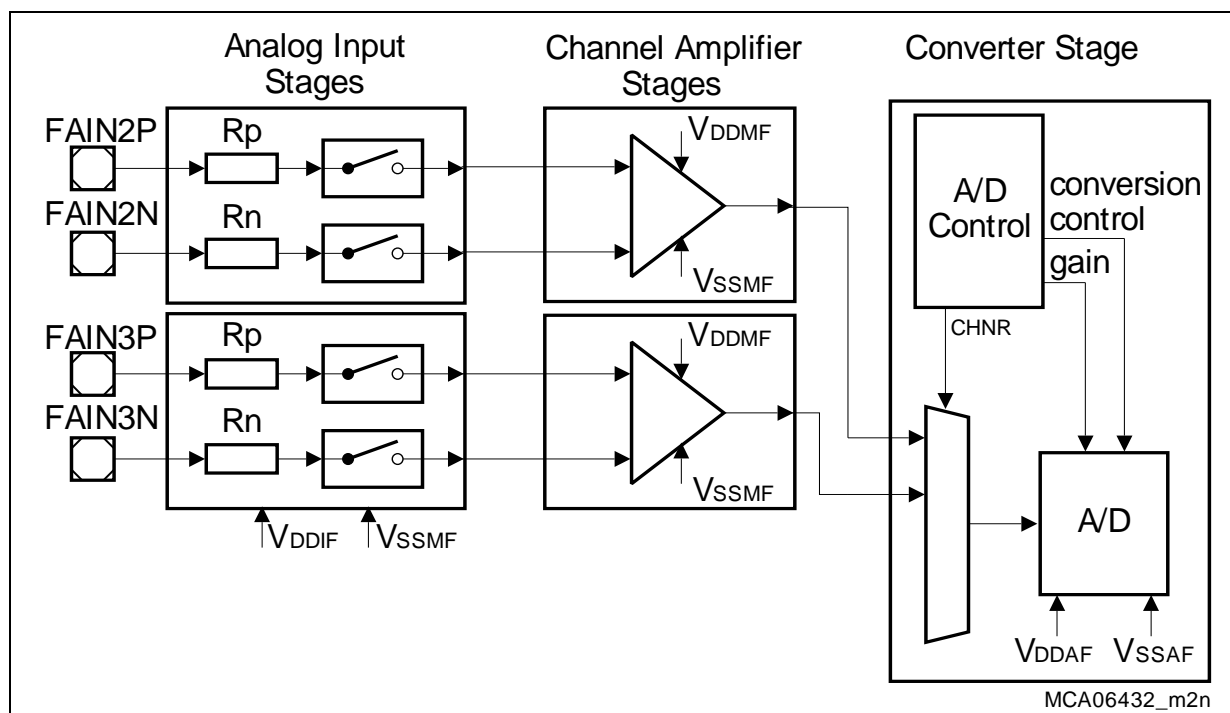


Figure 2-14 FADC Input Structure in TC1736

2.6 On-Chip Debug Support (OCDS)

The TC1736 contains resources for different kinds of “debugging”, covering needs from software development to real-time-tuning. These resources are either embedded in specific modules (e.g. breakpoint logic of the TriCore) or part of a central peripheral (known as CERBERUS).

2.6.1 On-Chip Debug Support

The classic software debug approach (start/stop, single-stepping) is supported by several features labelled “OCDS Level 1”:

- Run/stop and single-step execution for TriCore.
- Means to request all kinds of reset without usage of sideband pins.
- Halt-after-Reset for repeatable debug sessions.
- Different Boot modes to use application software not yet programmed to the Flash.
- A total of four hardware breakpoints for the TriCore based on instruction address, data address or combination of both.
- Unlimited number of software breakpoints (DEBUG instruction) for TriCore.
- Debug event generated by access to a specific address via the system peripheral bus.
- Tool access to all SFRs and internal memories independent of the Core.
- Two central Break Switches to collect debug events from all modules (TriCore, DMA, BCU, break input pins) and distribute them selectively to breakable modules (TriCore, break output pins).
- Central Suspend Switch to suspend parts of the system (TriCore, Peripherals) instead of breaking them as reaction to a debug event.
- Dedicated interrupt resources to handle debug events inside TriCore (breakpoint trap, software interrupt) and Cerberus, e.g. for implementing Monitor programs.
- Access to all OCDS Level 1 resources also for TriCore for debug tools integrated into the application code.
- Triggered Transfer of data in response to a debug event; if target is programmed to be a device interface simple variable tracing can be done.
- In depth performance analysis and profiling support given by the Emulation Device through MCDS Event Counters driven by a variety of trigger signals (e.g. cache hit, wait state, interrupt accepted).

2.6.2 Real Time Trace

For detailed tracing of the system’s behavior a pin-compatible Emulation Device will be available.¹⁾

1) The OCDS L2 interface of AudoNG is not available.

2.6.3 Calibration Support

Two main use cases are catered for by resources in addition the OCDS Level 1 infrastructure: Overlay of non-volatile on-chip memory and non-intrusive signaling:

- 4 KB SRAM for Overlay.
- Can be split into up to 16 blocks which can overlay independent regions of on-chip Data Flash.
- Changing the configuration is triggered by a single SFR access to maintain consistency.
- Overlay configuration switch does not require the TriCore to be stopped or suspended.
- Invalidation of the Data Cache (maintaining write-back data) can be done concurrently with the same SFR.
- 256 KB additional Overlay RAM on Emulation Device, shared with the trace functionality.
- A dedicated trigger SFR with 32 independent status bits is provided to centrally post requests from application code to the host computer.
- The host is notified automatically when the trigger SFR is updated by the TriCore. No polling via a system bus is required.

2.6.4 Tool Interfaces

Three options exist for the communication channel between Tools (e.g. Debugger, Calibration Tool) and TC1736:

- Two wire DAP (Device Access Port) protocol for long connections or noisy environments.
- Four (or five) wire JTAG (IEEE 1149.1) for standardized manufacturing tests.
- CAN (plus software linked into the application code) for low bandwidth deeply embedded purposes.
- DAP and JTAG are clocked by the tool.
- Bit clock up to 40 MHz for JTAG, up to 80 MHz for DAP.
- Hot attach (i.e. physical disconnect/reconnect of the host connection without reset of the TC1736) for all interfaces.
- Infineon standard DAS (Device Access Server) implementation for seamless, transparent tool access over any supported interface.
- Lock mechanism to prevent unauthorized tool access to critical application code.

2.6.5 Self-Test Support

Some manufacturing tests can be invoked by the application (e.g. after power-on) if needed:

- Hardware-accelerated checksum calculation (e.g. for Flash content).

2.6.6 FAR Support

To efficiently locate and identify faults after integration of a TC1736 into a system special functions are available:

- Boundary Scan (IEEE 1149.1) via JTAG and DAP.
- SSCM (Single Scan Chain Mode¹⁾) for structural scan testing of the chip itself.

1) This function requires access to some device pins (e.g. $\overline{\text{TESTMODE}}$) in addition to those needed for OCDS.

3 Pinning

3.1 TC1736 Pinning

Figure 3-1 shows the TC1736 logic symbol.

3.1.1 Logic Symbol

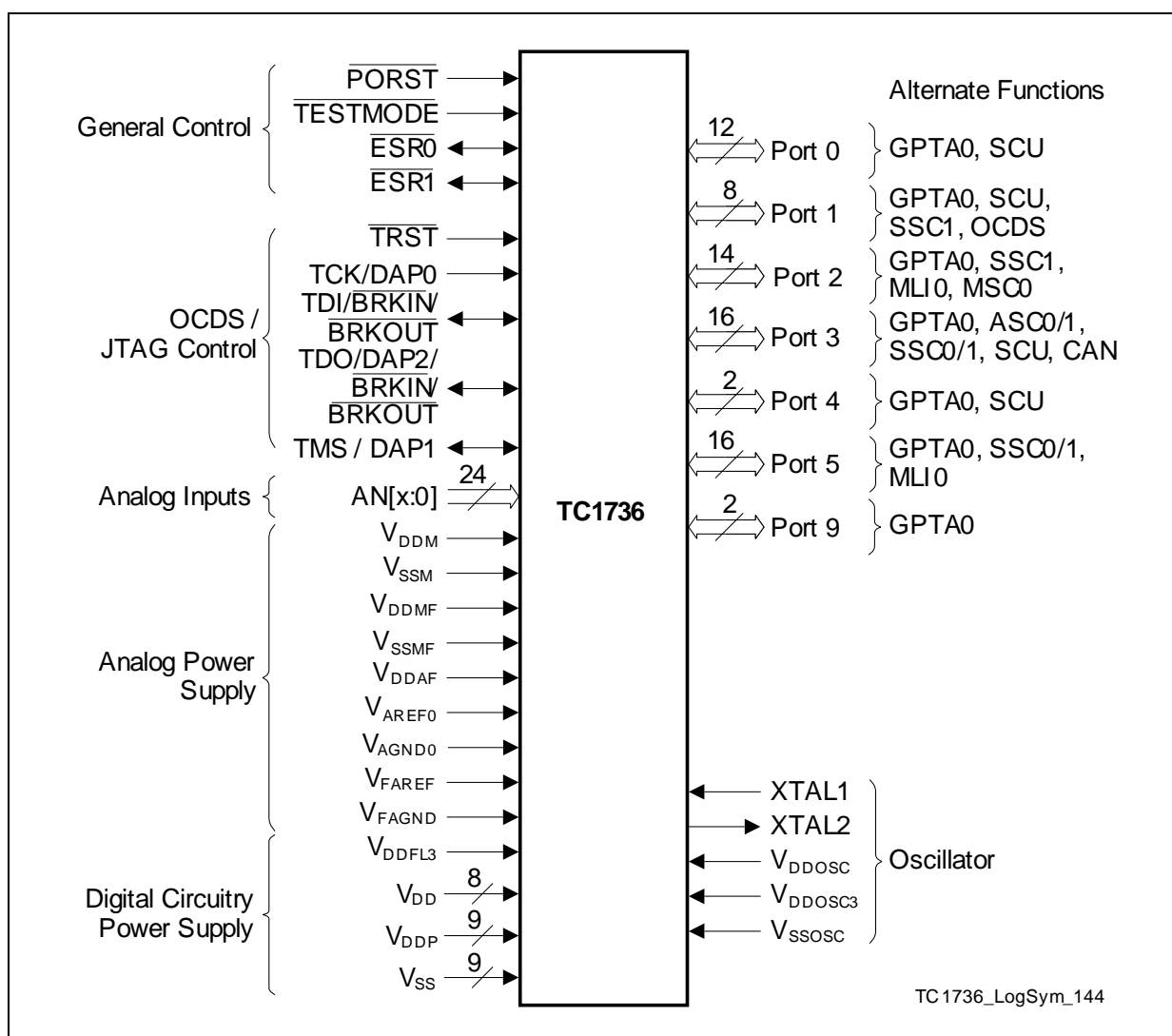


Figure 3-1 TC1736 Logic Symbol

3.1.2 Pin Configuration

Figure 3-2 shows the pin configuration of the TC1736 package PG-LQFP-144-10.

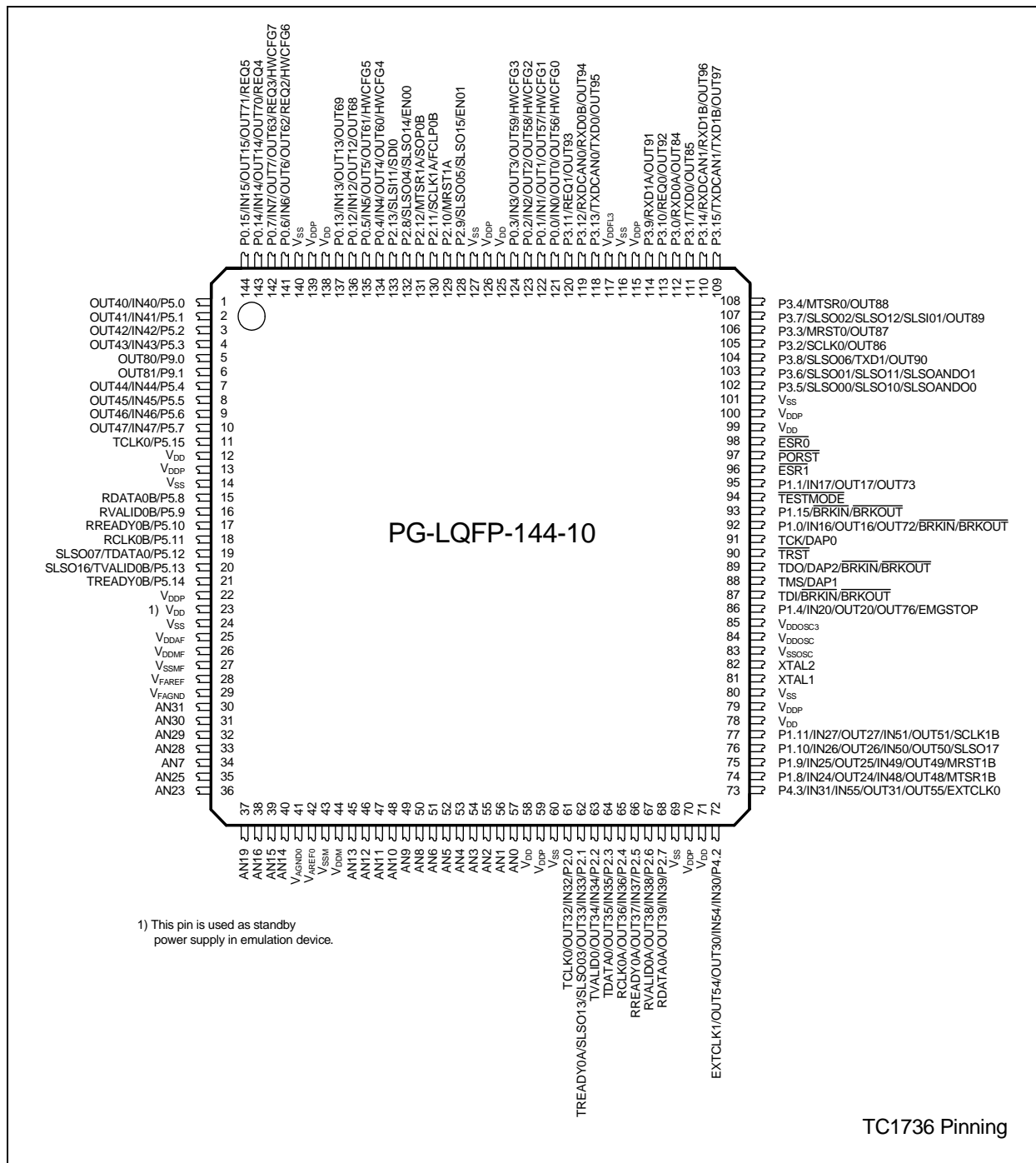


Figure 3-2 Pin Configuration of PG-LQFP-144-10 Package (top view)

3.2 Pin Definitions and Functions

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾

| Pin | Symbol | Ctrl. | Type | Function |
|---------------|----------|-------|-----------|--|
| Port 0 | | | | |
| 121 | P0.0 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 0 |
| | IN0 | I | | GPTA0 Input 0 |
| | HWCFG0 | I | | Hardware Configuration Input 0 |
| | OUT0 | O1 | | GPTA0 Output 0F |
| | OUT56 | O2 | | GPTA0 Output 56 |
| | Reserved | O3 | | – |
| 122 | P0.1 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 1 |
| | IN1 | I | | GPTA0 Input 1 |
| | HWCFG1 | I | | Hardware Configuration Input 1 |
| | OUT1 | O1 | | GPTA0 Output 1 |
| | OUT57 | O2 | | GPTA0 Output 57 |
| | Reserved | O3 | | – |
| 123 | P0.2 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 2 |
| | IN2 | I | | GPTA0 Input 2 |
| | HWCFG2 | I | | Hardware Configuration Input 2 |
| | OUT2 | O1 | | GPTA0 Output 2 |
| | OUT58 | O2 | | GPTA0 Output 58 |
| | Reserved | O3 | | – |
| 124 | P0.3 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 3 |
| | IN3 | I | | GPTA0 Input 3 |
| | HWCFG3 | I | | Hardware Configuration Input 3 |
| | OUT3 | O1 | | GPTA0 Output 3 |
| | OUT59 | O2 | | GPTA0 Output 59 |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|--|
| 134 | P0.4 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 4 |
| | IN4 | I | | GPTA0 Input 4 |
| | HWCFG4 | I | | Hardware Configuration Input 4 |
| | OUT4 | O1 | | GPTA0 Output 4 |
| | OUT60 | O2 | | GPTA0 Output 60 |
| | Reserved | O3 | | – |
| 135 | P0.5 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 5 |
| | IN5 | I | | GPTA0 Input 5 |
| | HWCFG5 | I | | Hardware Configuration Input 5 |
| | OUT5 | O1 | | GPTA0 Output 5 |
| | OUT61 | O2 | | GPTA0 Output 61 |
| | Reserved | O3 | | – |
| 141 | P0.6 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 6 |
| | IN6 | I | | GPTA0 Input 6 |
| | HWCFG6 | I | | Hardware Configuration Input 6 |
| | REQ2 | I | | External Request Input 2 |
| | OUT6 | O1 | | GPTA0 Output 6 |
| | OUT62 | O2 | | GPTA0 Output 62 |
| | Reserved | O3 | | – |
| 142 | P0.7 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 7 |
| | IN7 | I | | GPTA0 Input 7 |
| | HWCFG7 | I | | Hardware Configuration Input 7 |
| | REQ3 | I | | External Request Input 3 |
| | OUT7 | O1 | | GPTA0 Output 7 |
| | OUT63 | O2 | | GPTA0 Output 63 |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|---|
| 136 | P0.12 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 12 |
| | IN12 | I | | GPTA0 Input 12 |
| | OUT12 | O1 | | GPTA0 Output 12 |
| | OUT68 | O2 | | GPTA0 Output 68 |
| | Reserved | O3 | | – |
| 137 | P0.13 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 13 |
| | IN13 | I | | GPTA0 Input 13 |
| | OUT13 | O1 | | GPTA0 Output 13 |
| | OUT69 | O2 | | GPTA0 Output 69 |
| | Reserved | O3 | | – |
| 143 | P0.14 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 14 |
| | IN14 | I | | GPTA0 Input 14 |
| | REQ4 | I | | External Request Input 4 |
| | OUT14 | O1 | | GPTA0 Output 14 |
| | OUT70 | O2 | | GPTA0 Output 70 |
| | Reserved | O3 | | – |
| 144 | P0.15 | I/O0 | A1/ PU | Port 0 General Purpose I/O Line 15 |
| | IN15 | I | | GPTA0 Input 15 |
| | REQ5 | I | | External Request Input 5 |
| | OUT15 | O1 | | GPTA0 Output 15 |
| | OUT71 | O2 | | GPTA0 Output 71 |
| | Reserved | O3 | | – |

Port 1

| | | | | |
|----|----------|------|-----------|--|
| 92 | P1.0 | I/O0 | A2/ PU | Port 1 General Purpose I/O Line 0 |
| | IN16 | I | | GPTA0 Input 16 |
| | BRKIN | I | | OCDS Break Input |
| | OUT16 | O1 | | GPTA0 Output 16 |
| | OUT72 | O2 | | GPTA0 Output 72 |
| | Reserved | O3 | | – |
| | BRKOUT | O | | OCDS Break Output (controlled by OCDS module) |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|--|
| 95 | P1.1 | I/O0 | A1/ PU | Port 1 General Purpose I/O Line 1 |
| | IN17 | I | | GPTA0 Input 17 |
| | OUT17 | O1 | | GPTA0 Output 17 |
| | OUT73 | O2 | | GPTA0 Output 73 |
| | Reserved | O3 | | – |
| 86 | P1.4 | I/O0 | A1/ PU | Port 1 General Purpose I/O Line 4 |
| | IN20 | I | | GPTA0 Input 20 |
| | EMGSTOP | I | | Emergency Stop Input |
| | OUT20 | O1 | | GPTA0 Output 20 |
| | OUT76 | O2 | | GPTA0 Output 76 |
| | Reserved | O3 | | – |
| 74 | P1.8 | I/O0 | A2/ PU | Port 1 General Purpose I/O Line 8 |
| | IN24 | I | | GPTA0 Input 24 |
| | IN48 | I | | GPTA0 Input 48 |
| | MTSR1B | I | | SSC1 Slave Receive Input B (Slave Mode) |
| | OUT24 | O1 | | GPTA0 Output 24 |
| | OUT48 | O2 | | GPTA0 Output 48 |
| | MTSR1B | O3 | | SSC1 Master Transmit Output B (Master Mode) |
| 75 | P1.9 | I/O0 | A2/ PU | Port 1 General Purpose I/O Line 9 |
| | IN25 | I | | GPTA0 Input 25 |
| | IN49 | I | | GPTA0 Input 49 |
| | MRST1B | I | | SSC1 Master Receive Input B (Master Mode) |
| | OUT25 | O1 | | GPTA0 Output 25 |
| | OUT49 | O2 | | GPTA0 Output 49 |
| | MRST1B | O3 | | SSC1 Slave Transmit Output B (Slave Mode) |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|--|
| 76 | P1.10 | I/O0 | A2/ PU | Port 1 General Purpose I/O Line 10 |
| | IN26 | I | | GPTA0 Input 26 |
| | IN50 | I | | GPTA0 Input 50 |
| | OUT26 | O1 | | GPTA0 Output 26 |
| | OUT50 | O2 | | GPTA0 Output 50 |
| | SLSO17 | O3 | | SSC1 Slave Select Output 7 |
| 77 | P1.11 | I/O0 | A2/ PU | Port 1 General Purpose I/O Line 11 |
| | IN27 | I | | GPTA0 Input 27 |
| | IN51 | I | | GPTA0 Input 51 |
| | SCLK1B | I | | SSC1 Clock Input B |
| | OUT27 | O1 | | GPTA0 Output 27 |
| | OUT51 | O2 | | GPTA0 Output 51 |
| | SCLK1B | O3 | | SSC1 Clock Output B |
| 93 | P1.15 | I/O0 | A2/ PU | Port 1 General Purpose I/O Line 15 |
| | BRKIN | I | | OCDS Break Input |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| | BRKOUT | O | | OCDS Break Output (controlled by OCDS module) |

Port 2

| | | | | |
|----|----------|------|-----------|--|
| 61 | P2.0 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 0 |
| | IN32 | I | | GPTA0 Input 32 |
| | OUT32 | O1 | | GPTA0 Output 32 |
| | TCLK0 | O2 | | MLI0 Transmitter Clock Output 0 |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|--|
| 62 | P2.1 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 1 |
| | IN33 | I | | GPTA0 Input 33 |
| | TREADY0A | I | | MLI0 Transmitter Ready Input A |
| | OUT33 | O1 | | GPTA0 Output 33 |
| | SLSO03 | O2 | | SSC0 Slave Select Output Line 3 |
| | SLSO13 | O3 | | SSC1 Slave Select Output Line 3 |
| 63 | P2.2 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 2 |
| | IN34 | I | | GPTA0 Input 34 |
| | OUT34 | O1 | | GPTA0 Output 34 |
| | TVALID0 | O2 | | MLI0 Transmitter Valid Output |
| | Reserved | O3 | | – |
| 64 | P2.3 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 3 |
| | IN35 | I | | GPTA0 Input 35 |
| | OUT35 | O1 | | GPTA0 Output 35 |
| | TDATA0 | O2 | | MLI0 Transmitter Data Output |
| | Reserved | O3 | | – |
| 65 | P2.4 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 4 |
| | IN36 | I | | GPTA0 Input 36 |
| | RCLK0A | I | | MLI Receiver Clock Input A |
| | OUT36 | O1 | | GPTA0 Output 36 |
| | OUT36 | O2 | | GPTA0 Output 36 |
| | Reserved | O3 | | – |
| 66 | P2.5 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 5 |
| | IN37 | I | | GPTA0 Input 37 |
| | OUT37 | O1 | | GPTA0 Output 37 |
| | RREADY0A | O2 | | MLI0 Receiver Ready Output A |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|---|
| 67 | P2.6 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 6 |
| | IN38 | I | | GPTA0 Input 38 |
| | RVALID0A | I | | MLI Receiver Valid Input A |
| | OUT38 | O1 | | GPTA0 Output 38 |
| | OUT38 | O2 | | GPTA0 Output 38 |
| | Reserved | O3 | | – |
| 68 | P2.7 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 7 |
| | IN39 | I | | GPTA0 Input 39 |
| | RDATA0A | I | | MLI Receiver Data Input A |
| | OUT39 | O1 | | GPTA0 Output 39 |
| | OUT39 | O2 | | GPTA0 Output 39 |
| | Reserved | O3 | | – |
| 132 | P2.8 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 8 |
| | SLSO04 | O1 | | SSC0 Slave Select Output 4 |
| | SLSO14 | O2 | | SSC1 Slave Select Output 4 |
| | EN00 | O3 | | MSC0 Enable Output 0 |
| 128 | P2.9 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 9 |
| | SLSO05 | O1 | | SSC0 Slave Select Output 5 |
| | SLSO15 | O2 | | SSC1 Slave Select Output 5 |
| | EN01 | O3 | | MSC0 Enable Output 1 |
| 129 | P2.10 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 10 |
| | MRST1A | I | | SSC1 Master Receive Input A |
| | MRST1A | O1 | | SSC1 Slave Transmit Output |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 130 | P2.11 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 11 |
| | SCLK1A | I | | SSC1 Clock Input A |
| | SCLK1A | O1 | | SSC1 Clock Output A |
| | Reserved | O2 | | – |
| | FCLP0B | O3 | | MSC0 Clock Output Positive B |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|---|
| 131 | P2.12 | I/O0 | A2/ PU | Port 2 General Purpose I/O Line 12 |
| | MTSR1A | I | | SSC1 Slave Receive Input A |
| | MTSR1A | O1 | | SSC1 Master Transmit Output A |
| | Reserved | O2 | | – |
| | SOP0B | O3 | | MSC0 Serial Data Output Positive B |
| 133 | P2.13 | I/O0 | A1/ PU | Port 2 General Purpose I/O Line 13 |
| | SLS11 | I | | SSC1 Slave Select Input 1 |
| | SDI0 | I | | MSC0 Serial Data Input |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |

Port 3

| | | | | |
|-----|-------|------|-----------|--|
| 112 | P3.0 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 0 |
| | RXD0A | I | | ASC0 Receiver Input A (Async. & Sync. Mode) |
| | RXD0A | O1 | | ASC0 Clock Output (Synch. Mode) |
| | RXD0A | O2 | | ASC0 Clock Output (Synch. Mode) |
| | OUT84 | O3 | | GPTA0 Output 84 |
| 111 | P3.1 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 1 |
| | TXD0 | O1 | | ASC0 Transmitter Output |
| | TXD0 | O2 | | ASC0 Transmitter Output |
| | OUT85 | O3 | | GPTA0 Output 85 |
| 105 | P3.2 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 2 |
| | SCLK0 | I | | SSC0 Clock Input (Slave Mode) |
| | SCLK0 | O1 | | SSC0 Clock Output (Master Mode) |
| | SCLK0 | O2 | | SSC0 Clock Output (Master Mode) |
| | OUT86 | O3 | | GPTA0 Output 86 |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|-----------|-------|-----------|---|
| 106 | P3.3 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 3 |
| | MRST0 | I | | SSC0 Master Receive Input (Master Mode) |
| | MRST0 | O1 | | SSC0 Slave Transmit Output (Slave Mode) |
| | MRST0 | O2 | | SSC0 Slave Transmit Output (Slave Mode) |
| | OUT87 | O3 | | GPTA0 Output 87 |
| 108 | P3.4 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 4 |
| | MTSR0 | I | | SSC0 Slave Receive Input (Slave Mode) |
| | MTSR0 | O1 | | SSC0 Master Transmit Output (Master Mode) |
| | MTSR0 | O2 | | SSC0 Master Transmit Output (Master Mode) |
| | OUT88 | O3 | | GPTA0 Output 88 |
| 102 | P3.5 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 5 |
| | SLSO00 | O1 | | SSC0 Slave Select Output 0 |
| | SLSO10 | O2 | | SSC1 Slave Select Output 0 |
| | SLSOANDO0 | O3 | | SSC0 AND SSC1 Slave Select Output 0 |
| 103 | P3.6 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 6 |
| | SLSO01 | O1 | | SSC0 Slave Select Output 1 |
| | SLSO11 | O2 | | SSC1 Slave Select Output 1 |
| | SLSOANDO1 | O3 | | SSC0 AND SSC1 Slave Select Output 1 |
| 107 | P3.7 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 7 |
| | SLSI01 | I | | SSC0 Slave Select Input 1 |
| | SLSO02 | O1 | | SSC0 Slave Select Output 2 |
| | SLSO12 | O2 | | SSC1 Slave Select Output 2 |
| | OUT89 | O3 | | GPTA0 Output 89 |
| 104 | P3.8 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 8 |
| | SLSO06 | O1 | | SSC0 Slave Select Output 6 |
| | TXD1 | O2 | | ASC1 Transmitter Output |
| | OUT90 | O3 | | GPTA0 Output 90 |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|--|
| 114 | P3.9 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 9 |
| | RXD1A | I | | ASC1 Receiver Input A |
| | RXD1A | O1 | | ASC1 Receiver Output A (Synchronous Mode) |
| | RXD1A | O2 | | ASC1 Receiver Output A (Synchronous Mode) |
| | OUT91 | O3 | | GPTA0 Output 91 |
| 113 | P3.10 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 10 |
| | REQ0 | I | | External Request Input 0 |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | OUT92 | O3 | | GPTA0 Output 92 |
| 120 | P3.11 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 11 |
| | REQ1 | I | | External Request Input 1 |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | OUT93 | O3 | | GPTA0 Output 93 |
| 119 | P3.12 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 12 |
| | RXDCAN0 | I | | CAN Node 0 Receiver Input |
| | RXD0B | I | | ASC0 Receiver Input B |
| | RXD0B | O1 | | ASC0 Receiver Output B (Synchronous Mode) |
| | RXD0B | O2 | | ASC0 Receiver Output B (Synchronous Mode) |
| | OUT94 | O3 | | GPTA0 Output 94 |
| 118 | P3.13 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 13 |
| | TXDCAN0 | O1 | | CAN Node 0 Transmitter Output |
| | TXD0 | O2 | | ASC0 Transmitter Output |
| | OUT95 | O3 | | GPTA0 Output 95 |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|--------|---------|-------|-----------|---|
| 110 | P3.14 | I/O0 | A1/ PU | Port 3 General Purpose I/O Line 14 |
| | RXDCAN1 | I | | CAN Node 1 Receiver Input |
| | RXD1B | I | | ASC1 Receiver Input B |
| | RXD1B | O1 | | ASC1 Receiver Output B (Synchronous Mode) |
| | RXD1B | O2 | | ASC1 Receiver Output B (Synchronous Mode) |
| | OUT96 | O3 | | GPTA0 Output 96 |
| 109 | P3.15 | I/O0 | A2/ PU | Port 3 General Purpose I/O Line 15 |
| | TXDCAN1 | O1 | | CAN Node 1 Transmitter Output |
| | TXD1 | O2 | | ASC1 Transmitter Output |
| | OUT97 | O3 | | GPTA0 Output 97 |
| Port 4 | | | | |
| 72 | P4.2 | I/O0 | A2/ PU | Port 4 General Purpose I/O Line 2 |
| | IN30 | I | | GPTA0 Input 30 |
| | IN54 | I | | GPTA0 Input 54 |
| | OUT30 | O1 | | GPTA0 Output 30 |
| | OUT54 | O2 | | GPTA0 Output 54 |
| | EXTCLK1 | O3 | | External Clock 1 Output |
| 73 | P4.3 | I/O0 | A2/ PU | Port 4 General Purpose I/O Line 3 |
| | IN31 | I | | GPTA0 Input 31 |
| | IN55 | I | | GPTA0 Input 55 |
| | OUT31 | O1 | | GPTA0 Output 31 |
| | OUT55 | O2 | | GPTA0 Output 55 |
| | EXTCLK0 | O3 | | External Clock 0 Output |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---------------|----------|-------|-----------|--|
| Port 5 | | | | |
| 1 | P5.0 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 0 |
| | IN40 | I | | GPTA0 Input 40 |
| | OUT40 | O1 | | GPTA0 Output 40 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 2 | P5.1 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 1 |
| | IN41 | I | | GPTA0 Input 41 |
| | OUT41 | O1 | | GPTA0 Output 41 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 3 | P5.2 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 2 |
| | IN42 | I | | GPTA0 Input 42 |
| | OUT42 | O1 | | GPTA0 Output 42 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 4 | P5.3 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 3 |
| | IN43 | I | | GPTA0 Input 43 |
| | OUT43 | O1 | | GPTA0 Output 43 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 7 | P5.4 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 4 |
| | IN44 | I | | GPTA0 Input 44 |
| | OUT44 | O1 | | GPTA0 Output 44 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|---|
| 8 | P5.5 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 5 |
| | IN45 | I | | GPTA0 Input 45 |
| | OUT45 | O1 | | GPTA0 Output 45 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 9 | P5.6 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 6 |
| | IN46 | I | | GPTA0 Input 46 |
| | OUT46 | O1 | | GPTA0 Output 46 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 10 | P5.7 | I/O0 | A1/ PU | Port 5 General Purpose I/O Line 7 |
| | IN47 | I | | GPTA0 Input 47 |
| | OUT47 | O1 | | GPTA0 Output 47 |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 15 | P5.8 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 8 |
| | RDATA0B | I | | MLI0 Receiver Data Input B |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 16 | P5.9 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 9 |
| | RVALID0B | I | | MLI0 Receiver Data Valid Input B |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 17 | P5.10 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 10 |
| | RREADY0B | O1 | | MLI0 Receiver Ready Input B |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|---|
| 18 | P5.11 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 11 |
| | RCLK0B | I | | MLI0 Receiver Clock Input B |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 19 | P5.12 | I/O0 | A2 | Port 5 General Purpose I/O Line 12 |
| | TDATA0 | O1 | | MLI0 Transmitter Data Output |
| | SLSO07 | O2 | | SSC0 Slave Select Output 7 |
| | Reserved | O3 | | – |
| 20 | P5.13 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 13 |
| | TVALID0B | O1 | | MLI0 Transmitter Valid Input B |
| | SLSO16 | O2 | | SSC1 Slave Select Output 6 |
| | Reserved | O3 | | – |
| 21 | P5.14 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 14 |
| | TREADY0B | I | | MLI0 Transmitter Ready Input B |
| | Reserved | O1 | | – |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |
| 11 | P5.15 | I/O0 | A2/ PU | Port 5 General Purpose I/O Line 15 |
| | TCLK0 | O1 | | MLI0 Transmitter Clock Output |
| | Reserved | O2 | | – |
| | Reserved | O3 | | – |

Port 9

| | | | | |
|---|----------|------|-----------|--|
| 5 | P9.0 | I/O0 | A1/ PU | Port 9 General Purpose I/O Line 0 |
| | Reserved | O1 | | – |
| | OUT80 | O2 | | GPTA0 Output 80 |
| | Reserved | O3 | | – |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|----------|-------|-----------|--|
| 6 | P9.1 | I/O0 | A2/ PU | Port 9 General Purpose I/O Line 1 |
| | Reserved | O1 | | – |
| | OUT81 | O2 | | GPTA0 Output 81 |
| | Reserved | O3 | | – |

Analog Input Port

| | | | | |
|----|------------------|---|---|---|
| 57 | AN0 | I | D | Analog Input 0 |
| 56 | AN1 | I | D | Analog Input 1 |
| 55 | AN2 | I | D | Analog Input 2 |
| 54 | AN3 | I | D | Analog Input 3 |
| 53 | AN4 | I | D | Analog Input 4 |
| 52 | AN5 | I | D | Analog Input 5 |
| 51 | AN6 | I | D | Analog Input 6 |
| 34 | AN7 | I | D | Analog Input 7 |
| 50 | AN8 | I | D | Analog Input 8 |
| 49 | AN9 | I | D | Analog Input 9 |
| 48 | AN10 | I | D | Analog Input 10 |
| 47 | AN11 | I | D | Analog Input 11 |
| 46 | AN12 | I | D | Analog Input 12 |
| 45 | AN13 | I | D | Analog Input 13 |
| 40 | AN14 | I | D | Analog Input 14 |
| 39 | AN15 | I | D | Analog Input 15 |
| 38 | AN16 | I | D | Analog Input 16 |
| 37 | AN19 | I | D | Analog Input 19 |
| 36 | AN23 | I | D | Analog Input 23 |
| 35 | AN25 | I | D | Analog Input 25 |
| 33 | AN28 | I | D | Analog Input 28 |
| 32 | AN29 | I | D | Analog Input 29 |
| 31 | AN30 | I | D | Analog Input 30 |
| 30 | AN31 | I | D | Analog Input 31 |
| 44 | V _{DDM} | – | – | ADC Analog Part Power Supply (3.3V - 5V) |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|-------------|-------|------|--|
| 43 | V_{SSM} | — | — | ADC Analog Part Ground |
| 42 | V_{AREF0} | — | — | ADC Reference Voltage |
| 41 | V_{AGND0} | — | — | ADC Reference Ground |
| 26 | V_{DDMF} | — | — | FADC Analog Part Power Supply (3.3V) ²⁾ |
| 25 | V_{DDAF} | — | — | FADC Analog Part Logic Power Supply (1.5V) |
| 27 | V_{SSMF} | — | — | FADC Analog Part Ground |
| | V_{SSAF} | — | — | FADC Analog Part Ground |
| 28 | V_{FAREF} | — | — | FADC Reference Voltage |
| 29 | V_{FAGND} | — | — | FADC Reference Ground |
| 12, 23, ³⁾ 58, 71, 78, 99, 125, 138 | V_{DD} | — | — | Digital Core Power Supply (1.5V) |
| 13, 22, 59, 70, 79, 100, 115, 126, 139 | V_{DDP} | — | — | Port Power Supply (3.3V) |
| 14, 24, 60, 69, 80, 101, 116, 127, 140 | V_{SS} | - | — | Digital Ground |
| 84 | V_{DDOSC} | — | — | Main Oscillator and PLL Power Supply (1.5V) |

Pinning

Table 3-1 Pin Definitions and Functions (PG-LQFP-144-10 Package)¹⁾ (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|-----|---|-------|-----------|---|
| 85 | V_{DDOSC3} | – | – | Main Oscillator Power Supply (3.3V) |
| 83 | V_{SSOSC} | – | – | Main Oscillator and PLL Ground |
| 117 | V_{DDFL3} | – | – | Power Supply for Flash (3.3V) |
| 81 | XTAL1 | I | – | Main Oscillator Input |
| 82 | XTAL2 | O | – | Main Oscillator Output |
| 87 | $\overline{\text{TDI/BRKIN/BRKOUT}}$ | I/O | A2/ PU | JTAG Serial Data Input / OCDS Break Input / OCDS Break Output (controlled by OCDS module) |
| 88 | TMS/DAP1 | I/O | A2/ PD | JTAG State Machine Control Input / Device Access Port Line 1 |
| 89 | $\overline{\text{TDO/DAP2/BRKIN/BRKOUT}}$ | I/O | A2/ PU | JTAG Serial Data Output / Device Access Port Line 2 / OCDS Break Input / OCDS Break Output (controlled by OCDS module) |
| 90 | $\overline{\text{TRST}}$ | I | A1/ PD | JTAG Reset Input |
| 91 | TCK/DAP0 | I | A1/ PD | JTAG Clock Input / Device Access Port Line 0 |
| 94 | $\overline{\text{TESTMODE}}$ | I | PU | Test Mode Select Input |
| 96 | $\overline{\text{ESR1}}$ | I/O | A2/ PD | External System Request Reset Input 1 |
| 97 | $\overline{\text{PORST}}$ | I | PD | Power On Reset Input (input pad with input spike-filter) |
| 98 | $\overline{\text{ESR0}}$ | I/O | A2/ PD | External System Request Reset Input 0 |

1) TC1736ED : PG-LQFP-144-10

2) This pin is also connected to the analog power supply for comparator of the ADC module.

3) For the emulation device (ED), this pin is bonded to VDD_{SB} (ED Stand By RAM supply). In the non ED device, this pin is bonded to a VDD pad.

Legend for Table 3-1

Column “Ctrl.”:

I = Input (for GPIO port lines with IOCR bit field selection $PCx = 0XXX_B$)

O = Output

O0 = Output with IOCR bit field selection PCx = 1X00_B

O1 = Output with IOCR bit field selection PCx = 1X01_B (ALT1)

O2 = Output with IOCR bit field selection PCx = 1X10_B (ALT2)

O3 = Output with IOCR bit field selection PCx = 1X11 (ALT3)

Column "Type":

A1 = Pad class A1 (LVTTL)

A2 = Pad class A2 (LVTTL)

D = Pad class D (ADC)

PU = with pull-up device connected during reset ($\overline{\text{PORST}} = 0$)

PD = with pull-down device connected during reset ($\overline{\text{PORST}} = 0$)

TR = tri-state during reset ($\overline{\text{PORST}} = 0$)

3.2.1 Reset Behavior of the Pins

Table 3-2 describes the pull-up/pull-down behavior of the System I/O pins during power-on reset.

Table 3-2 List of Pull-up/Pull-down $\overline{\text{PORST}}$ Reset Behavior of the Pins

| Pins | $\overline{\text{PORST}} = 0$ | $\overline{\text{PORST}} = 1$ |
|--------------------------|---|-------------------------------|
| All GPIOs, TDI, TESTMODE | Pull-up | |
| PORST, TRST, TCK, TMS | Pull-down | |
| ESR0 | The open-drain driver is used to drive low. ¹⁾ | Pull-up ²⁾ |
| ESR1 | Pull-down ³⁾ | |
| TDO | Pull-up | High-impedance |

1) Valid additionally after deactivation of $\overline{\text{PORST}}$ until the internal reset phase has finished. See the SCU chapter for details.

2) See the SCU_IOCR register description.

3) see the SCU_IOCR register description.

4 Identification Registers

The Identification Registers uniquely identify a module or the whole device.

Table 4-1 TC1736 Identification Registers

| Short Name | Value | Address | Stepping |
|------------|------------------------|------------------------|----------|
| ADC0_ID | 0058 C000 _H | F010 1008 _H | — |
| ADC1_ID | 0058 C000 _H | F010 1408 _H | — |
| ASC0_ID | 0000 4402 _H | F000 0A08 _H | — |
| ASC1_ID | 0000 4402 _H | F000 0B08 _H | — |
| CAN_ID | 002B C061 _H | F000 4008 _H | — |
| CBS_JDPID | 0000 6350 _H | F000 0408 _H | — |
| CBS_JTAGID | 1015 B083 _H | F000 0464 _H | — |
| CPS_ID | 0015 C007 _H | F7E0 FF08 _H | — |
| CPU_ID | 000A C006 _H | F7E1 FE18 _H | — |
| DMA_ID | 001A C004 _H | F000 3C08 _H | — |
| DMI_ID | 0008 C005 _H | F87F FC08 _H | — |
| FADC_ID | 0027 C003 _H | F010 0408 _H | — |
| FLASH0_ID | 0056 C001 _H | F800 2008 _H | — |
| FPU_ID | 0054 C003 _H | F7E1 A020 _H | — |
| GPTA0_ID | 0029 C005 _H | F000 1808 _H | — |
| LBCU_ID | 000F C005 _H | F87F FE08 _H | — |
| LFI_ID | 000C C006 _H | F87F FF08 _H | — |
| MCHK_ID | 001B C001 _H | F010 C208 _H | — |
| MLI0_ID | 0025 C007 _H | F010 C008 _H | — |
| MSC0_ID | 0028 C003 _H | F000 0808 _H | — |
| PMI_ID | 000B C005 _H | F87F FD08 _H | — |
| PMU0_ID | 0050 C001 _H | F800 0508 _H | — |
| SBCU_ID | 0000 6A0C _H | F000 0108 _H | — |
| SCU_CHIPID | 0000 9201 _H | F000 0640 _H | — |
| SCU_ID | 0052 C001 _H | F000 0508 _H | — |
| SCU_MANID | 0000 1820 _H | F000 0644 _H | — |
| SCU_RTID | 0000 0000 _H | F000 0648 _H | AA-step |

Identification Registers
Table 4-1 TC1736 Identification Registers (cont'd)

| Short Name | Value | Address | Stepping |
|------------|------------------------|------------------------|----------|
| SSC0_ID | 0000 4511 _H | F010 0108 _H | – |
| SSC1_ID | 0000 4511 _H | F010 0208 _H | – |
| STM_ID | 0000 C006 _H | F000 0208 _H | – |

5 Electrical Parameters

5.1 General Parameters

5.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1736 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column "Symbol":

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1736 and must be regarded for a system design.
- **SR**
Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1736 designed in.

Electrical Parameters

5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the [Section 18.2.1](#).

Table 2 Pad Driver and Pad Classes Overview

| Class | Power Supply | Type | Sub Class | Speed Grade | Load | Leakage ¹⁾ | Termination |
|----------------------|--------------|--------------------------|---------------------------------|-------------|--------|-----------------------|--------------------------------|
| A | 3.3 V | LVTTL I/O, LVTTL outputs | A1 (e.g. GPIO) | 6 MHz | 100 pF | 500 nA | No |
| | | | A2 (e.g. serial I/Os) | 40 MHz | 50 pF | 6 μ A | Series termination recommended |
| D_E | 5 V | ADC | — | — | — | — | see Table 18-7 |

1) Values are for $T_{Jmax} = 150\text{ }^{\circ}\text{C}$.

Electrical Parameters

5.1.3 Absolute Maximum Ratings

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

During absolute maximum rating overload conditions ($V_{IN} > \text{related } V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on the related V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 3 Absolute Maximum Rating Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------------------------|--------|------|--------------------------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Ambient temperature | T_A SR | -40 | – | 125 | °C | Under bias |
| Storage temperature | T_{ST} SR | -65 | – | 150 | °C | – |
| Junction temperature | T_J SR | -40 | – | 150 | °C | Under bias |
| Voltage at 1.5 V power supply pins with respect to V_{SS} ¹⁾ | V_{DD} SR | – | – | 2.25 | V | – |
| Voltage at 3.3 V power supply pins with respect to V_{SS} ²⁾ | V_{DDP} SR | – | – | 3.75 | V | – |
| Voltage at 5 V power supply pins with respect to V_{SS} | V_{DDM} SR | – | – | 5.5 | V | – |
| Voltage on any Class A input pin and dedicated input pins with respect to V_{SS} | V_{IN} SR | -0.5 | – | $V_{DDP} + 0.5$ or max. 3.7 | V | Whatever is lower |
| Voltage on any Class D analog input pin with respect to V_{AGND} | V_{AIN} V_{AREFx} SR | -0.5 | – | $V_{DDM} + 0.5$ | V | – |
| Voltage on any Class D analog input pin with respect to V_{SSAF} , if the FADC is switched through to the pin. | V_{AINF} V_{FAREF} SR | -0.5 | – | $V_{DDM} + 0.5$ | V | – |

1) Applicable for V_{DD} , V_{DDOSC} , V_{DDPLL} , and V_{DDAF} .

2) Applicable for V_{DDP} , V_{DDFL3} , and V_{DDMF} .

Electrical Parameters

5.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the TC1736. All parameters specified in the following table refer to these operating conditions, unless otherwise noted.

Table 4 Operating Condition Parameters

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|--|------------------|----|--------|------|--------------------|------|--|
| | | | Min. | Typ. | Max. | | |
| Digital supply voltage ¹⁾ | V_{DD} | SR | 1.42 | – | 1.58 ²⁾ | V | – |
| | V_{DDOSC} | SR | | | | | |
| | V_{DDP} | SR | 3.13 | – | 3.47 ³⁾ | V | For Class A pins (3.3 V \pm 5%) |
| | V_{DDOSC3} | SR | | | | | |
| Analog supply voltages | V_{DDFL3} | SR | 3.13 | – | 3.47 ³⁾ | V | – |
| | V_{DDMF} | SR | 3.13 | – | 3.47 ³⁾ | V | FADC |
| | V_{DDAF} | SR | 1.42 | – | 1.58 ²⁾ | V | FADC |
| | V_{DDM} | SR | 4.75 | – | 5.25 | V | For Class D _E pins, ADC |
| Digital ground voltage | V_{SS} | SR | 0 | – | – | V | – |
| Ambient temperature under bias | T_A | SR | – | -40 | +125 | °C | – |
| Analog supply voltages | – | | – | – | – | – | See separate specification Page 18-12 , Page 18-17 |
| Overload current at class D pins | I_{OV} | | -1 | – | 3 | mA | ⁴⁾ |
| Sum of overload current at class D pins | $\Sigma I_{OV} $ | | – | – | 10 | mA | per single ADC |
| Overload coupling factor for analog inputs ⁵⁾ | K_{OVAP} | | – | – | 5×10^{-5} | | $0 < I_{OV} < 3$ mA |
| | K_{OVAN} | | – | – | 5×10^{-4} | | -1 mA $< I_{OV} < 0$ |
| CPU & LMB Bus Frequency | f_{CPU} | SR | – | – | 80 40 | MHz | Derivative dependent |
| FPI Bus Frequency | f_{SYS} | SR | – | – | 80 | MHz | ⁶⁾ |
| Short circuit current | I_{SC} | SR | -5 | – | +5 | mA | ⁶⁾ |

Electrical Parameters

Table 4 Operating Condition Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|--------------------------|--------|------|------|------|--|
| | | Min. | Typ. | Max. | | |
| Absolute sum of short circuit currents of a pin group (see Table 5) | $\Sigma I_{SC_PG} $ SR | – | – | 20 | mA | See note |
| Inactive device pin current | I_{ID} SR | -1 | – | 1 | mA | All power supply voltages $V_{DDx} = 0$ |
| Absolute sum of short circuit currents of the device | $\Sigma I_{SC_D} $ SR | – | – | 100 | mA | See note ⁴⁾ |
| External load capacitance | C_L SR | – | – | – | pF | Depending on pin class. See DC characteristics |

- 1) Digital supply voltages applied to the TC1736 must be static regulated voltages which allow a typical voltage swing of $\pm 5\%$.
- 2) Voltage overshoot up to 1.7 V is permissible at Power-Up and \overline{PORST} low, provided the pulse duration is less than 100 μs and the cumulated summary of the pulses does not exceed 1 h.
- 3) Voltage overshoot up to 4 V is permissible at Power-Up and \overline{PORST} low, provided the pulse duration is less than 100 μs and the cumulated summary of the pulses does not exceed 1 h.
- 4) See additional document "TC1767 Pin Reliability in Overload" for definition of overload current on digital pins.
- 5) The overload coupling factor (kA) defines the worst case relation of an overload condition (IOV) at one pin to the resulting leakage current (IleakTOT) into an adjacent pin: $IleakTOT = \pm kA \times |IOV| + IOZ1$.
Thus under overload conditions an additional error leakage voltage (VAEL) will be induced onto an adjacent analog input pin due to the resistance of the analog input source (RAIN). That means $VAEL = RAIN \times |IleakTOT|$.
The definition of adjacent pins is related to their order on the silicon.
The Injected leakage current always flows in the opposite direction from the causing overload current. Therefore, the total leakage current must be calculated as an algebraic sum of the both component leakage currents (the own leakage current IOZ1 and the optional injected leakage current).
- 6) Applicable for digital outputs.

Electrical Parameters

Table 5 Pin Groups for Overload/Short-Circuit Current Sum Parameter

| Group | Pins |
|-------|--|
| 1 | P5.[14:8] |
| 2 | P2.[7:0] |
| 3 | P4.[3:2]; P1.[11:8] |
| 4 | P1.4; $\overline{\text{TDI/BRKIN/BRKOUT}}$; TMS/DAP1; TDO/DAP2/ $\overline{\text{BRKIN/BRKOUT}}$; $\overline{\text{TRST}}$, TCK/DAP0; P1.[1:0]; P1.15; $\overline{\text{TESTMODE}}$; $\overline{\text{ESR0}}$; $\overline{\text{PORST}}$; $\overline{\text{ESR1}}$ |
| 5 | P3.[10:0]; P3.[15:14] |
| 6 | P3.[13:11]; P0.[3:0] |
| 7 | P2.[13:8]; P0.[5:4]; P0.[13:12] |
| 8 | P0.[7:6]; P0.[15:14]; P5.[7:0]; P5.15; P9.[1:0] |

Electrical Parameters

5.2 DC Parameters

5.2.1 Input/Output Pins

Table 6 Input/Output DC-Characteristics (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-----------------|-----------------------|------|--------------------------------|------|---|
| | | Min. | Typ. | Max. | | |
| General Parameters | | | | | | |
| Pull-up current ¹⁾ | I_{PUH} CC | 10 | – | 100 | μA | $V_{IN} < V_{IHmin}$; class A1/A2/Input pads. |
| Pull-down current ¹⁾ | I_{PDL} CC | 10 | – | 150 | μA | $V_{IN} > V_{ILmax}$; class A1/A2/Input pads. |
| Pin capacitance ¹⁾ (Digital I/O) | C_{IO} CC | – | – | 10 | pF | $f = 1\text{ MHz}$ $T_A = 25\text{ °C}$ |
| Input only Pads ($V_{DDP} = 3.13\text{ to }3.47\text{ V} = 3.3\text{ V} \pm 5\%$) | | | | | | |
| Input low voltage | V_{ILI} SR | -0.3 | – | $0.36 \times V_{DDP}$ | V | – |
| Input high voltage | V_{IHI} SR | $0.62 \times V_{DDP}$ | – | $V_{DDP} + 0.3$ or max. 3.6 | V | Whatever is lower |
| Ratio V_{IL}/V_{IH} | CC | 0.58 | – | – | – | – |
| Input high voltage TRST, TCK | V_{IHJ} SR | $0.64 \times V_{DDP}$ | – | $V_{DDP} + 0.3$ or max. 3.6 | V | Whatever is lower |
| Input hysteresis | HYSI CC | $0.1 \times V_{DDP}$ | – | – | V | ⁴⁾ |
| Input leakage current ²⁾ | I_{OZI} CC | – | – | ±3000 ±6000 | nA | $((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ Otherwise |
| Spike filter always blocked pulse duration | t_{SF1} CC | – | – | 10 | ns | |

Electrical Parameters

Table 6 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------|-----------------------|------|-----------------------------|------|---|
| | | Min. | Typ. | Max. | | |
| Spike filter pass-through pulse duration | t_{SF2} CC | 100 | — | — | ns | |
| Class A Pads ($V_{DDP} = 3.13$ to 3.47 V = 3.3 V \pm 5%) | | | | | | |
| Output low voltage ²⁾³⁾ | V_{OLA} CC | — | — | 0.4 | V | $I_{OL} = 2$ mA for medium and strong driver mode, $I_{OL} = 500$ μ A for weak driver mode |
| Output high voltage ^{2) 3)} | V_{OHA} CC | 2.4 | — | — | V | $I_{OH} = -2$ mA for medium and strong driver mode, $I_{OH} = -500$ μ A for weak driver mode |
| | | $V_{DDP} - 0.4$ | — | — | V | $I_{OH} = -1.4$ mA for medium and strong driver mode, $I_{OH} = -400$ μ A for weak driver mode |
| Input low voltage Class A1/2 pins | V_{ILA} SR | -0.3 | — | $0.36 \times V_{DDP}$ | V | — |
| Input high voltage Class A1 pins | V_{IHA1} SR | $0.62 \times V_{DDP}$ | — | $V_{DDP} + 0.3$ or max. 3.6 | V | Whatever is lower |
| Ratio V_{IL}/V_{IH} | SR | 0.58 | — | — | — | — |
| Input high voltage Class A2 pins | V_{IHA2} SR | $0.60 \times V_{DDP}$ | — | $V_{DDP} + 0.3$ or max. 3.6 | V | Whatever is lower |
| Ratio V_{IL}/V_{IH} | CC | 0.60 | — | — | — | — |
| Input hysteresis | HYESA CC | $0.1 \times V_{DDP}$ | — | — | V | ⁴⁾ |
| Input leakage current Class A2 pins | I_{OZA2} | — | — | ± 3000 ± 6000 | nA | $((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1)$ Otherwise ²⁾ |

Electrical Parameters

Table 6 **Input/Output DC-Characteristics** (cont'd)(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|------------------|--------|------|------|------|---------------------------------|
| | | Min. | Typ. | Max. | | |
| Input leakage current Class A1 pins | I_{OZA1} CC | — | — | ±500 | nA | $0\text{ V} < V_{IN} < V_{DDP}$ |

Class D Pads

| | | | | | |
|-------------------------|---|---|---|---|---|
| See ADC Characteristics | — | — | — | — | — |
|-------------------------|---|---|---|---|---|

- 1) Not subject to production test, verified by design / characterization.
- 2) Only one of these parameters is tested, the other is verified by design characterization
- 3) Maximum resistance of the driver $R_{DS(on)}$, defined for P_MOS / N_MOS transistor separately:
25 / 20 Ω for strong driver mode, $I_{OH/L} < 2\text{ mA}$,
200 / 150 Ω for medium driver mode, $I_{OH/L} < 400\text{ uA}$,
600 / 400 Ω for weak driver mode, $I_{OH/L} < 100\text{ uA}$,
verified by design / characterization.
- 4) Function verified by design, value verified by design characterization.
Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce.
It cannot be guaranteed that it suppresses switching due to external system noise.

Electrical Parameters

5.2.2 Analog to Digital Converters (ADC0/ADC1)

All ADC parameters are optimized for and valid in the range of $V_{DDM} = 5V \pm 5\%$.

Table 7 ADC Characteristics (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---------------------------|----|---------------------|-----------|----------------------------|------------|--|
| | | | Min. | Typ. | Max. | | |
| Analog supply voltage | V_{DDM} | SR | 4.75 | 5 | 5.25 | V | – |
| | | | 3.13 | 3.3 | 3.47 ¹⁾ | V | – |
| | V_{DD} | SR | 1.42 | 1.5 | 1.58 ²⁾ | V | Power supply for ADC digital part, internal supply |
| Analog ground voltage | V_{SSM} | SR | -0.1 | – | 0.1 | V | – |
| Analog reference voltage ¹⁴⁾ | V_{AREF_x} | SR | $V_{AGND_x} + 1V$ | V_{DDM} | $V_{DDM} + 0.05$ 1)3)4) | V | – |
| Analog reference ground ¹⁴⁾ | V_{AGND_x} | SR | $V_{SSM_x} - 0.05V$ | 0 | $V_{AREF} - 1V$ | V | – |
| Analog input voltage range | V_{AIN} | SR | V_{AGND_x} | – | V_{AREF_x} | V | – |
| Analog reference voltage range ⁵⁾¹⁴⁾ | $V_{AREF_x} - V_{AGND_x}$ | SR | $V_{DDM}/2$ | – | $V_{DDM} + 0.05$ | V | – |
| Converter Clock | f_{ADC} | SR | 1 | – | 80 | MHz | – |
| Internal ADC clocks | f_{ADCI} | CC | 0.5 | – | 10 | MHz | – |
| Sample time | t_s | CC | 2 | – | 257 | T_{ADCI} | – |
| Total unadjusted error ⁵⁾ | TUE ⁶⁾ | CC | – | – | ± 4 | LSB | 12-bit conversion, without noise ⁷⁾⁸⁾ |
| | | | – | – | ± 2 | LSB | 10-bit conversion ⁸⁾ |
| | | | – | – | ± 1 | LSB | 8-bit conversion ⁸⁾ |
| DNL error ^{9) 5)} | EA_{DNL} | CC | – | ± 1.5 | ± 3.0 | LSB | 12-bit conversion without noise ⁸⁾¹⁰⁾ |
| INL error ⁹⁾⁵⁾ | EA_{INL} | CC | – | ± 1.5 | ± 3.0 | LSB | 12-bit conversion without noise ⁸⁾¹⁰⁾ |
| Gain error ⁹⁾⁵⁾ | EA_{GAIN} | CC | – | ± 0.5 | ± 3.5 | LSB | 12-bit conversion without noise ⁸⁾¹⁰⁾ |

Electrical Parameters

Table 7 ADC Characteristics (cont'd) (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------|--------|------|------|--------|---|
| | | Min. | Typ. | Max. | | |
| Offset error ⁹⁾⁵⁾ | $E_{A_{OFF}}$ CC | – | ±1.0 | ±4.0 | LSB | 12-bit conversion without noise ⁸⁾¹⁰⁾ |
| Input leakage current at analog inputs of ADC0/1 ^{11) 12) 13)} | I_{OZ1} CC | -300 | – | 100 | nA | (0% V_{DDM}) < V_{IN} < (3% V_{DDM}) |
| | | -100 | – | 200 | nA | (3% V_{DDM}) < V_{IN} < (97% V_{DDM}) |
| | | -100 | – | 300 | nA | (97% V_{DDM}) < V_{IN} < (100% V_{DDM}) |
| Input leakage current at $V_{AREF0/1}$, per module | I_{OZ2} CC | – | – | ±1.5 | μA | 0 V < V_{AREF} < V_{DDM} , no conversion running |
| Input current at $V_{AREF0/1}$ ¹⁴⁾ , per module | I_{AREF} CC | – | 35 | 75 | μA rms | 0 V < V_{AREF} < V_{DDM} ¹⁵⁾ |
| Total capacitance of the voltage reference inputs ¹⁶⁾¹⁴⁾ | $C_{AREFTOT}$ CC | – | 20 | 40 | pF | ⁸⁾ |
| Switched capacitance at the positive reference voltage input ¹⁴⁾ | C_{AREFSW} CC | – | 15 | 30 | pF | ⁸⁾¹⁷⁾ |
| Resistance of the reference voltage input path ¹⁶⁾ | R_{AREF} CC | – | 500 | 1000 | Ω | 500 Ohm increased for AN[1:0] used as reference input ⁸⁾ |
| Total capacitance of the analog inputs ¹⁶⁾ | C_{AINTOT} CC | – | 25 | 30 | pF | ⁶⁾⁸⁾ |

Electrical Parameters

Table 7 **ADC Characteristics (cont'd)** (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------|--------|--------|--------------------|----------|--|
| | | Min. | Typ. | Max. | | |
| Switched capacitance at the analog voltage inputs | C_{AINSW} CC | – | 7 | 20 | pF | 8)18) |
| ON resistance of the transmission gates in the analog voltage path | R_{AIN} CC | – | 700 | 1500 | Ω | 8) |
| ON resistance for the ADC test (pull-down for AIN7) | R_{AIN7T} CC | 180 | 550 | 900 ¹⁹⁾ | Ω | Test feature available only for AIN7 ^{8) 20)} |
| Current through resistance for the ADC test (pull-down for AIN7) | I_{AIN7T} CC | – | 15 rms | 30 peak | mA | Test feature available only for AIN7 ⁸⁾ |

- 1) Voltage overshoot up to 4 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 μs and the cumulated summary of the pulses does not exceed 1 h.
- 2) Voltage overshoot up to 1.7 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 μs and the cumulated summary of the pulses does not exceed 1 h.
- 3) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoot).
- 4) If the reference voltage V_{AREF} increases or the V_{DDM} decreases, so that $V_{\text{AREF}} = (V_{\text{DDM}} + 0.05 \text{ V to } V_{\text{DDM}} + 0.07 \text{ V})$, then the accuracy of the ADC decreases by 4 LSB12.
- 5) If a reduced reference voltage in a range of $V_{\text{DDM}}/2$ to V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced with the factor k ($k < 1$), then TUE, DNL, INL Gain and Offset errors increase with the factor $1/k$.
If a reduced reference voltage in a range of 1 V to $V_{\text{DDM}}/2$ is used, then there are additional decrease in the ADC speed and accuracy.
- 6) TUE is tested at $V_{\text{AREF}} = 5.0 \text{ V}$, $V_{\text{AGND}} = 0 \text{ V}$ and $V_{\text{DDM}} = 5.0 \text{ V}$
- 7) ADC module capability.
- 8) Not subject to production test, verified by design / characterization.
- 9) The sum of DNL/INL/Gain/Offset errors does not exceed the related TUE total unadjusted error.
- 10) For 10-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with factor 0.25.
For 8-bit conversions the DNL/INL/Gain/Offset error values must be multiplied with 0.0625.
- 11) The leakage current definition is a continuous function, as shown in [Figure 18-3](#). The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function.

Electrical Parameters

- 12) Only one of these parameters is tested, the other is verified by design characterization.
- 13) The leakage current decreases typically 30% for junction temperature decrease of 10°C.
- 14) Applies to AINx, when used as auxiliary reference inputs.
- 15) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to $t_C = 25\mu s$ can be calculated with the formula $I_{AREF_MAX} = Q_{CONV}/t_C$. Every conversion needs a total charge of $Q_{CONV} = 150pC$ from V_{AREF} .
All ADC conversions with a duration longer than $t_C = 25\mu s$ consume an $I_{AREF_MAX} = 6\mu A$.
- 16) For the definition of the parameters see also [Figure 18-2](#).
- 17) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this smaller capacitances are successively switched to the reference voltage.
- 18) The sampling capacity of the conversion C-Network is pre-charged to $V_{AREF}/2$ before the sampling moment. Because of the parasitic elements the voltage measured at AINx deviates from $V_{AREF}/2$, and is typically 1.35V.
- 19) $R_{AIN7T} = 1400\text{ Ohm}$ maximum and 830 Ohm typical in the $V_{DDM} = 3.3V \pm 5\%$ range.
- 20) The DC current at the pin is limited to 3 mA for the operational lifetime.

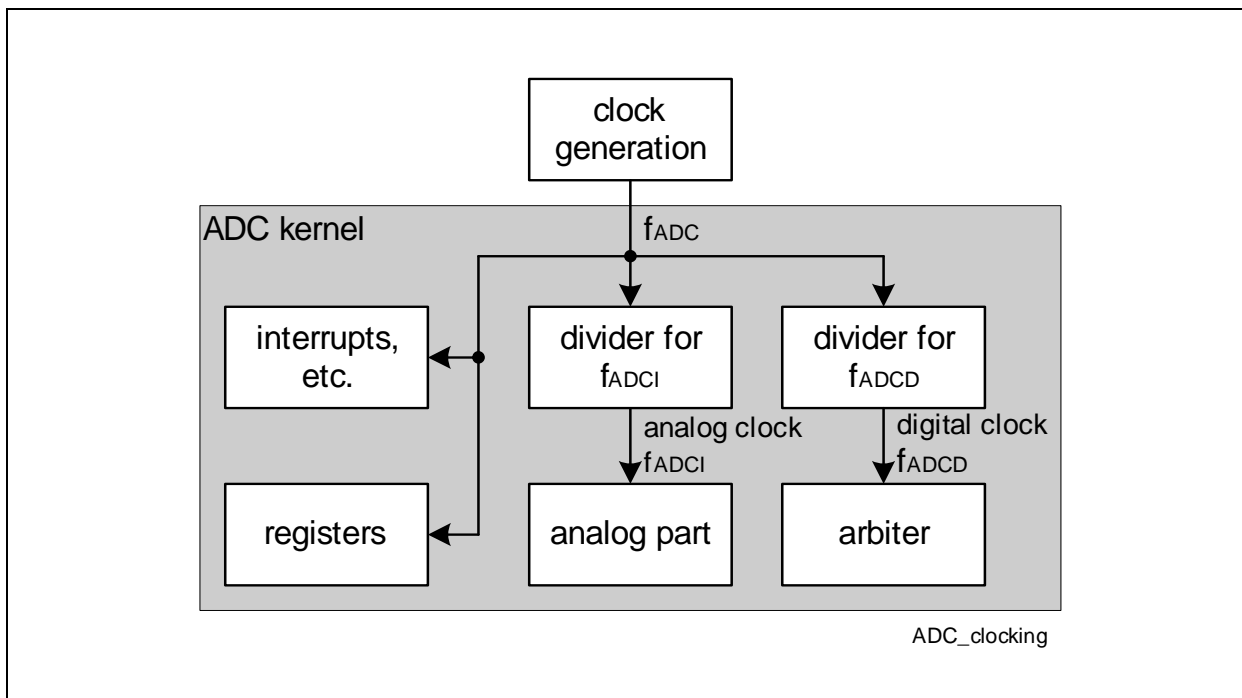
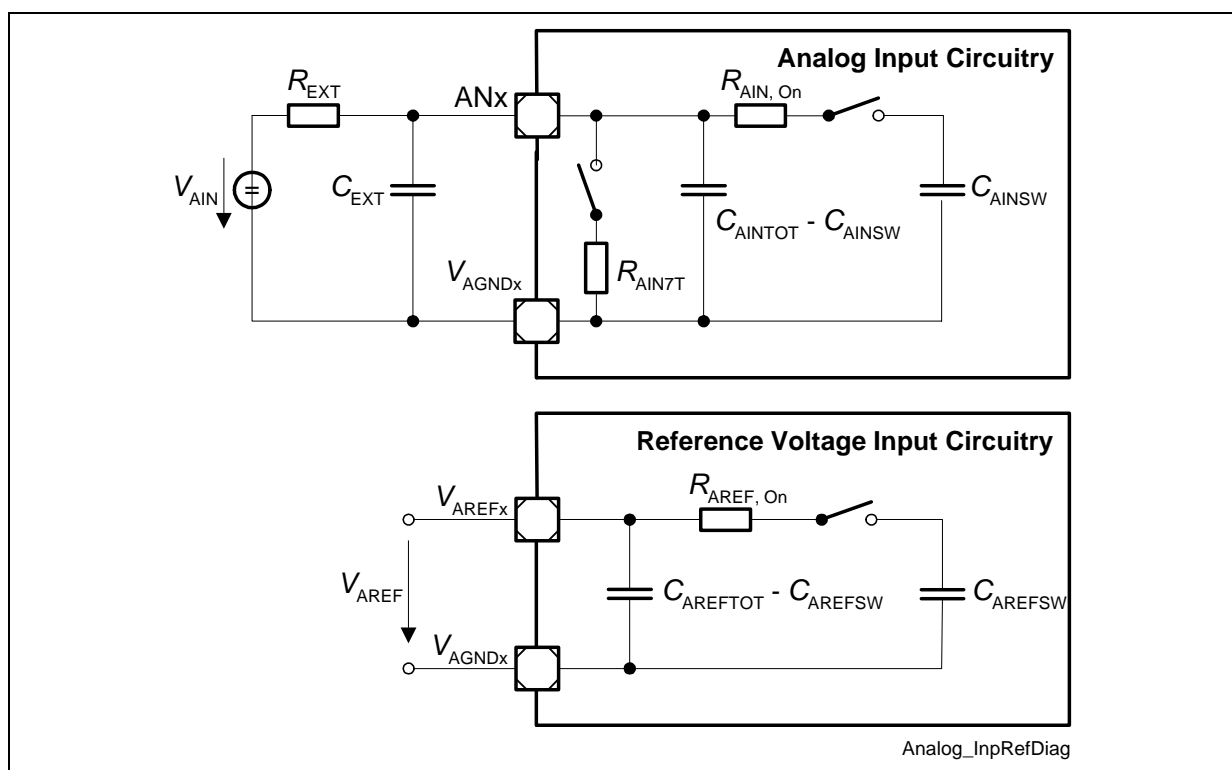
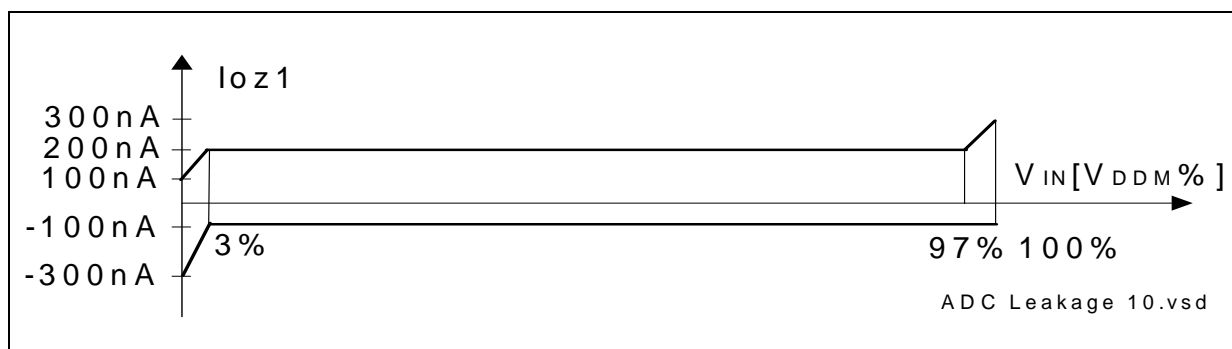


Figure 1 **ADC0/ADC1 Clock Circuit**

Electrical Parameters

Table 8 Conversion Time (Operating Conditions apply)

| Parameter | Symbol | Value | Unit | Note |
|--|----------|--|---------|--|
| Conversion time with post-calibration | t_C CC | $2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$ | μs | $n = 8, 10, 12$ for n - bit conversion $T_{ADC} = 1 / f_{ADC}$ $T_{ADCI} = 1 / f_{ADCI}$ |
| Conversion time without post-calibration | | $2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$ | | |


Figure 2 ADC0/ADC1 Input Circuits

Figure 3 ADC0/ADC1 Analog Inputs Leakage

Electrical Parameters

5.2.3 Fast Analog to Digital Converter (FADC)

All parameters apply to FADC used in differential mode, which is the default and the intended mode of operation, and which takes advantage of many error cancelation effects inherent to differential measurements in general.

Table 9 FADC Characteristics (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------------------------|-----------------------------|------|-----------------------------|-------------------|-----------------------------------|
| | | Min. | Typ. | Max. | | |
| DNL error | EF_{DNL} CC | – | – | ± 1 | LSB | ⁹⁾ |
| INL error | EF_{INL} CC | – | – | ± 4 | LSB | ⁹⁾ |
| Gradient error ⁹⁾ | EF_{GRAD} CC | – | – | ± 5 | % | Without calibration gain 1, 2, 4 |
| | | – | – | ± 6 | % | Without calibration gain 8 |
| Offset error ⁹⁾¹⁾ | EF_{OFF} ²⁾ CC | – | – | ± 20 ³⁾ | mV | With calibration ¹⁾ |
| | | – | – | ± 90 ³⁾ | mV | Without calibration |
| Reference error of internal $V_{FAREF}/2$ | EF_{REF} CC | – | – | ± 60 | mV | – |
| Analog supply voltages | V_{DDMF} SR | 3.13 | – | 3.47 ⁴⁾ | V | – |
| | V_{DDAF} SR | 1.42 | – | 1.58 ⁵⁾ | V | – |
| Analog ground voltage | V_{SSAF} SR | -0.1 | – | 0.1 | V | – |
| Analog reference voltage | V_{FAREF} SR | 3.13 | – | 3.47 ⁴⁾⁶⁾ | V | Nominal 3.3 V |
| Analog reference ground | V_{FAGND} SR | $V_{SSAF} - 0.05 \text{ V}$ | – | $V_{SSAF} + 0.05 \text{ V}$ | V | – |
| Analog input voltage range | V_{AINF} SR | V_{FAGND} | – | V_{DDMF} | V | – |
| Analog supply currents | I_{DDMF} SR | – | – | 10 | mA | – |
| | I_{DDAF} SR | – | – | 10 | mA | ⁷⁾ |
| Input current at V_{FAREF} | I_{FAREF} CC | – | – | 120 | $\mu\text{A rms}$ | Independent of conversion |
| Input leakage current at V_{FAREF} ⁸⁾ | I_{FOZ2} CC | – | – | ± 500 | nA | $0 \text{ V} < V_{IN} < V_{DDMF}$ |
| Input leakage current at V_{FAGND} ⁸⁾ | I_{FOZ3} CC | – | – | ± 8 | μA | $0 \text{ V} < V_{IN} < V_{DDMF}$ |

Electrical Parameters

Table 9 FADC Characteristics (Operating Conditions apply) (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|------------------|--------|------|------|-------------------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Conversion time | t_{C_FADC} CC | – | – | 21 | CLK of f_{FADC} | For 10-bit conv. |
| Converter clock | f_{FADC} SR | 10 | – | 80 | MHz | – |
| Input resistance of the analog voltage path (Rn, Rp) | R_{FAIN} CC | 100 | – | 200 | k Ω | ⁹⁾ |
| Channel amplifier cutoff frequency ⁹⁾ | f_{COFF} CC | 2 | – | – | MHz | – |
| Settling time of a channel amplifier (after changing channel amplifier input) ⁹⁾ | t_{SET} CC | – | – | 5 | μ s | – |

- 1) Calibration should be performed at each power-up. In case of continuous operation, calibration should be performed minimum once per week, or on regular basis in order to compensate for temperature changes.
- 2) The offset error voltage drifts over the whole temperature range maximum ± 6 LSB.
- 3) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be multiplied with the applied gain.
- 4) Voltage overshoots up to 4 V are permissible, provided the pulse duration is less than 100 μ s and the cumulated summary of the pulses does not exceed 1 h.
- 5) Voltage overshoots up to 1.7 V are permissible, provided the pulse duration is less than 100 μ s and the cumulated sum of the pulses does not exceed 1 h.
- 6) A running conversion may become inexact in case of violating the normal operating conditions (voltage overshoots).
- 7) Current peaks of up to 40 mA with a duration of max. 2 ns may occur
- 8) This value applies in power-down mode.
- 9) Not subject to production test, verified by design / characterization.

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

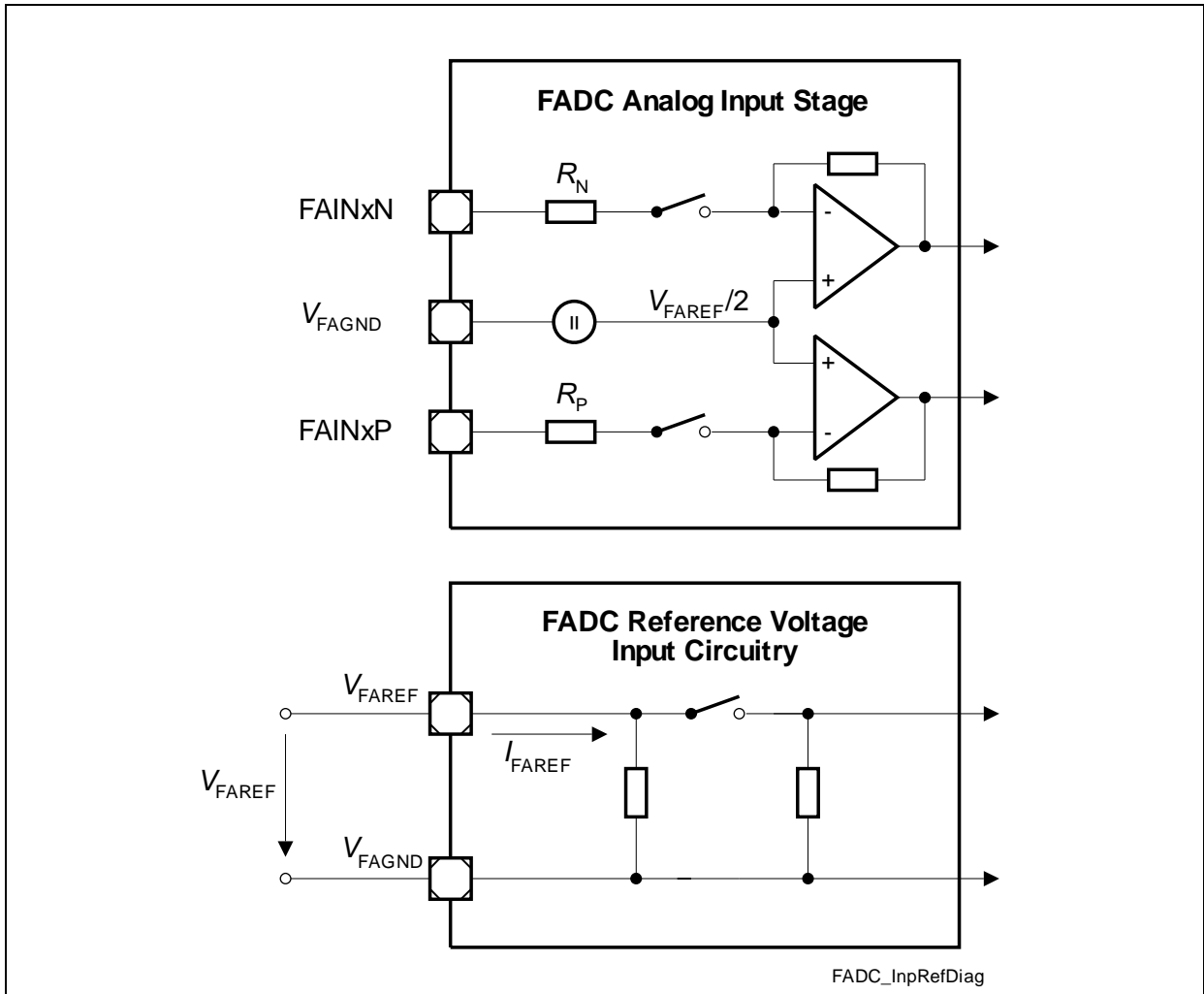


Figure 4 FADC Input Circuits

Electrical Parameters

5.2.4 Oscillator Pins

Table 10 Oscillator Pins Characteristics (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|-----------|----|-------------------------|------|-------------------------|---------|--------------------------------|
| | | | Min. | Typ. | Max. | | |
| Frequency range | f_{OSC} | CC | 8 | – | 25 | MHz | External Crystal Mode selected |
| Input low voltage at XTAL1 ¹⁾ | V_{ILX} | SR | -0.2 | – | $0.3 \times V_{DDOSC3}$ | V | – |
| Input high voltage at XTAL1 ¹⁾ | V_{IHx} | SR | $0.7 \times V_{DDOSC3}$ | – | $V_{DDOSC3} + 0.2$ | V | – |
| Input current at XTAL1 | I_{IX1} | CC | – | – | ± 25 | μA | $0 V < V_{IN} < V_{DDOSC3}$ |

1) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of $0.3 \times V_{DDOSC3}$ is sufficient.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Refer to the limits specified by the crystal supplier.

5.2.5 Temperature Sensor

Table 11 Temperature Sensor Characteristics (Operating Conditions apply)

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|-------------------------------------|------------|----|--------|------|---------|---------|-----------------------|
| | | | Min. | Typ. | Max. | | |
| Temperature sensor range | T_{SR} | SR | -40 | | 150 | °C | Junction temperature |
| Temperature sensor measurement time | t_{TSMT} | SR | – | – | 100 | μs | – |
| Start-up time after reset | t_{TSST} | SR | – | – | 10 | μs | – |
| Sensor accuracy | T_{TSA} | CC | – | – | ± 6 | °C | Calibrated |

Electrical Parameters

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bitfield of the DTSSTAT register.

(1)

$$T_j = \frac{DTSSTAT_{RESULT} - 619}{2, 28}$$

Electrical Parameters

5.2.6 Power Supply Current

The default test conditions (differences explicitly specified) are:

$V_{DD} = 1.58 \text{ V}$, $V_{DDP} = 3.47 \text{ V}$, $T_J = 150^\circ\text{C}$. All other operating conditions apply.

Table 12 Power Supply Currents, Maximum Power Consumption

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---------------|----|--------|------|------|------|--|
| | | | Min. | Typ. | Max. | | |
| Core active mode supply current ^{1) 2)} | I_{DD} | CC | – | – | 250 | mA | $f_{CPU}=80 \text{ MHz}$ $f_{CPU}/f_{SYS} = 1:1$ |
| Realistic core active mode supply current ³⁾⁴⁾ | | | – | – | 150 | mA | $V_{DD} = 1.53 \text{ V}$, $T_J = 150^\circ\text{C}$ |
| FADC 3.3 V analog supply current | I_{DDMF} | CC | – | – | 10 | mA | – |
| FADC 1.5 V analog supply current | I_{DDAF} | CC | – | – | 10 | mA | – ⁴⁾ |
| Flash memory 3.3 V supply current | I_{DDFL3R} | CC | – | – | 60 | mA | continuously reading the Flash memory ⁵⁾ |
| | I_{DDFL3E} | CC | – | – | 61 | mA | Flash memory erase-verify ⁶⁾ |
| Oscillator 1.5 V supply | I_{DDOSC} | CC | – | – | 3 | mA | – ⁴⁾ |
| Oscillator 3.3 V supply | I_{DDOSC3} | CC | – | – | 10 | mA | – ⁴⁾ |
| Pad currents, sum of V_{DDP} 3.3 V supplies | I_{DDP} | CC | – | – | 14 | mA | – ^{4) 7)} |
| | I_{DDP_FP} | CC | – | – | 34 | mA | I_{DDP} including Data Flash programming current ^{4) 8)} |
| ADC 5 V power supply | I_{DDM} | CC | – | 2 | 3 | mA | ADC0 / 1 |
| Maximum Average Power Dissipation ¹⁾ | P_D | SR | – | | 800 | mW | worst case $T_A = 125^\circ\text{C}$, $P_D \times R_{\theta JA} < 25^\circ\text{C}$ |

1) Infineon Power Loop: CPU running, all peripherals active. The power consumption of each custom application will most probably be lower than this value, but must be evaluated separately.

2) The I_{DD} maximum value is 190 mA at $f_{CPU} = 40 \text{ MHz}$, constant $T_J = 150^\circ\text{C}$, for the Infineon Max Power Loop. The dependency in this range is, at constant junction temperature, linear.

$f_{CPU}/f_{SYS} = 1:1$ mode.

3) The I_{DD} maximum value is 110 mA at $f_{CPU} = 40 \text{ MHz}$, constant $T_J = 150^\circ\text{C}$, for the Realistic Pattern. The dependency in this range is, at constant junction temperature, linear.

$f_{CPU}/f_{SYS} = 1:1$ mode.

Electrical Parameters

- 4) Not tested in production separately, verified by design / characterization.
- 5) This value assumes worst case of reading flash line with all cells erased. In case of 50% cells written with "1" and 50% cells written with "0", the maximum current drops down to 53 mA.
- 6) Relevant for the power supply dimensioning, not for thermal considerations.
In case of erase of Data Flash, internal flash array loading effects may generate transient current spikes of up to 15 mA for maximum 5 ms.
- 7) No GPIO activity
- 8) This value is relevant for the power supply dimensioning not for thermal considerations.
The currents caused by the GPIO activity depend on the particular application and should be added separately.

5.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled. That means, keeping the pads constantly at maximum strength.

5.3.1 Testing Waveforms

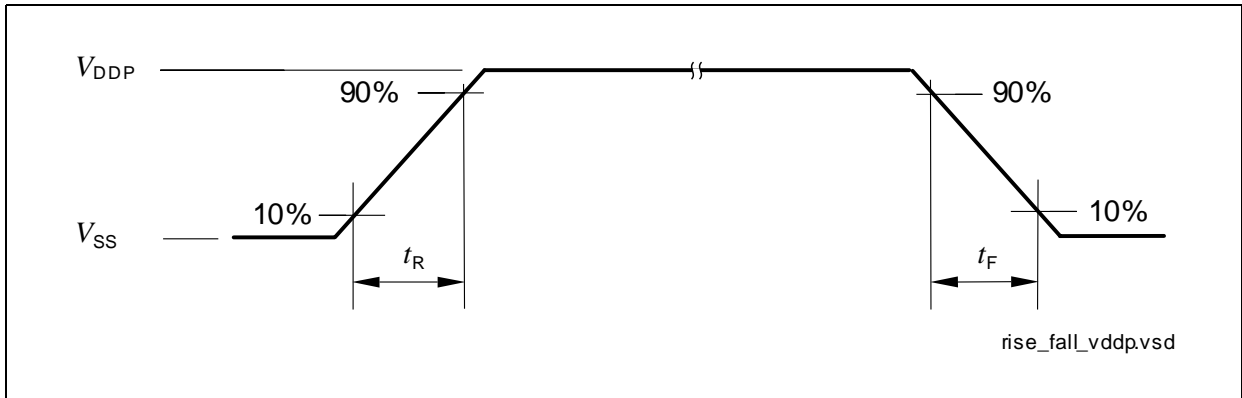


Figure 5 Rise/Fall Time Parameters

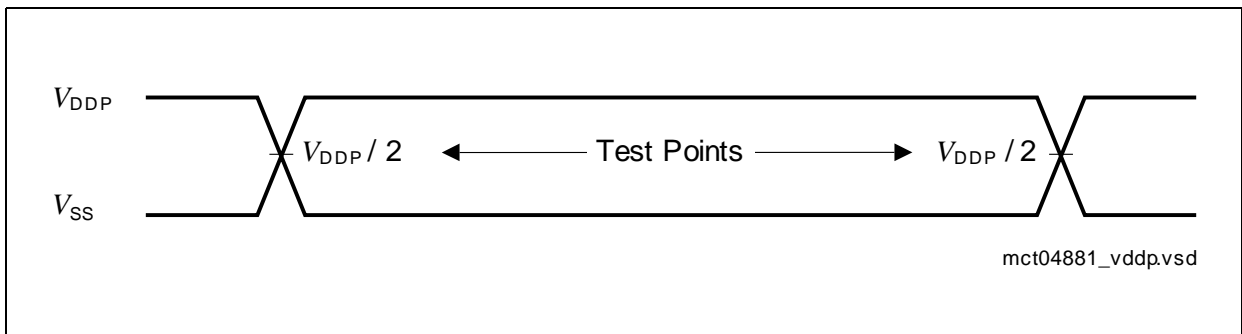


Figure 6 Testing Waveform, Output Delay

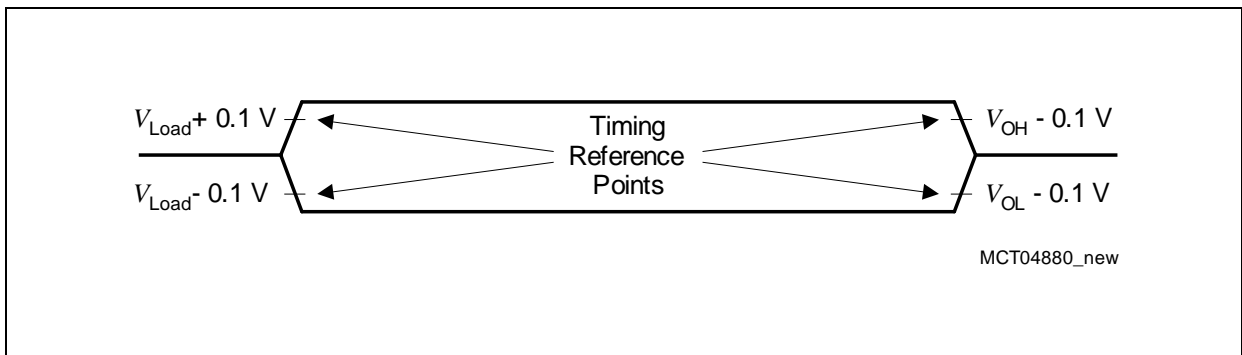


Figure 7 Testing Waveform, Output High Impedance

Electrical Parameters

5.3.2 Output Rise/Fall Times

Table 13 Output Rise/Fall Times (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------------|--------------------|--------|------|--|------|--|
| | | Min. | Typ. | Max. | | |
| Class A1 Pads | | | | | | |
| Rise/fall times ¹⁾ | t_{RA1}, t_{FA1} | — | — | 50 140 18000 150 550 65000 | ns | Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF |
| Class A2 Pads | | | | | | |
| Rise/fall times ¹⁾ | t_{RA2}, t_{FA2} | — | — | 3.7 7.5 7 18 50 140 18000 150 550 65000 | ns | Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF |

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

5.3.3 Power Sequencing

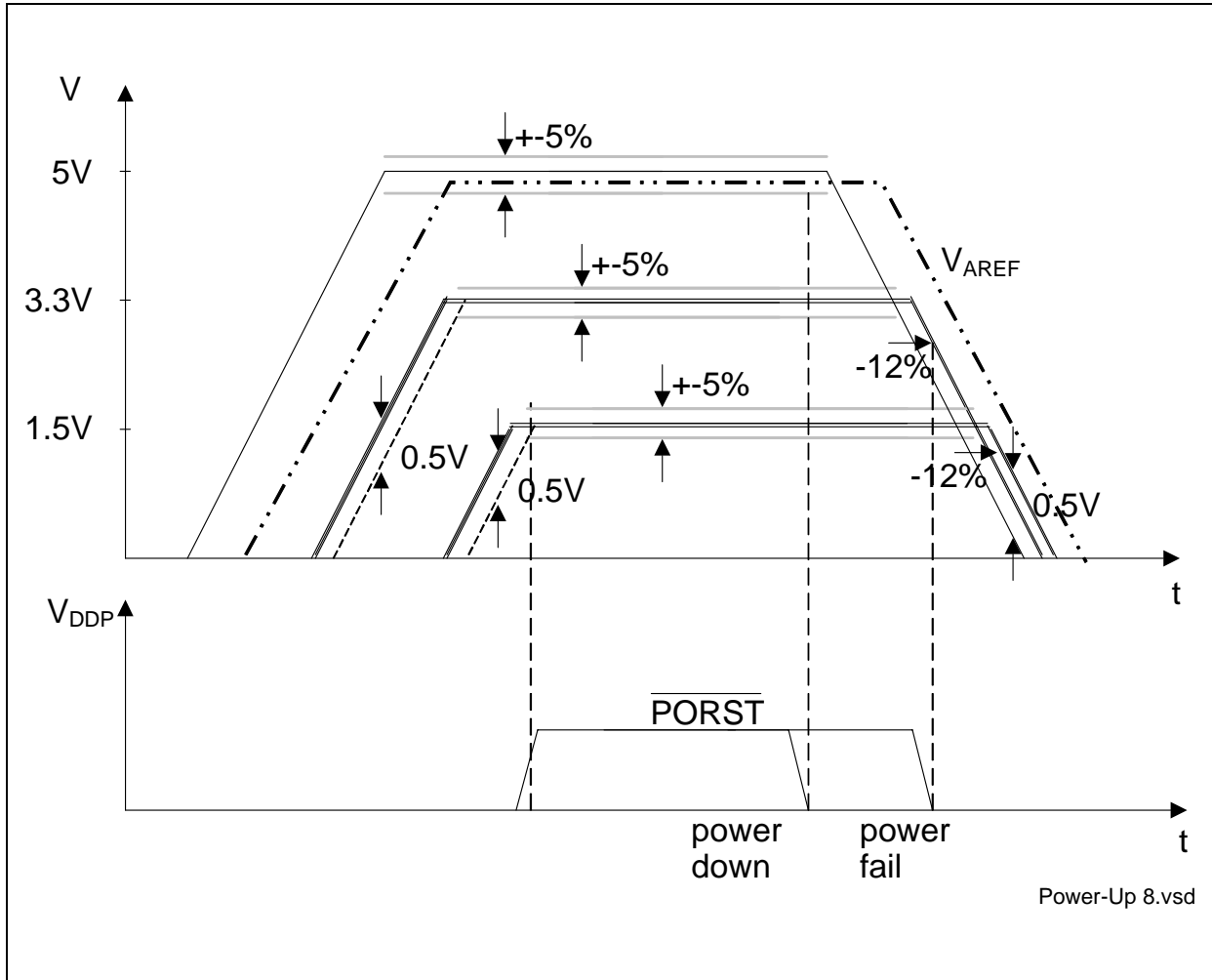


Figure 8 5 V / 3.3 V / 1.5 V Power-Up/Down Sequence

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- 1. At any moment, each power supply must be higher than any lower_power_supply - 0.5 V, or:
 $V_{DD5} > V_{DD3.3} - 0.5 \text{ V}$; $V_{DD5} > V_{DD1.5} - 0.5 \text{ V}$; $V_{DD3.3} > V_{DD1.5} - 0.5 \text{ V}$, see [Figure 18-8](#).
- 2. During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.5 V, and 5 V) with different names (for example V_{DDP} , V_{DDFL3} ...), that are internally connected via diodes must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example all V_{DDP}), are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

Electrical Parameters

3. The $\overline{\text{PORST}}$ signal may be deactivated after all $V_{\text{DD}5}$, $V_{\text{DD}3.3}$, $V_{\text{DD}1.5}$, and V_{AREF} power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
4. At normal power down the $\overline{\text{PORST}}$ signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
5. At power fail the $\overline{\text{PORST}}$ signal must be activated at latest when any 3.3 V or 1.5 V power supply voltage falls 12% below the nominal level. The same limit of 3.3 V-12% applies to the 5 V power supply too. If, under these conditions, the $\overline{\text{PORST}}$ is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the $\overline{\text{PORST}}$ signal should be activated as close as possible to the normal operating voltage range.
6. In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
7. Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
8. Additionally, regarding the ADC reference voltage V_{AREF} :
 - V_{AREF} must power-up at the same time or later than V_{DDM} , and
 - V_{AREF} must power-down either earlier or at latest to satisfy the condition $V_{\text{AREF}} < V_{\text{DDM}} + 0.5 \text{ V}$. This is required in order to prevent discharge of V_{AREF} filter capacitance through the ESD diodes through the V_{DDM} power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

5.3.4 Power, Pad and Reset Timing

Table 14 Power, Pad and Reset Timing Parameters

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|--|-------------|----|-------------------------------------|------|----------------------|-----------|--|
| | | | Min. | Typ. | Max. | | |
| Min. V_{DDP} voltage to ensure defined pad states ¹⁾ | V_{DDPPA} | CC | 0.6 | — | — | V | — |
| Oscillator start-up time ²⁾ | t_{OSCS} | CC | — | — | 10 | ms | — |
| Minimum \overline{PORST} active time after power supplies are stable at operating levels | t_{POA} | SR | 10 | — | — | ms | — |
| $\overline{ESR0}$ pulse width | t_{HD} | CC | program mable ³⁾⁵⁾ | — | — | f_{SYS} | — |
| \overline{PORST} rise time | t_{POR} | SR | — | — | 50 | ms | — |
| Setup time to \overline{PORST} rising edge ⁴⁾ | t_{POS} | SR | 0 | — | — | ns | — |
| Hold time from \overline{PORST} rising edge | t_{POH} | SR | 100 | — | — | ns | $\overline{TESTMODE}$ \overline{TRST} |
| Setup time to $\overline{ESR0}$ rising edge | t_{HDS} | SR | 0 | — | — | ns | — |
| Hold time from $\overline{ESR0}$ rising edge | t_{HDH} | SR | $16 \times 1/f_{SYS}$ ⁵⁾ | — | — | ns | HWCFG |
| Ports inactive after \overline{PORST} reset active ⁶⁾⁷⁾ | t_{PIP} | CC | — | — | 150 | ns | — |
| Ports inactive after $\overline{ESR0}$ reset active (and for all logic) | t_{PI} | CC | — | — | $8 \times 1/f_{SYS}$ | ns | — |
| Power on Reset Boot Time ⁸⁾ | t_{BP} | CC | — | — | 2.5 | ms | — |
| Application Reset Boot Time ⁹⁾ | t_B | CC | 150 | — | 960 | μs | $f_{CPU}=80MHz$ |
| | | | | | 1.7 | ms | $f_{CPU}=40MHz$ |

1) This parameter is valid under assumption that \overline{PORST} signal is constantly at low level during the power-up/power-down of the V_{DDP} .

Electrical Parameters

- 2) t_{OSCS} is defined from the moment when $V_{DDOSC3} = 3.13 \text{ V}$ until the oscillations reach an amplitude at XTAL1 of $0,3 \times V_{DDOSC3}$. This parameter is verified by device characterization. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystal suppliers.
- 3) Any $\overline{ESR0}$ activation is internally prolonged to SCU_RSTCNTCON.RELSA FPI bus clock (f_{FPI}) cycles.
- 4) Applicable for input pins $\overline{TESTMODE}$ and \overline{TRST} pins.
- 5) $f_{FPI} = f_{CPU} / 2$
- 6) Not subject to production test, verified by design / characterization.
- 7) This parameter includes the delay of the analog spike filter in the \overline{PORST} pad.
- 8) The duration of the boot-time is defined between the rising edge of the \overline{PORST} and the moment when the first user instruction has entered the CPU and its processing starts.
- 9) The duration of the boot time is defined between the following events:
 1. Hardware reset: the falling edge of a short $\overline{ESR0}$ pulse and the moment when the first user instruction has entered the CPU and its processing starts, if the $\overline{ESR0}$ pulse is shorter than $SCU_RSTCNTCON.RELSA \times T_{FPI}$.
If the $\overline{ESR0}$ pulse is longer than $SCU_RSTCNTCON.RELSA \times T_{FPI}$, only the time beyond it should be added to the boot time ($\overline{ESR0}$ falling edge to first user instruction).
 2. Software reset: the moment of starting the software reset and the moment when the first user instruction has entered the CPU and its processing starts

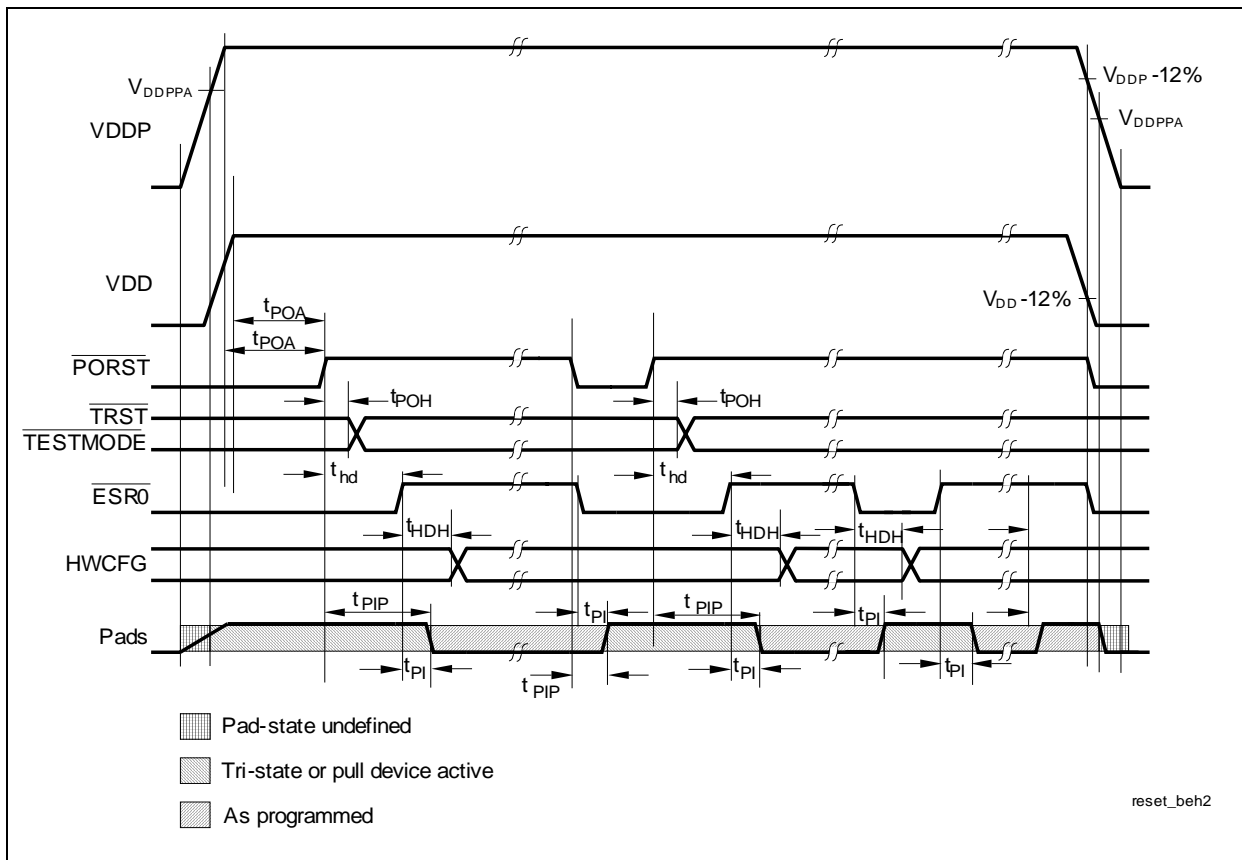


Figure 9 Power, Pad and Reset Timing

5.3.5 Phase Locked Loop (PLL)

Note: All PLL characteristics defined on this and the next page are not subject to production test, but verified by design characterization.

Table 15 PLL Parameters (Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|---------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Accumulated jitter | $ D_m $ | – | – | 7 | ns | – |
| VCO frequency range | f_{VCO} | 400 | – | 800 | MHz | – |
| VCO input frequency range | f_{REF} | 8 | – | 16 | MHz | – |
| PLL base frequency ¹⁾ | $f_{PLLBASE}$ | 50 | 200 | 320 | MHz | – |
| PLL lock-in time | t_L | – | – | 200 | μs | – |

1) The CPU base frequency with which the application software starts after PORST is calculated by dividing the limit values by 16 (this is the K2 factor after reset).

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the LMB-Bus clock f_{LMB}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using waitstates and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the K2 - factor, the LMB clock frequency f_{LMB} in [MHz], and the number m of consecutive f_{LMB} clock periods.

$$\text{for } (K2 \leq 100) \quad \text{and} \quad (m \leq (f_{LMB}[\text{MHz}])/2)$$

$$|D_m[\text{ns}]| = \left(\frac{740}{K2 \times f_{LMB}[\text{MHz}]} + 5 \right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[\text{MHz}] - 1} + 0,01 \times K2 \right) \quad (2)$$

$$\text{else} \quad |D_m[\text{ns}]| = \frac{740}{K2 \times f_{LMB}[\text{MHz}]} + 5 \quad (3)$$

Electrical Parameters

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency f_{LMB} results in a higher absolute maximum jitter value.

Figure 18-10 gives the jitter curves for several K2 / f_{LMB} combinations.

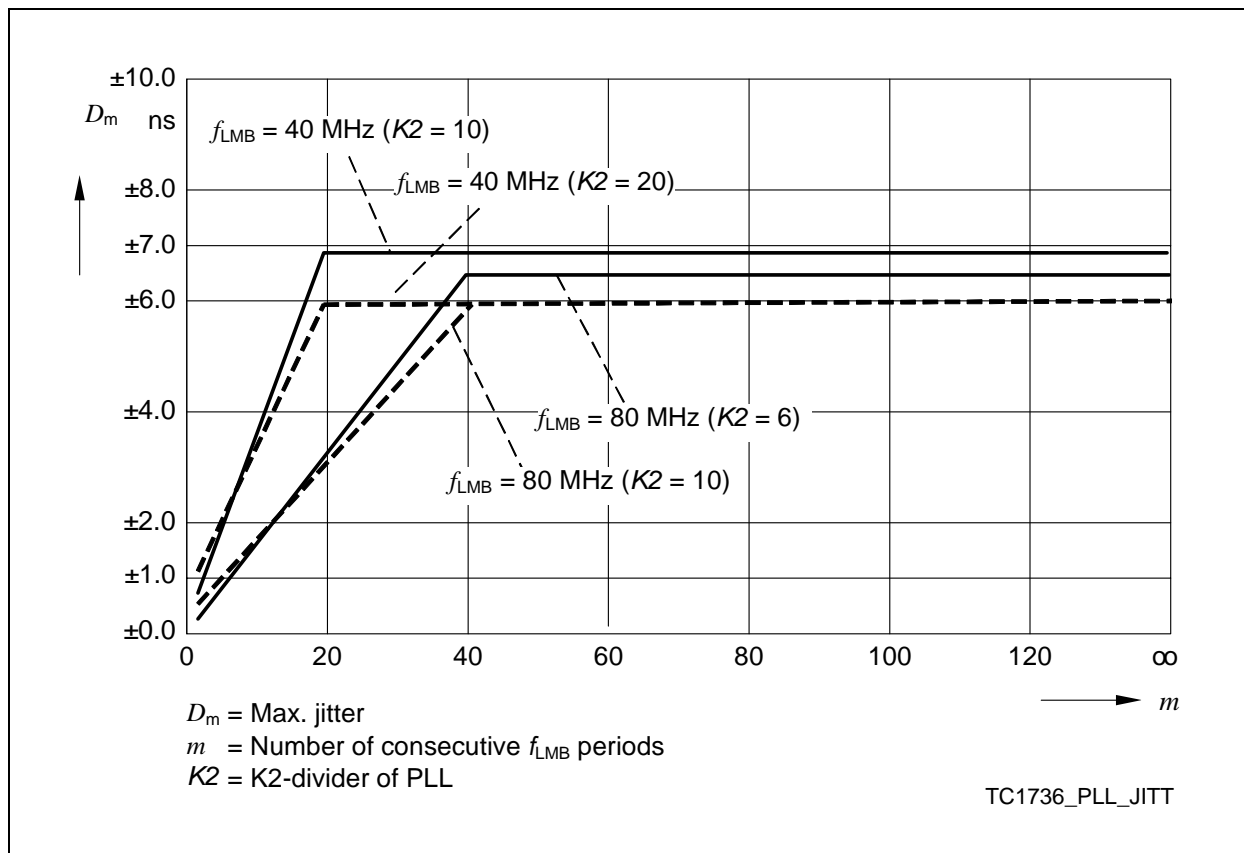


Figure 10 Approximated Maximum Accumulated PLL Jitter for Typical LMB-Bus Clock Frequencies f_{LMB}

Note: The specified PLL jitter values are valid if the capacitive load per output pin does not exceed $C_L = 20$ pF with the maximum driver and sharp edge. In case of applications with many pins with high loads, driver strengths and toggle rates the specified jitter values could be exceeded.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} at pin 85 and V_{SSOSC} at pin 83, is limited to a peak-to-peak voltage of $V_{\text{PP}} = 100$ mV for noise frequencies below 300 KHz and $V_{\text{PP}} = 40$ mV for noise frequencies above 300 KHz.

The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC} at pin 84 and V_{SSOSC} at pin 83, is limited to a peak-to-peak voltage of $V_{\text{PP}} = 100$ mV for noise frequencies below 300 KHz and $V_{\text{PP}} = 40$ mV for noise frequencies above 300 KHz.

Electrical Parameters

These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

5.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 16 JTAG Interface Timing Parameters
(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| TCK clock period | t_1 SR | 25 | – | – | ns | – |
| TCK high time | t_2 SR | 12 | – | – | ns | – |
| TCK low time | t_3 SR | 10 | – | – | ns | – |
| TCK clock rise time | t_4 SR | – | – | 4 | ns | – |
| TCK clock fall time | t_5 SR | – | – | 4 | ns | – |
| TDI/TMS setup to TCK rising edge | t_6 SR | 6 | – | – | ns | – |
| TDI/TMS hold after TCK rising edge | t_7 SR | 6 | – | – | ns | – |
| TDO valid after TCK falling edge ¹⁾ (propagation delay) | t_8 CC | – | – | 13 | ns | $C_L = 50$ pF |
| | t_8 CC | – | – | 3 | ns | $C_L = 20$ pF |
| TDO hold after TCK falling edge ¹⁾ | t_{18} CC | 2 | – | – | ns | |
| TDO high imped. to valid from TCK falling edge ¹⁾²⁾ | t_9 CC | – | – | 14 | ns | $C_L = 50$ pF |
| TDO valid to high imped. from TCK falling edge ¹⁾ | t_{10} CC | – | – | 13.5 | ns | $C_L = 50$ pF |

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

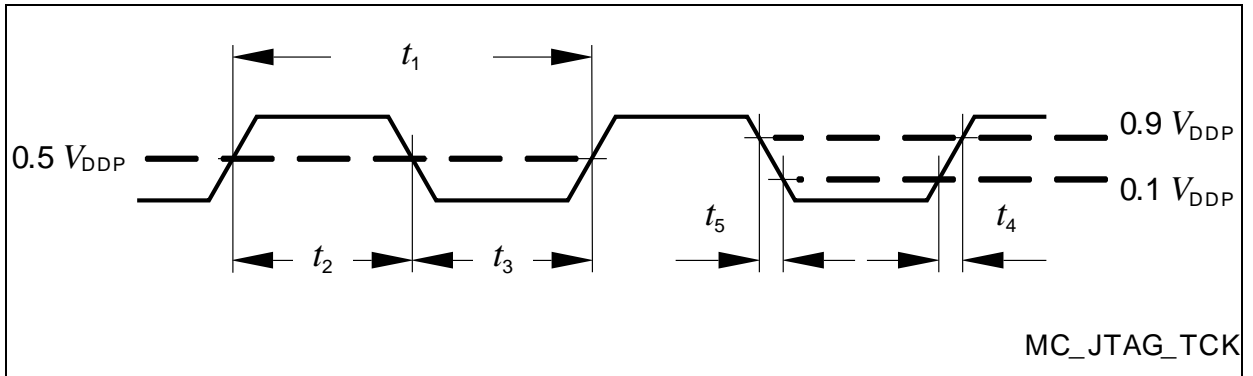


Figure 11 Test Clock Timing (TCK)

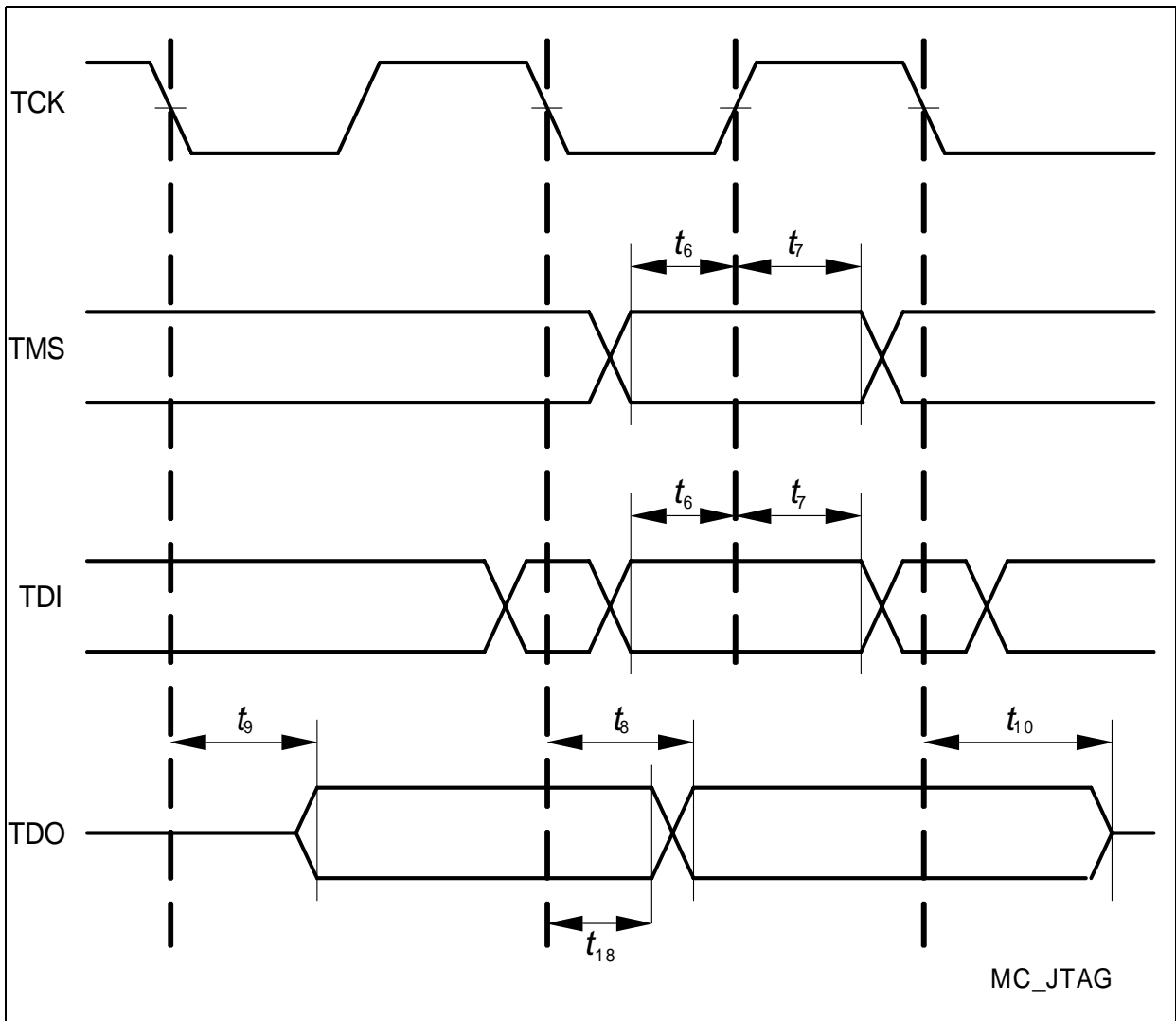


Figure 12 JTAG Timing

Electrical Parameters

5.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 17 DAP Interface Timing Parameters
(Operating Conditions apply)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------|--------|------|------|------|--------------------------|
| | | Min. | Typ. | Max. | | |
| DAP0 clock period | t_{11} SR | 12.5 | – | – | ns | – |
| DAP0 high time | t_{12} SR | 4 | – | – | ns | – |
| DAP0 low time | t_{13} SR | 4 | – | – | ns | – |
| DAP0 clock rise time | t_{14} SR | – | – | 2 | ns | – |
| DAP0 clock fall time | t_{15} SR | – | – | 2 | ns | – |
| DAP1 setup to DAP0 rising edge | t_{16} SR | 6 | – | – | ns | – |
| DAP1 hold after DAP0 rising edge | t_{17} SR | 6 | – | – | ns | – |
| DAP1 valid per DAP0 clock period ¹⁾ | t_{19} SR | 8 | – | – | ns | 80 MHz, $C_L = 20$ pF |
| | t_{19} SR | 10 | – | – | ns | 40 MHz, $C_L = 50$ pF |

1) The Host has to find a suitable sampling point by analyzing the sync telegram response.

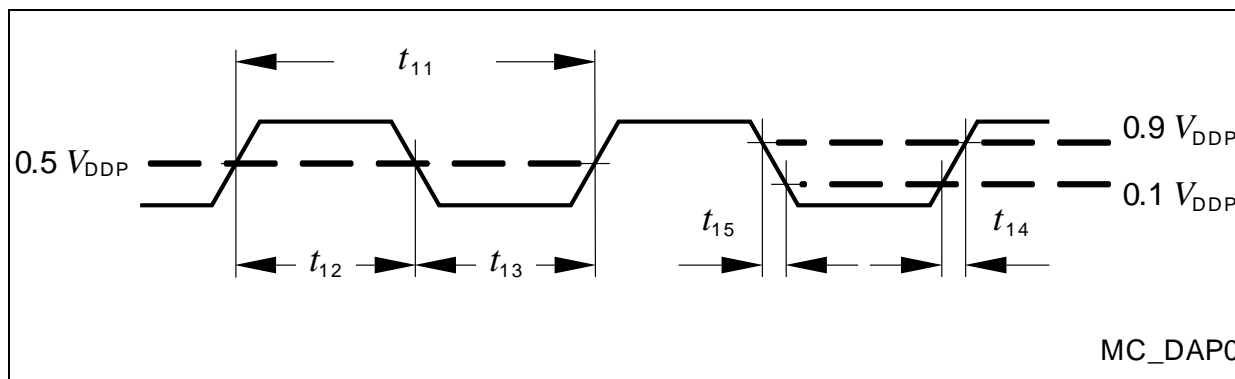


Figure 13 Test Clock Timing (DAP0)

Electrical Parameters

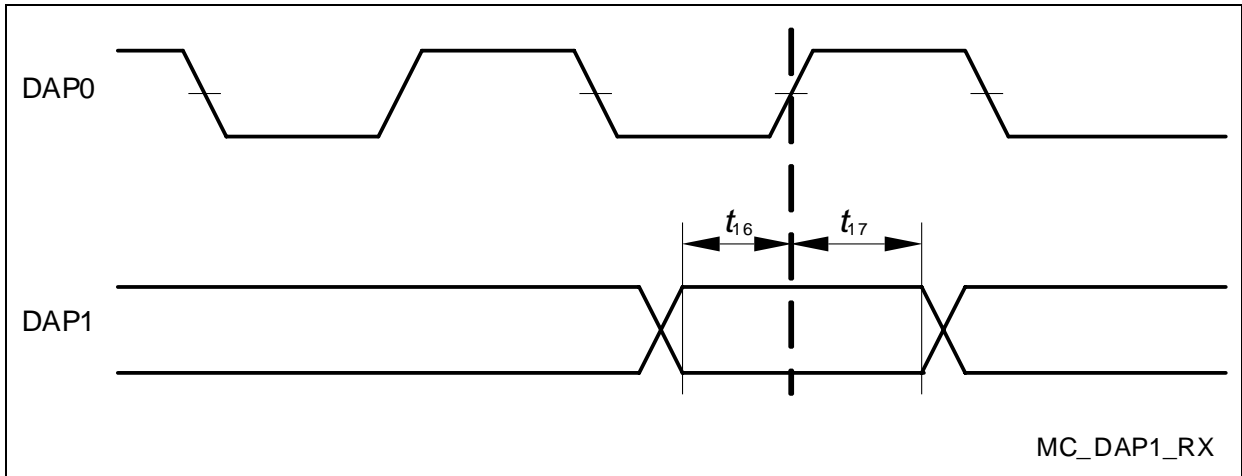


Figure 14 DAP Timing Host to Device

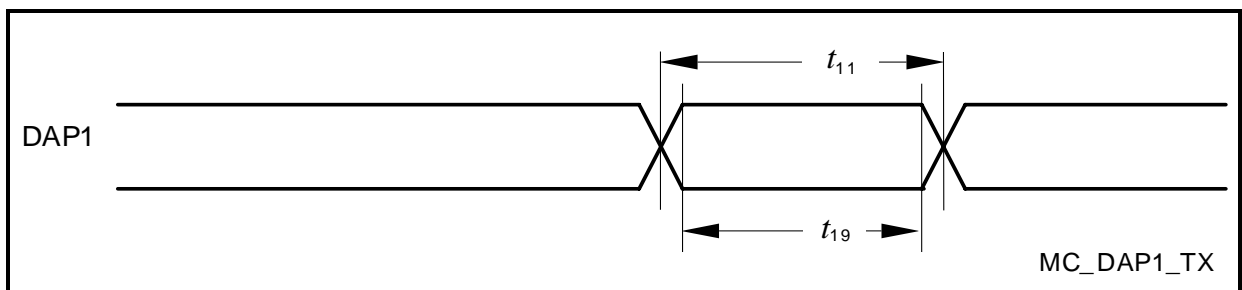


Figure 15 DAP Timing Device to Host

5.3.8 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design / characterization.

5.3.8.1 Micro Link Interface (MLI) Timing

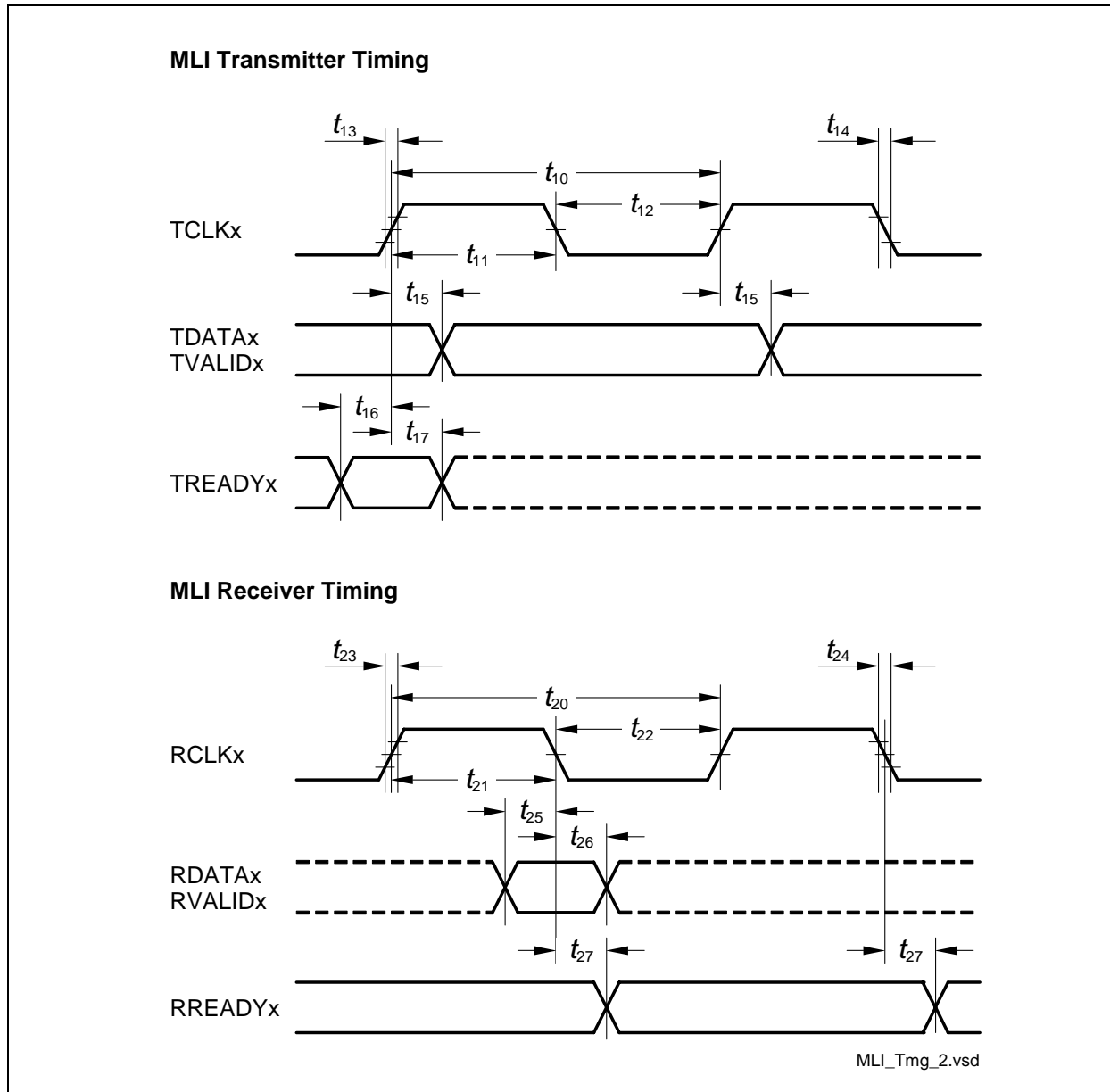


Figure 16 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

Electrical Parameters

Table 18 MLI Transmitter/Receiver Timing
(Operating Conditions apply), $C_L = 50$ pF

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-------------|---------------------------|---------------------|----------------------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| MLI Transmitter Timing | | | | | | |
| TCLK clock period | t_{10} CC | $2 \times T_{\text{MLI}}$ | — | — | ns | 1) |
| TCLK high time | t_{11} CC | $0.45 \times t_{10}$ | $0.5 \times t_{10}$ | $0.55 \times t_{10}$ | ns | 2)3) |
| TCLK low time | t_{12} CC | $0.45 \times t_{10}$ | $0.5 \times t_{10}$ | $0.55 \times t_{10}$ | ns | 2)3) |
| TCLK rise time | t_{13} CC | — | — | 4) | ns | — |
| TCLK fall time | t_{14} CC | — | — | 4) | ns | — |
| TDATA/TVALID output delay time | t_{15} CC | -3 | — | 4.4 | ns | — |
| TREADY setup time to TCLK rising edge | t_{16} SR | 18 | — | — | ns | — |
| TREADY hold time from TCLK rising edge | t_{17} SR | 0 | — | — | ns | — |
| MLI Receiver Timing | | | | | | |
| RCLK clock period | t_{20} SR | $1 \times T_{\text{MLI}}$ | — | — | ns | 1) |
| RCLK high time | t_{21} SR | — | $0.5 \times t_{20}$ | — | ns | 5)6) |
| RCLK low time | t_{22} SR | — | $0.5 \times t_{20}$ | — | ns | 5)6) |
| RCLK rise time | t_{23} SR | — | — | 4 | ns | 7) |
| RCLK fall time | t_{24} SR | — | — | 4 | ns | 7) |
| RDATA/RVALID setup time to RCLK falling edge | t_{25} SR | 4.2 | — | — | ns | — |
| RDATA/RVALID hold time from RCLK rising edge | t_{26} SR | 2.2 | — | — | ns | — |
| RREADY output delay time | t_{27} CC | 0 | — | 16 | ns | — |

1) $T_{MLImin.} = T_{SYS} = 1/f_{SYS}$. When $f_{SYS} = 80$ MHz, $t_{10} = 25$ ns and $t_{20} = 12.5$ ns.

2) The following formula is valid: $t_{11} + t_{12} = t_{10}$

3) The min./max. TCLK low/high times t_{11}/t_{12} include the PLL jitter of f_{SYS} . Fractional divider settings must be regarded additionally to t_{11}/t_{12} .

4) For high-speed MLI interface, strong driver sharp edge selection (class A2 pad) is recommended for TCLK.

5) The following formula is valid: $t_{21} + t_{22} = t_{20}$

6) The min. and max. value of is parameter can be adjusted by considering the other receiver timing parameters.

Electrical Parameters

- 7) The RCLK max. input rise/fall times are best case parameters for $f_{SYS} = 80$ MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

5.3.8.2 Micro Second Channel (MSC) Interface Timing

Table 19 MSC Interface Timing (Operating Conditions apply), $C_L = 50$ pF

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|-------------|----------------------------------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| FCLP clock period ¹⁾²⁾ | t_{40} CC | $2 \times T_{MSC}$ ³⁾ | — | — | ns | — |
| SOP/ENx outputs delay from FCLP rising edge | t_{45} CC | -10 | | 10 | ns | — |
| SDI bit time | t_{46} CC | $8 \times T_{MSC}$ | | — | ns | — |
| SDI rise time | t_{48} SR | | | 100 | ns | — |
| SDI fall time | t_{49} SR | | | 100 | ns | — |

1) FCLP signal rise/fall times are the same as the A2 Pads rise/fall times.

2) FCLP signal high and low can be minimum $1 \times T_{MSC}$.

3) $T_{MSCmin} = T_{SYS} = 1/f_{SYS}$. When $f_{SYS} = 80$ MHz, $t_{40} = 25$ ns

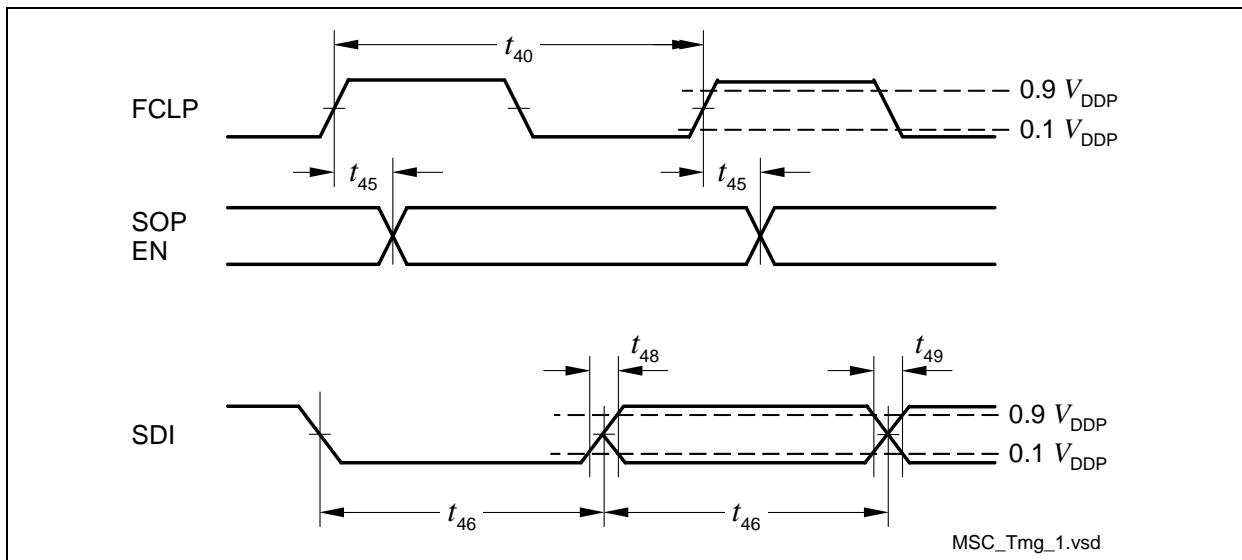


Figure 17 MSC Interface Timing

Note: Sample the data at SOP with the falling edge of FCLP in the target device.

5.3.8.3 SSC Master / Slave Mode Timing

Table 20 SSC Master/Slave Mode Timing
(Operating Conditions apply), $C_L = 50 \text{ pF}$

| Parameter | Symbol | | Values | | | Unit | Note / Test Con- dition |
|--|-----------------|----|--------------------|------|------|------|-------------------------------|
| | | | Min. | Typ. | Max. | | |
| Master Mode Timing | | | | | | | |
| SCLK clock period | t_{50} | CC | $2 \times T_{SSC}$ | — | — | ns | 1)2)3) |
| MTSR/SLSOx delay from SCLK rising edge | t_{51} | CC | 0 | — | 8 | ns | — |
| MRST setup to SCLK falling edge | t_{52} | SR | 13 | — | — | ns | 3) |
| MRST hold from SCLK falling edge | t_{53} | SR | 0 | — | — | ns | 3) |
| Slave Mode Timing | | | | | | | |
| SCLK clock period | t_{54} | SR | $4 \times T_{SSC}$ | — | — | ns | 1)3) |
| SCLK duty cycle | t_{55}/t_{54} | SR | 45 | — | 55 | % | — |
| MTSR setup to SCLK latching edge | t_{56} | SR | $T_{SSC} + 5$ | — | — | ns | 3)4) |
| MTSR hold from SCLK latching edge | t_{57} | SR | $T_{SSC} + 5$ | — | — | ns | 3)4) |
| SLSI setup to first SCLK latching edge | t_{58} | SR | $T_{SSC} + 5$ | — | — | ns | 3) |
| SLSI hold from last SCLK latching edge | t_{59} | SR | 7 | — | — | ns | — |
| MRST delay from SCLK shift edge | t_{60} | CC | 0 | — | 15 | ns | — |
| SLSI to valid data on MRST | t_{61} | CC | — | — | 10 | ns | — |

1) SCLK signal rise/fall times are the same as the A2 Pads rise/fall times.

2) SCLK signal high and low times can be minimum $1 \times T_{SSC}$.

3) $T_{SSCmin} = T_{SYS} = 1/f_{SYS}$. When $f_{SYS} = 80 \text{ MHz}$, $t_{50} = 25 \text{ ns}$.

4) Fractional divider switched off, SSC internal baud rate generation used.

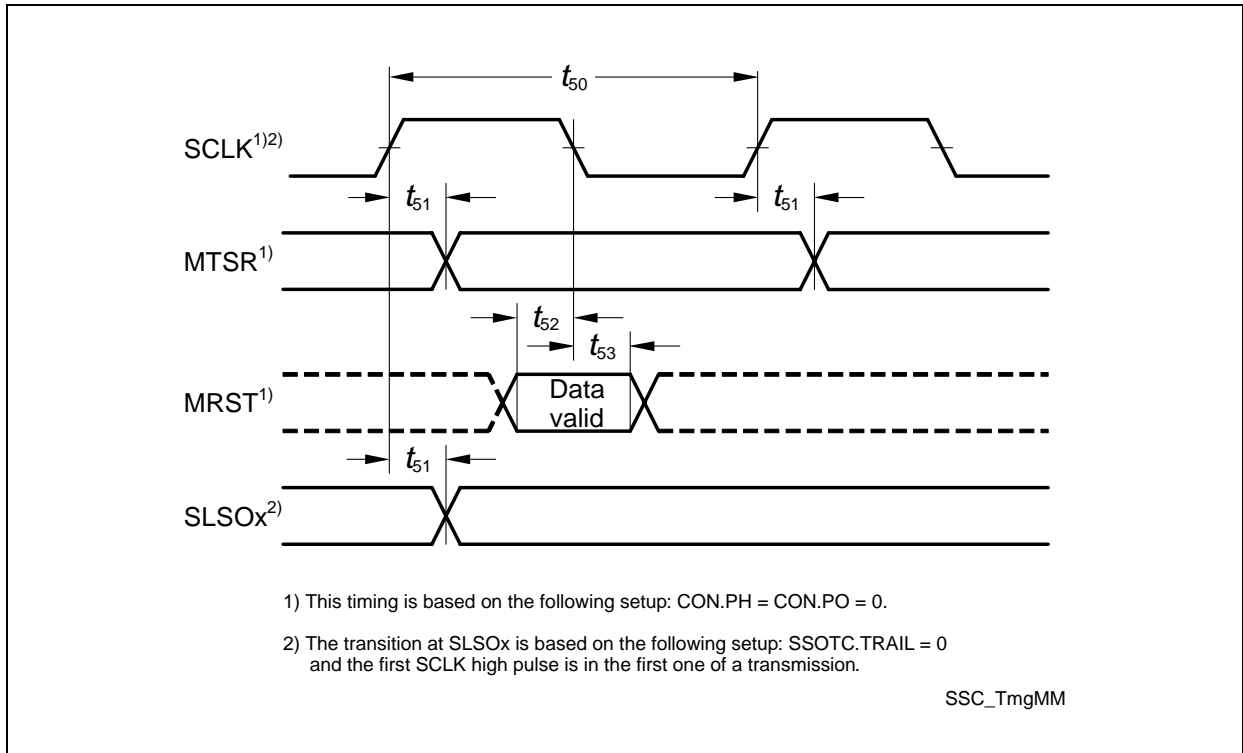


Figure 18 SSC Master Mode Timing

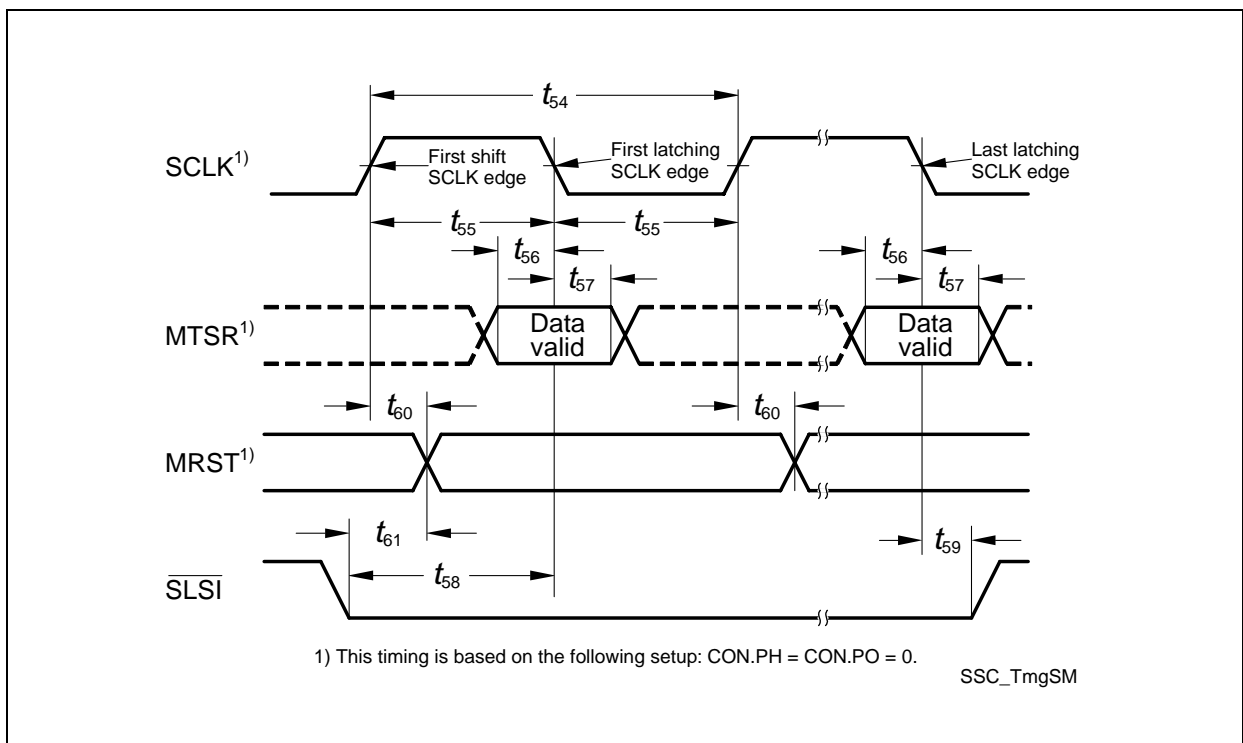


Figure 19 SSC Slave Mode Timing

5.4 Package and Reliability

5.4.1 Package Parameters

Table 21 Thermal Parameters (Operating Conditions apply)

| Device | Package | $R_{\Theta JCT}^{1)}$ | $R_{\Theta JCB}^{1)}$ | $R_{\Theta JLeads}^{1)}$ | Unit | Note |
|--------|----------------|-----------------------|-----------------------|--------------------------|------|------|
| TC1736 | PG-LQFP-144-10 | 8.0 | 7.5 | 34.0 | K/W | |

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT} , R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT} , R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT} , R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.

Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

Electrical Parameters

5.4.3 Flash Memory Parameters

The data retention time of the TC1736's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

Table 22 Flash Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|----------------------|--------|------|-----------------------------|--------|-----------------------------------|
| | | Min. | Typ. | Max. | | |
| Program Flash Retention Time, Physical Sector ¹⁾²⁾ | t_{RET} CC | 20 | – | – | years | Max. 1000 erase/program cycles |
| Program Flash Retention Time Logical Sector ¹⁾²⁾ | t_{RETL} CC | 20 | – | – | years | Max. 100 erase/program cycles |
| Data Flash Endurance per 16 KB Sector | N_{E} CC | 30 000 | – | – | cycles | Max. data retention time 5 years |
| Data Flash Endurance, EEPROM Emulation (4 × 8 KB) | N_{E8} CC | 120000 | – | – | cycles | Max. data retention time 5 years |
| Programming Time per Page ³⁾ | t_{PR} CC | – | – | 5 | ms | – |
| Program Flash Erase Time per 256-KB Sector | t_{ERP} CC | – | – | 5 | s | $f_{\text{CPU}} = 80 \text{ MHz}$ |
| Data Flash Erase Time for 2 x 16-KB Sector | t_{ERD} CC | – | – | 1.25 | s | $f_{\text{CPU}} = 80 \text{ MHz}$ |
| Wake-up time | t_{WU} CC | – | – | $4000/f_{\text{CPU}} + 180$ | μs | – |

1) Storage and inactive time included.

2) At average weighted junction temperature $T_j = 100^\circ\text{C}$, or the retention time at average weighted temperature of $T_j = 110^\circ\text{C}$ is minimum 10 years, or the retention time at average weighted temperature of $T_j = 150^\circ\text{C}$ is minimum 0.7 years.

3) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.

5.4.4 Quality Declarations

Table 23 Quality Parameters

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|--|-----------|--------|------|-------|-------|--|
| | | Min. | Typ. | Max. | | |
| Operation Lifetime ¹⁾ | t_{OP} | — | — | 24000 | hours | — ²⁾ ³⁾ |
| ESD susceptibility according to Human Body Model (HBM) | V_{HBM} | — | — | 2000 | V | Conforming to JESD22-A114-B |
| ESD susceptibility according to Charged Device Model (CDM) | V_{CDM} | — | — | 500 | V | Conforming to JESD22-C101-C |
| Moisture Sensitivity Level | MSL | — | — | 3 | — | Conforming to Jedec J-STD-020C for 240°C |

1) This lifetime refers only to the time when the device is powered on.

2) For worst-case temperature profile equivalent to:

2000 hours at $T_j = 150^{\circ}\text{C}$

16000 hours at $T_j = 125^{\circ}\text{C}$

6000 hours at $T_j = 110^{\circ}\text{C}$

3) This 30000 hours worst-case temperature profile is also covered:

300 hours at $T_j = 150^{\circ}\text{C}$

1000 hours at $T_j = 140^{\circ}\text{C}$

1700 hours at $T_j = 130^{\circ}\text{C}$

24000 hours at $T_j = 120^{\circ}\text{C}$

3000 hours at $T_j = 110^{\circ}\text{C}$

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