

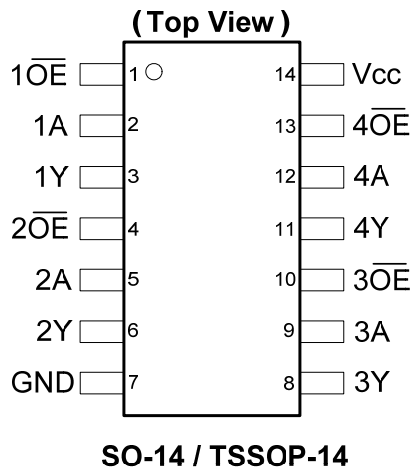
## Description

The 74AHCT125 provides provides four independent buffer gates with 3-state outputs. Each buffer has a separate enable pin that if driven with a high logic level places the corresponding output in the high impedance state. The device is designed for operation with a power supply range of 4.5V to 5.5V.

## Features

- Wide Supply Voltage Range from 4.5V to 5.5V
- Inputs Are TTL Voltage Level Compatible
- Outputs Sink or Source 8mA at  $V_{CC} = 4.5V$
- CMOS Low Power Consumption
- Schmitt Trigger Action at All Inputs
- ESD Protection Exceeds JESD 22
  - 200-V Machine Model (A115-A)
  - 2000-V Human Body Model (A114-A)
  - Exceeds 1000-V Charged Device Model (C101C)
- Latch-Up Exceeds 250mA per JESD 78, Class II
- Range of Package Options SO-14 and TSSOP-14
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Pin Assignments



## Applications

- General Purpose Logic
- Wide array of products such as:
  - PCs, Networking, Notebooks, Netbooks
  - Computer Peripherals, Hard Drives, CD/DVD ROM
  - TV, DVD, DVR, Set Top Box

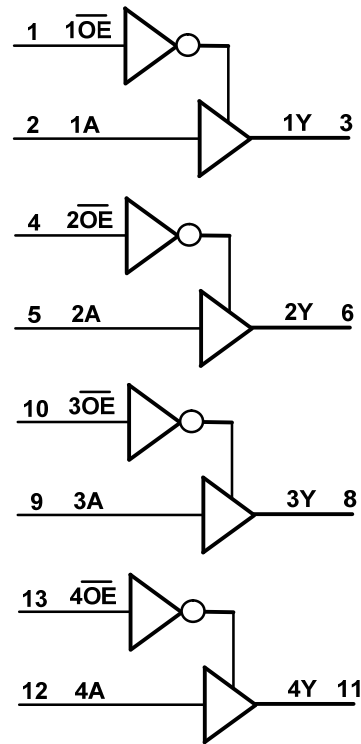
- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

[Click here for ordering information, located at the end of datasheet](#)

### Pin Descriptions

Pin Number	Pin Name	Function
1	1 $\overline{OE}$	Data Enable Input (active low)
2	1A	Data Input
3	1Y	Data Output
4	2 $\overline{OE}$	Data Enable Input (active low)
5	2A	Data Input
6	2Y	Data Output
7	GND	Ground
8	3Y	Data Output
9	3A	Data Input
10	3 $\overline{OE}$	Data Enable Input (active low)
11	4Y	Data Output
12	4A	Data Input
13	4 $\overline{OE}$	Data Enable Input (active low)
14	V <sub>CC</sub>	Supply Voltage

### Logic Diagram



### Function Table

Inputs		Output
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

### Absolute Maximum Ratings (Note 4) (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD CDM	Charged Device Model ESD Protection	1	KV
ESD MM	Machine Model ESD Protection	200	V
V <sub>CC</sub>	Supply Voltage Range	-0.5 to +7.0	V
V <sub>I</sub>	Input Voltage Range	-0.5 to +7.0	V
I <sub>IK</sub>	Input Clamp Current V <sub>I</sub> < -0.5V	-20	mA
I <sub>OK</sub>	Output Clamp Current V <sub>O</sub> < 0V	-20	mA
I <sub>OK</sub>	Output Clamp Current V <sub>O</sub> > V <sub>CC</sub>	20	mA
I <sub>O</sub>	Continuous Output Current 0V < V <sub>O</sub> < V <sub>CC</sub>	+/- 25	mA
I <sub>CC</sub>	Continuous Current Through V <sub>CC</sub>	50	mA
I <sub>GND</sub>	Continuous Current Through GND	-50	mA
T <sub>J</sub>	Operating Junction Temperature	-40 to +150	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>TOT</sub>	Total Power Dissipation	500	mW

Note: 4. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.

**Recommended Operating Conditions** (Note 5) (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage	4.5	5.5	V
$V_I$	Input Voltage	0	5.5	V
$V_O$	Output Voltage	0	$V_{CC}$	V
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate		20	ns/V
$T_A$	Operating Free-Air Temperature	-40	+125	$^\circ\text{C}$

 Note: 5. Unused inputs should be held at  $V_{CC}$  or Ground.

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Test Conditions	$V_{CC}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		$T_A = -40^\circ\text{C to } +125^\circ\text{C}$		Unit
				Min	Max	Min	Max	
$V_{IH}$	High-Level Input Voltage		4.5V to 5.5V	2.0		2.0		V
$V_{IL}$	Low-Level Input Voltage		4.5V to 5.5V		0.8		0.8	V
$V_{OH}$	High-Level Output Voltage	$I_{OH} = -50\mu\text{A}$	4.5V	4.4		4.4		V
		$I_{OH} = -8\text{mA}$	4.5V	3.80		3.70		
$V_{OL}$	Low-Level Output Voltage	$I_{OL} = 50\mu\text{A}$	4.5V		0.1		0.1	V
		$I_{OL} = 8\text{mA}$	4.5V		0.44		0.55	
$I_{OZ}$	Z State Leakage Current	$V_O = 0$ to 5.5V	5.5V		$\pm 2.5$		$\pm 10$	$\mu\text{A}$
$I_I$	Input Current	$V_I = \text{GND to } 5.5\text{V}$	3.6V		$\pm 1$		$\pm 2$	$\mu\text{A}$
$I_{CC}$	Supply Current	$V_I = \text{GND or } V_{CC}, I_O = 0$	3.6V		20		40	$\mu\text{A}$
$\Delta I_{CC}$	Additional Supply Current	One input at $V_{CC} - 2.1\text{V}$ Other pins at $V_{CC}$ or GND	5.5V		1.35		5	mA

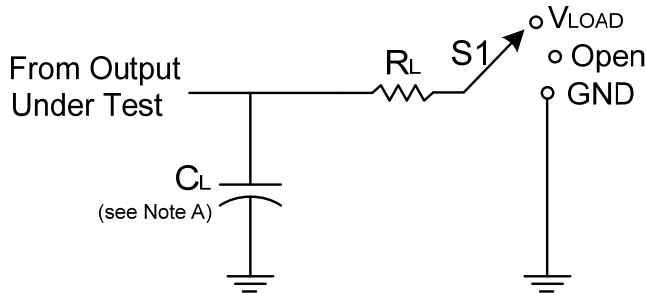
**Operating Characteristics**

Parameter		Test Conditions	$V_{CC} = 5.5\text{V}$	Unit
			Typ	
$C_{pd}$	Power Dissipation Capacitance per Gate	$f = 1\text{MHz}$	14.8	pF
$C_i$	Input Capacitance	$V_I = V_{CC} \text{ or GND}$	4.0	pF

**Switching Characteristics**

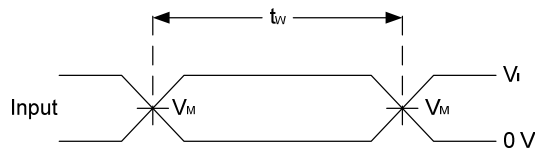
Symbol	Parameter	Test Conditions	$T_A = +25^\circ\text{C}$			$-40^\circ\text{C to } +85^\circ\text{C}$		$-40^\circ\text{C to } +125^\circ\text{C}$		Unit
			Min	Typ.	Max	Min	Max	Min	Max	
$t_{PD}$	Propagation Delay $A_N$ to $Y_N$	Figure 1 $C_L = 15\text{pF}$	0.5	3.0	5.5	0.5	6.5	0.5	7.0	ns
		Figure 1 $C_L = 50\text{pF}$	0.5	4.3	7.5	0.5	8.5	0.5	9.5	
$t_{EN}$	Enable Time $\overline{OE}_N$ to $Y_N$	Figure 1 $C_L = 15\text{pF}$	0.5	6.7	10.7	0.5	11.0	0.5	11.5	ns
		Figure 1 $C_L = 50\text{pF}$	0.5	9.8	10.9	0.5	12.1	0.5	12.5	
$t_{DIS}$	Disable Time $\overline{OE}_N$ to $Y_N$	Figure 1 $C_L = 15\text{pF}$	0.5	4.8	6.8	0.5	8.0	0.5	8.5	ns
		Figure 1 $C_L = 50\text{pF}$	0.5	6.5	8.9	0.5	10.0	0.5	11.5	

**Parameter Measurement Information**

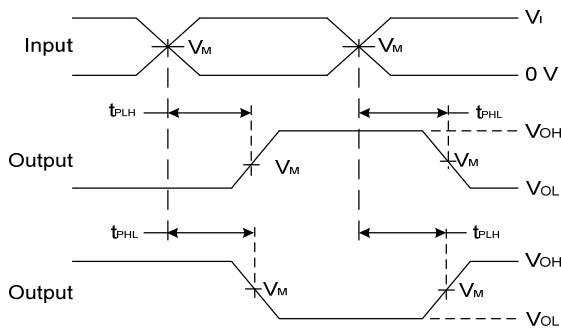


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	Vload
$t_{PHZ}/t_{PZH}$	GND

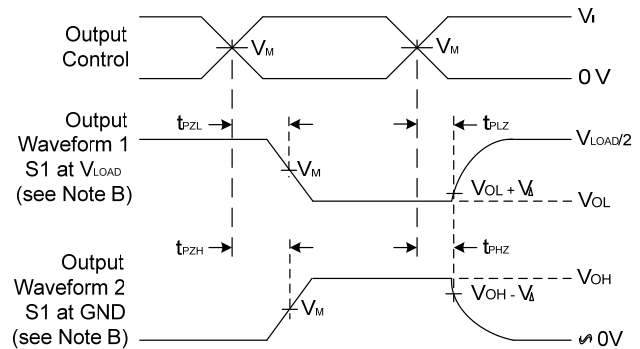
$V_{CC}$	Inputs		$V_M$ Inputs	$V_M$ Outputs	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$						
4.5V to 5.5V	3V	$\leq 3ns$	1.5V	$V_{CC}/2$	$V_{CC}$	15pF, 50pF	1K	0.3V



**Voltage Waveform Pulse Duration**



**Voltage Waveform Propagation Delay Times  
Inverting and Non Inverting Outputs**

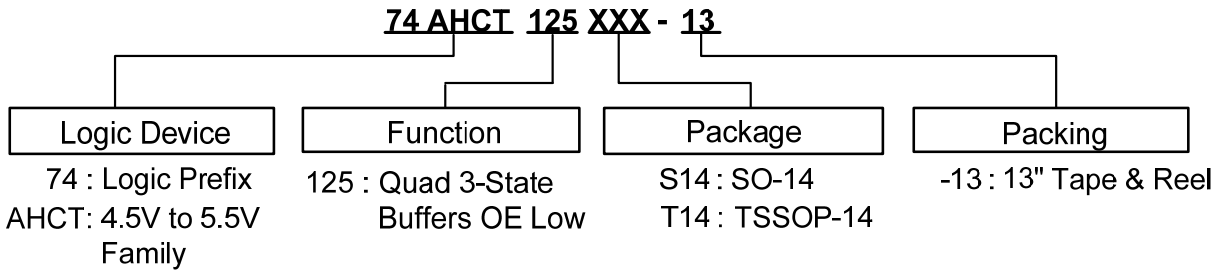


**Voltage Waveform Enable and Disable Times  
Low and High Level Enabling**

**Figure 1. Load Circuit and Voltage Waveforms**

- Notes:
- A. Includes test lead and test apparatus capacitance.
  - B. All pulses are supplied at pulse repetition rate  $\leq 1$  MHz.
  - C. Inputs are measured separately one transition per measurement.
  - D.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - E.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{EN0}$ .
  - F.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

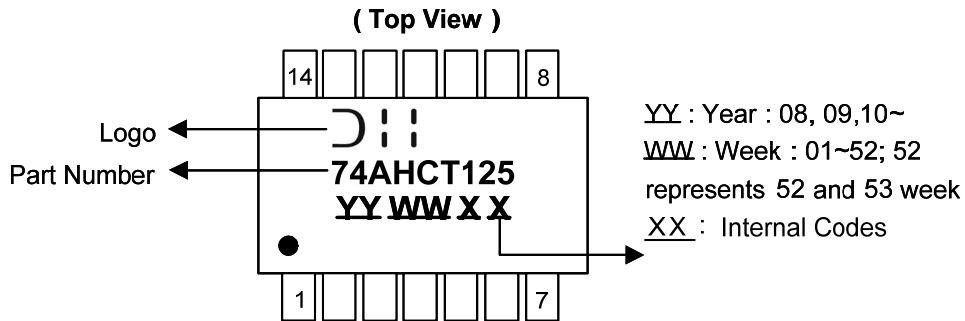
**Ordering Information**



Part Number	Package Code	Packaging	7" Tape and Reel	
			Quantity	Part Number Suffix
74AHCT125S14-13	S14	SO-14	2500/Tape & Reel	-13
74AHCT125T14-13	T14	TSSOP-14	2500/Tape & Reel	-13

**Marking Information**

(1) SO-14, TSSOP-14

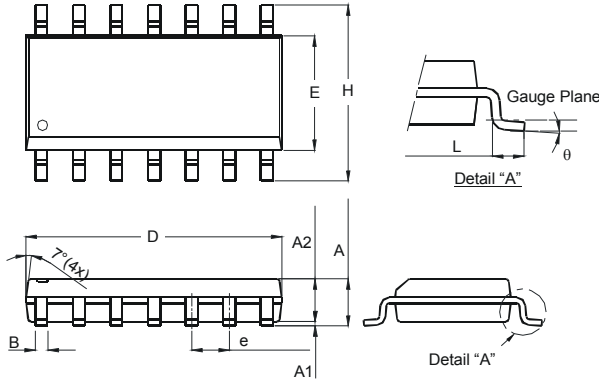


Part Number	Package
74AHCT125S14	SO-14
74AHCT125T14	TSSOP-14

**Package Outline Dimensions** (All dimensions in mm.)

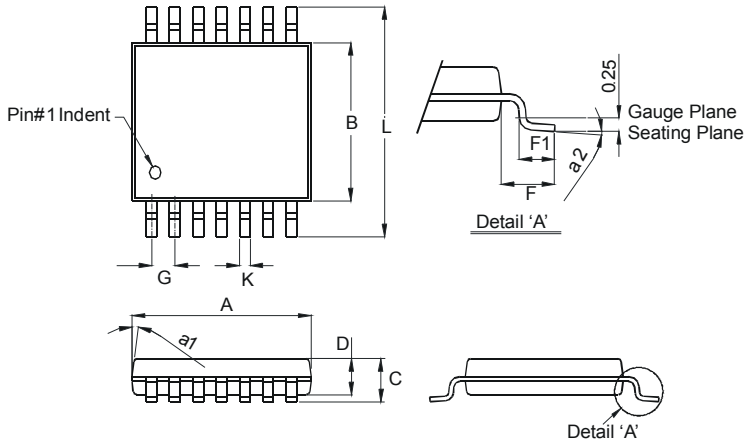
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.

**Package Type: SO-14**



SO-14		
Dim	Min	Max
A	1.47	1.73
A1	0.10	0.25
A2	1.45 Typ	
B	0.33	0.51
D	8.53	8.74
E	3.80	3.99
e	1.27 Typ	
H	5.80	6.20
L	0.38	1.27
$\theta$	0°	8°
<b>All Dimensions in mm</b>		

**Package Type: TSSOP-14**

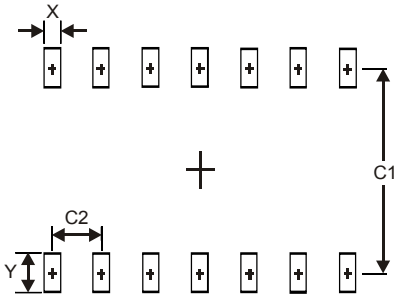


TSSOP-14		
Dim	Min	Max
a1	7° (4X)	
a2	0°	8°
A	4.9	5.10
B	4.30	4.50
C	—	1.2
D	0.8	1.05
F	1.00 Typ	
F1	0.45	0.75
G	0.65 Typ	
K	0.19	0.30
L	6.40 Typ	
<b>All Dimensions in mm</b>		

**Suggested Pad Layout**

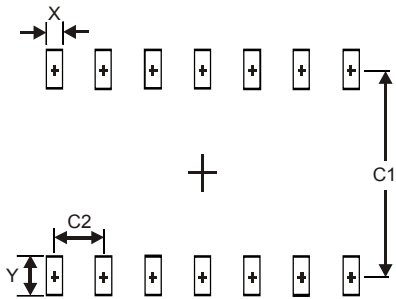
Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.

**Package Type: SO-14**



Dimensions	Value (in mm)
X	0.60
Y	1.50
C1	5.4
C2	1.27

**Package Type: TSSOP-14**



Dimensions	Value (in mm)
X	0.45
Y	1.45
C1	5.9
C2	0.65

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