

74AHC139; 74AHCT139

Dual 2-to-4 line decoder/demultiplexer

Rev. 02 — 9 May 2008

Product data sheet

1. General description

The 74AHC139; 74AHCT139 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC139; 74AHCT139 is a high-speed, dual 2-to-4 line decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs ($nA0$ and $nA1$) and providing four mutually exclusive active LOW outputs ($n\bar{Y}0$ to $n\bar{Y}3$). Each decoder has an active LOW enable input ($n\bar{E}$). When $n\bar{E}$ is HIGH, every output is forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application.

The 74AHC139; 74AHCT139 is identical to the HEF4556 of the HE4000B family.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - ◆ For 74AHC139: CMOS level
 - ◆ For 74AHCT139: TTL level
- ESD protection:
 - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
 - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

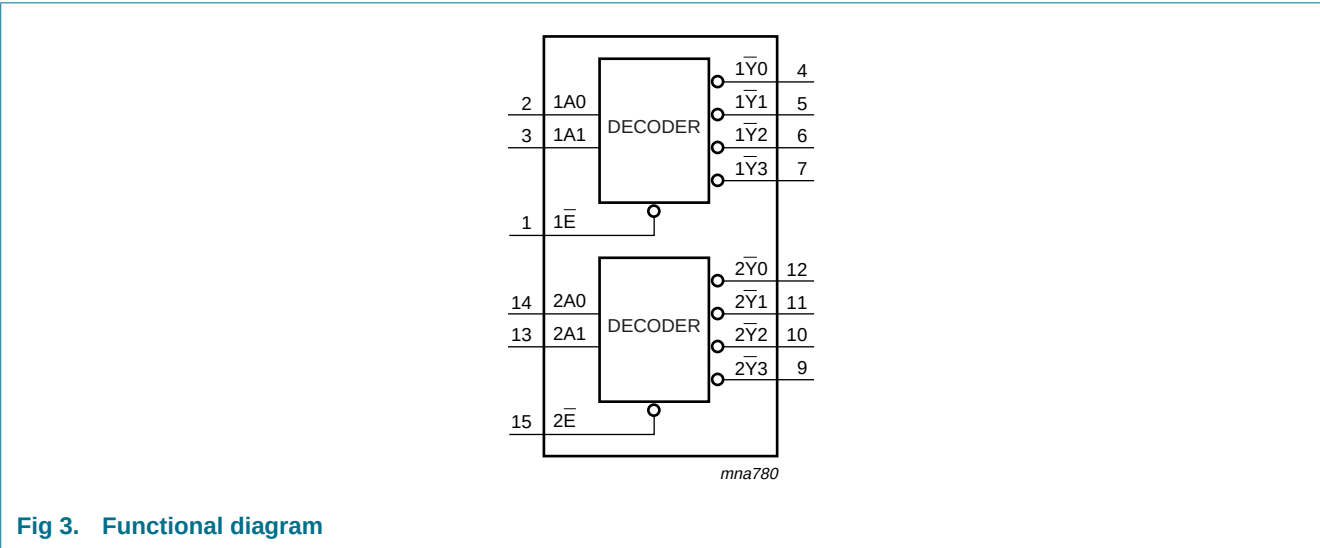
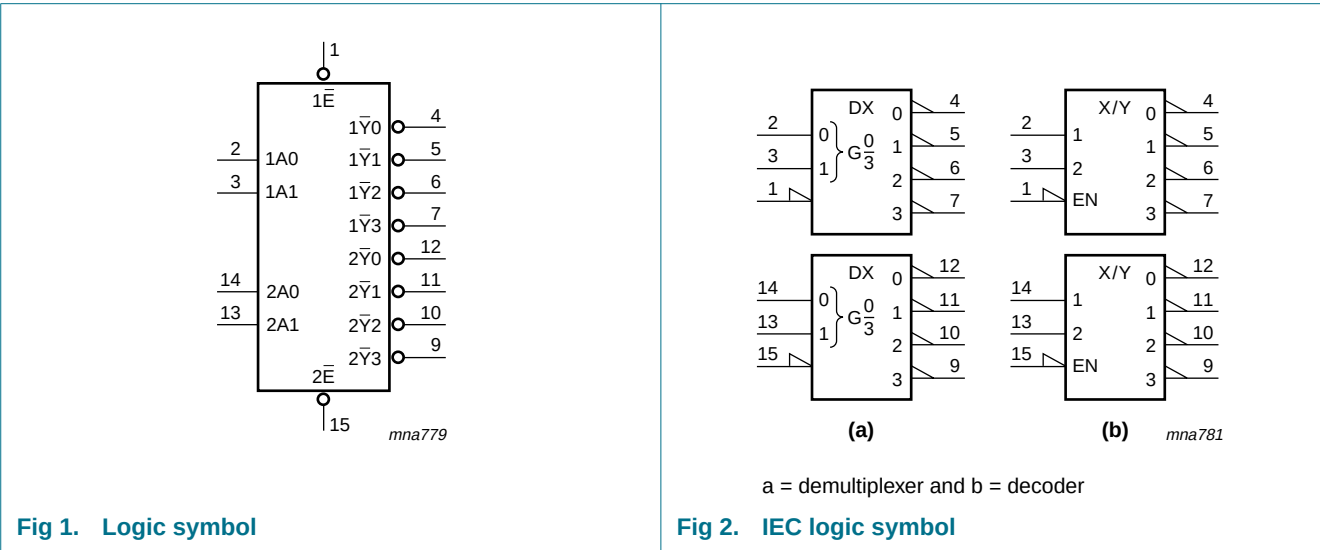
Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AHC139				
74AHC139D	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC139PW	$-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

Table 1. Ordering information ...continued

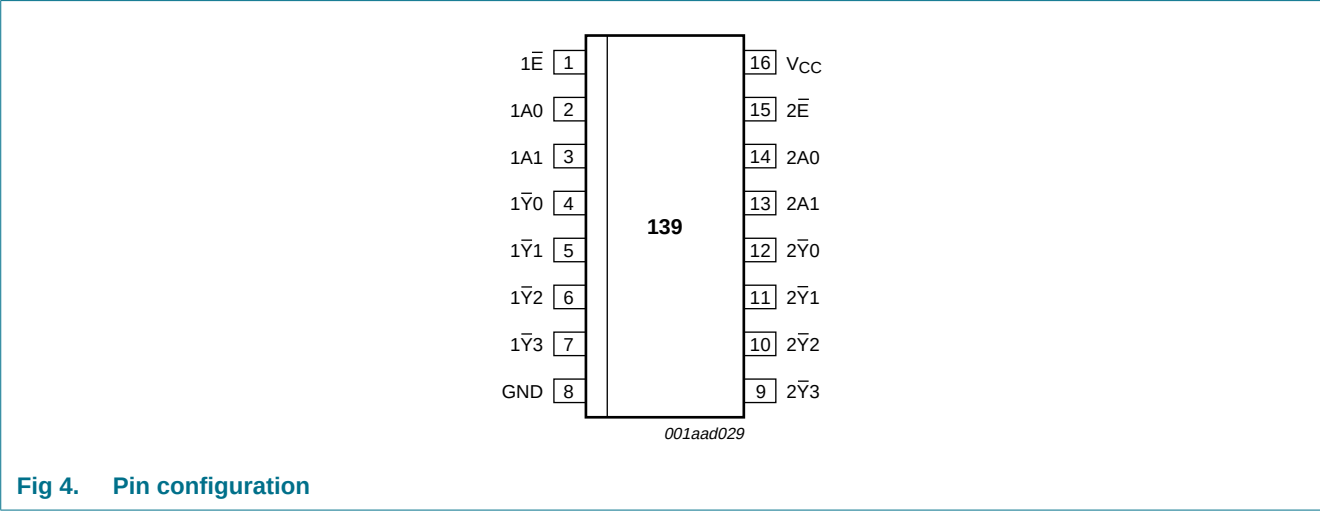
Type number	Package			
	Temperature range	Name	Description	Version
74AHCT139				
74AHCT139D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT139PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1E̅	1	enable input (active LOW)
1A0	2	address input
1A1	3	address input
1Y̅0	4	output
1Y̅1	5	output
1Y̅2	6	output
1Y̅3	7	output
GND	8	ground (0 V)
2Y̅3	9	output
2Y̅2	10	output
2Y̅1	11	output
2Y̅0	12	output
2A1	13	address input
2A0	14	address input
2E̅	15	enable input (active LOW)
VCC	16	supply voltage

6. Functional description

Table 3. Function table^[1]

Control	Input		Output			
$\overline{nE}$	nA0	nA1	$\overline{nY0}$	$\overline{nY1}$	$\overline{nY2}$	$\overline{nY3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
	H	L	H	L	H	H
	L	H	H	H	L	H
	H	H	H	H	H	L

- [1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	^[1] -20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	^[1] -20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-25	+25	mA
I_{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	^[2] -	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
For TSSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC139						
V _{CC}	supply voltage		2.0	5.0	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		−40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V
74AHCT139						
V _{CC}	supply voltage		4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		−40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC139										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = −50 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = −50 μA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = −50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = −4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = −8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF
74AHCT139										
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = -50 \mu\text{A}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -8.0 \text{ mA}$	3.94	-	-	3.80	-	3.70	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL} ; $V_{CC} = 4.5 \text{ V}$								
		$I_O = 50 \mu\text{A}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 8.0 \text{ mA}$	-	-	0.36	-	0.44	-	0.55	V
I_I	input leakage current	$V_I = 5.5 \text{ V}$ or GND; $V_{CC} = 0 \text{ V}$ to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$; $V_{CC} = 5.5 \text{ V}$	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}$; other pins at V_{CC} or GND; $I_O = 0 \text{ A}$; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF
C_O	output capacitance		-	4	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
74AHC139										
t _{pd}	propagation delay	nAn to nȳn; see Figure 5	[2]							
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.5	11.0	1.0	13.0	1.0	14.0	ns
		C _L = 50 pF	-	7.9	14.5	1.0	16.5	1.0	18.5	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.9	7.2	1.0	8.5	1.0	9.0	ns
		C _L = 50 pF	-	5.6	9.2	1.0	10.5	1.0	11.5	ns
		nĒ to nȳn; see Figure 6	[2]							
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.8	9.2	1.0	11.0	1.0	11.5	ns
		C _L = 50 pF	-	6.9	12.7	1.0	14.5	1.0	16.0	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.4	6.3	1.0	7.5	1.0	8.0	ns
		C _L = 50 pF	-	4.9	8.3	1.0	9.5	1.0	10.5	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC}	[3]	-	26	-	-	-	-	pF
74AHCT139; V _{CC} = 4.5 V to 5.5 V										
t _{pd}	propagation delay	nAn to nȳn; see Figure 5	[2]							
		C _L = 15 pF	-	4.7	7.2	1.0	8.5	1.0	9.0	ns
		C _L = 50 pF	-	6.5	9.2	1.0	10.5	1.0	11.5	ns
		nĒ to nȳn; see Figure 6	[2]							
		C _L = 15 pF	-	3.6	6.3	1.0	7.5	1.0	8.0	ns
		C _L = 50 pF	-	5.2	8.3	1.0	9.5	1.0	10.5	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC}	[3]	-	23	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ($V_{CC} = 3.3 \text{ V}$ and $V_{CC} = 5.0 \text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

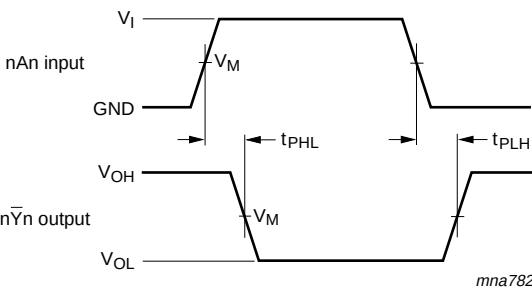
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

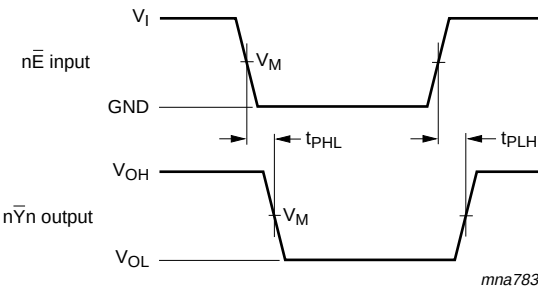
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Address input to output propagation delays

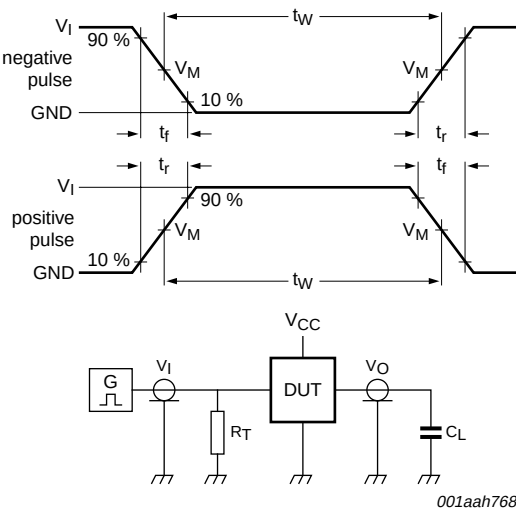


Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 6. Enable input to output propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC139	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT139	1.5 V	$0.5 \times V_{CC}$



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = load capacitance including jig and probe capacitance.

Fig 7. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC139	V_{CC}	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT139	3.0 V	$\leq 3.0 \text{ ns}$	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

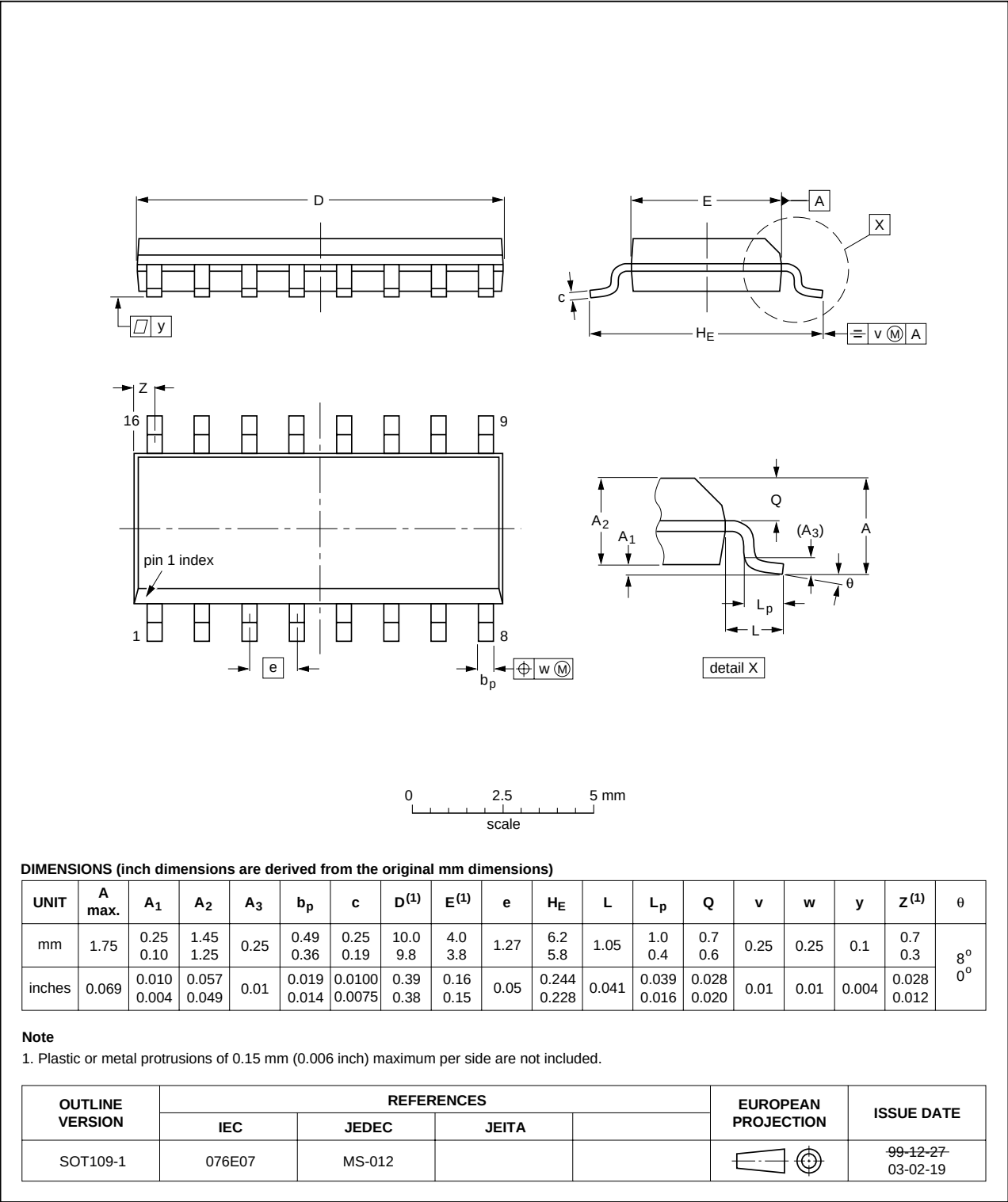


Fig 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

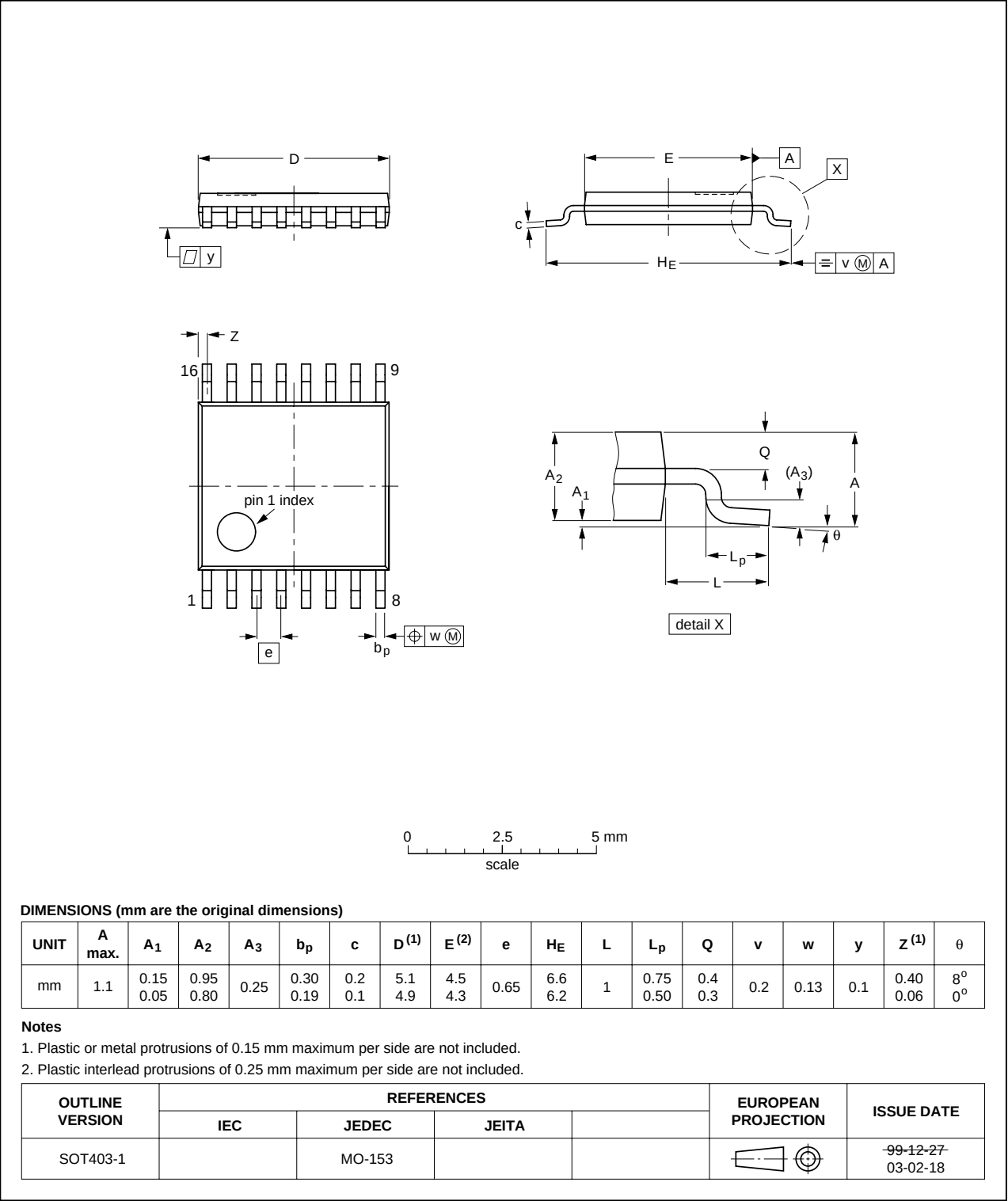


Fig 9. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT139_2	20080509	Product data sheet	-	74AHC_AHCT139_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: the conditions for input leakage current have been changed.			
74AHC_AHCT139_1	19990901	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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