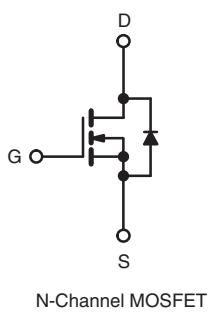
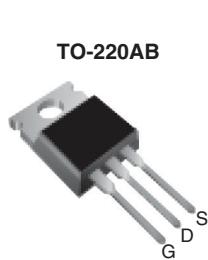


Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	50
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V 0.10
Q_g (Max.) (nC)	17
Q_{gs} (nC)	9.0
Q_{gd} (nC)	3.0
Configuration	Single



ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFZ20PbF SiHFZ20-E3
SnPb	IRFZ20 SiHFZ20

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage ^a	V_{DS}	50	V
Gate-Source Voltage ^a	V_{GS}	± 20	
Continuous Drain Current	I_D	15	A
		10	
	I_{DM}	60	
Pulsed Drain Current ^b	E_{AS}	5	mJ
Single Pulse Avalanche Energy ^c		0.32	W/°C
Linear Derating Factor (see fig. 16)		40	W
Maximum Power Dissipation (see fig. 16)	$T_C = 25$ °C	T_J, T_{stg}	- 55 to + 150
Operating Junction and Storage Temperature Range			°C
Soldering Recommendations (Peak Temperature)	for 10 s	300 (0.063" (1.6 mm) from case	

Notes

- a. $T_J = 25$ °C to 150 °C
- b. Repetitive rating: Pulse width limited by max. junction temperature. See transient temperature impedance curve (see fig. 11).
- c. Starting $T_J = 25$ °C, $L = 0.07$ mH, $R_g = 25$ Ω, $I_{AS} = 12$ A

* Pb containing terminations are not RoHS compliant, exemptions may apply



FEATURES

- Extremely Low $R_{DS(on)}$
- Compact Plastic Package
- Fast Switching
- Low Drive Current
- Ease of Parallelizing
- Excellent Temperature Stability
- Parts Per Million Quality
- Compliant to RoHS Directive 2002/95/EC

DESCRIPTION

The technology has expanded its product base to serve the low voltage, very low $R_{DS(on)}$ MOSFET transistor requirements. Vishay's highly efficient geometry and unique processing have been combined to create the lowest on resistance per device performance. In addition to this feature all have documented reliability and parts per million quality!

The transistor also offer all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of parallelizing, and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and in systems that are operated from low voltage batteries, such as automotive, portable equipment, etc.

THERMAL RESISTANCE RATINGS

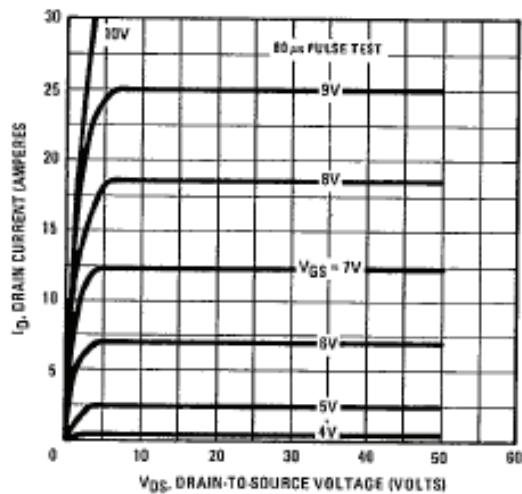
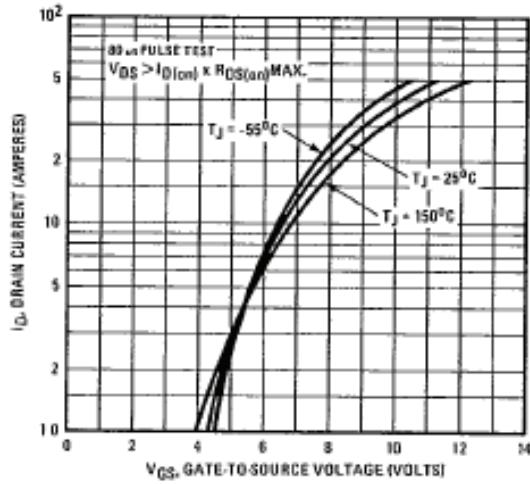
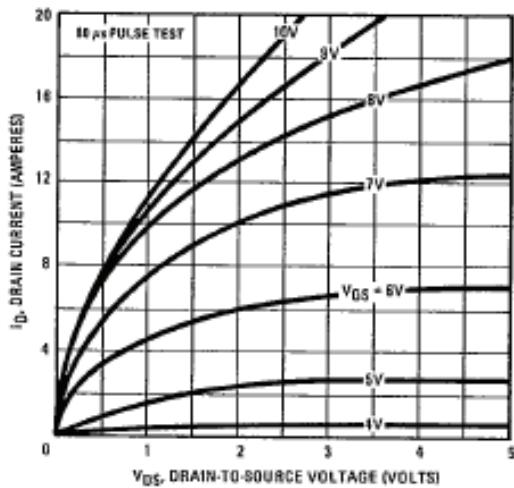
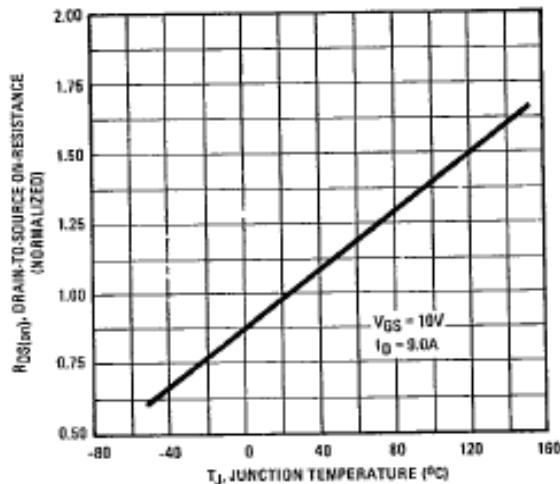
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Typical Socket Mount, Junction-to-Ambient	R_{thJA}	-	80	$^{\circ}\text{C}/\text{W}$
Case-to-Sink, Mounting Surface Flat, Smooth, and Greased	R_{thCS}	1.0	-	
Junction-to-Case	R_{thJC}	-	3.12	

ELECTRICAL CHARACTERISTICS ($T_J = 25 \text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	50	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$	-	-	± 500	nA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} > \text{Max. Rating}, V_{GS} = 0 \text{ V}$	-	-	250	μA	
		$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0 \text{ V}, T_C = 125 \text{ }^{\circ}\text{C}$	-	-	1000		
On-State Drain Current	$I_{D(on)}$	$V_{GS} = 10 \text{ V}$	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}$	-	-	A	
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 10 \text{ A}$	-	0.080	Ω	
Forward Transconductance ^b	g_{fs}	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, I_D = 9.0 \text{ A}$	5.0	6.0	-	S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1.0 \text{ MHz, see fig. 11}$	-	560	860	pF	
Output Capacitance	C_{oss}		-	250	350		
Reverse Transfer Capacitance	C_{rss}		-	60	100		
Total Gate Charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}, V_{DS} = 0.8 \text{ max. rating, see fig. 18 for test circuit (Gate charge is essentially independent of operating temperature)}$	-	12	17	nC
Gate-Source Charge	Q_{gs}			-	9.0	-	
Gate-Drain Charge	Q_{gd}			-	3.0	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 25 \text{ V}, I_D = 9.0 \text{ A}, Z_0 = 50 \Omega, \text{ see fig. 5}^b$	-	15	30	ns	
Rise Time	t_r		-	45	90		
Turn-Off Delay Time	$t_{d(off)}$		-	20	40		
Fall Time	t_f		-	15	30		
Internal Drain Inductance	L_D	Modified MOSFET symbol showing the internal device inductances	-	3.5	-	nH	
Internal Source Inductance	L_S		-	4.5	-		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction rectifier	-	-	15	A	
Pulsed Diode Forward Current ^a	I_{SM}		-	-	60		
Body Diode Voltage ^b	V_{SD}	$T_C = 25 \text{ }^{\circ}\text{C}, I_S = 15 \text{ A}, V_{GS} = 0 \text{ V}$	-	-	1.5	V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 150 \text{ }^{\circ}\text{C}, I_F = 15 \text{ A}, dI_F/dt = 100 \text{ A}/\mu\text{s}$	-	100	-	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.4	-	μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating: Pulse width limited by max. junction temperature. See transient temperature impedance curve (see fig. 5).
b. Pulse test: Pulse width $\leq 300 \mu\text{s}$; duty cycle $\leq 2 \%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Saturation Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

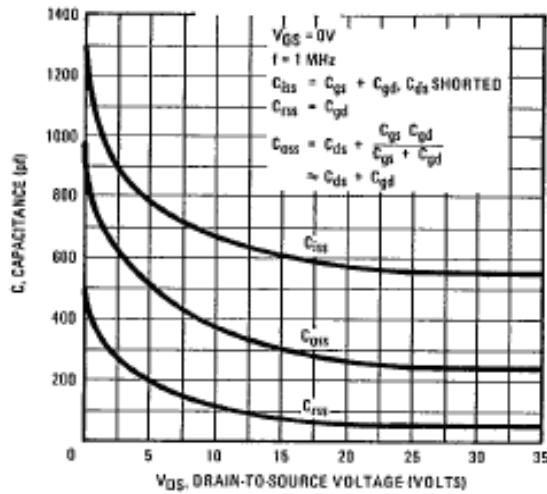


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

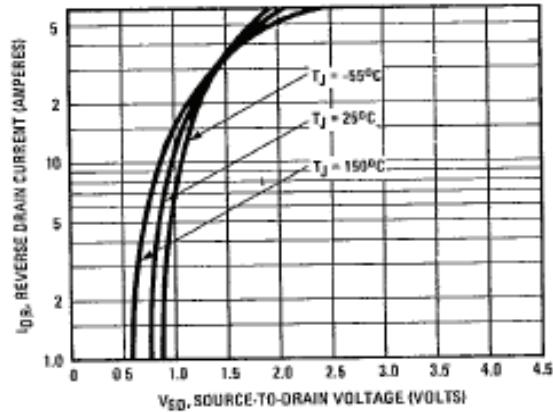


Fig. 7 - Typical Source-Drain Diode Forward Voltage

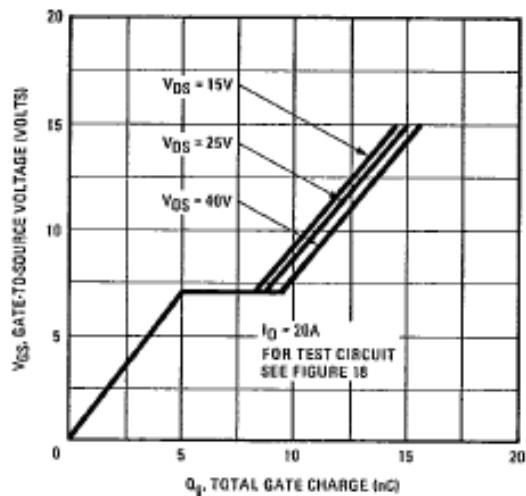


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

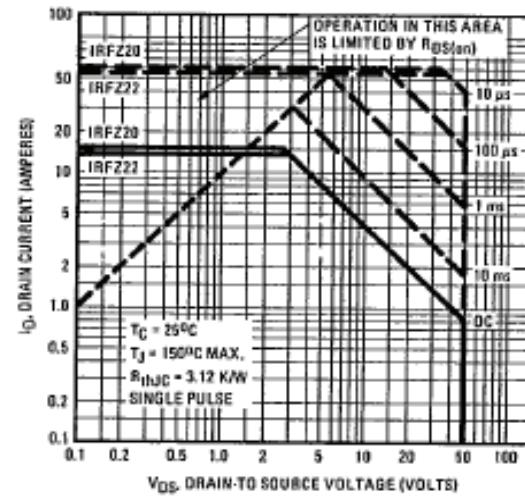


Fig. 8 - Maximum Safe Operating Area

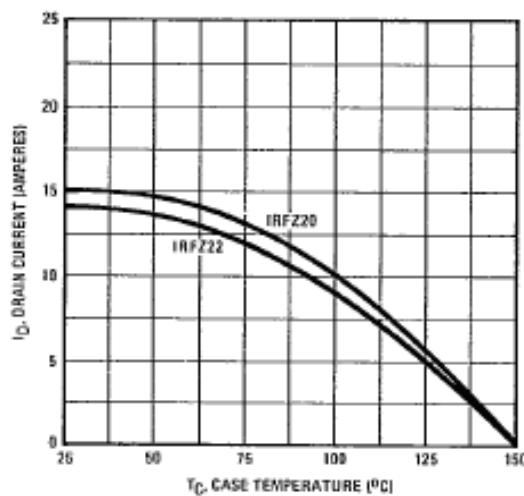


Fig. 9 - Maximum Drain Current vs. Case Temperature

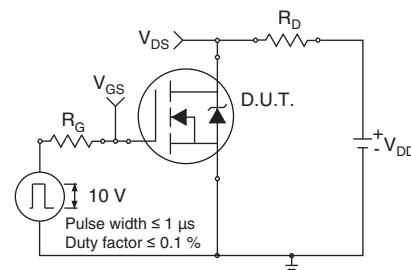


Fig. 10a - Switching Time Test Circuit

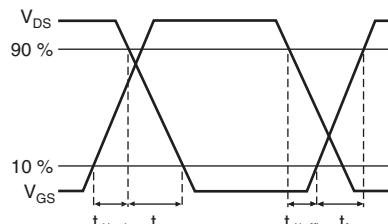


Fig. 10b - Switching Time Waveforms

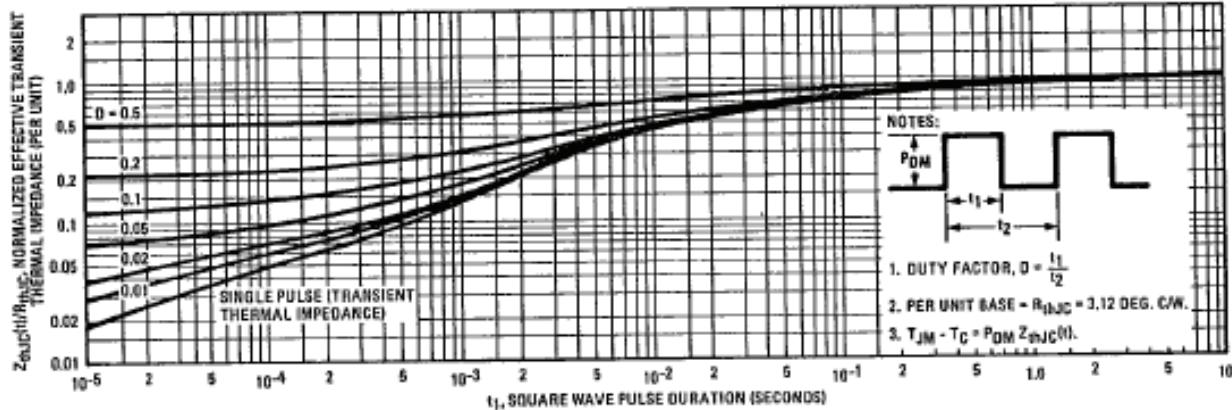


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

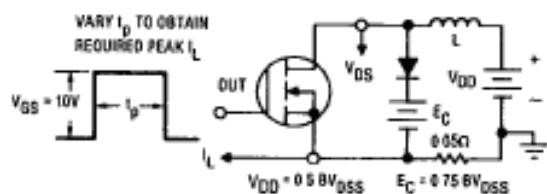


Fig. 12a - Clamped Inductive Test Circuit

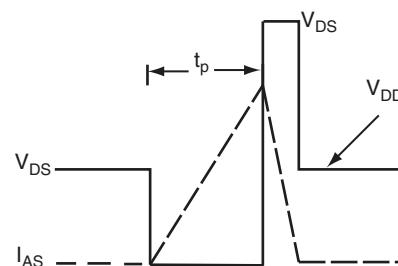


Fig. 12b - Unclamped Inductive Waveforms

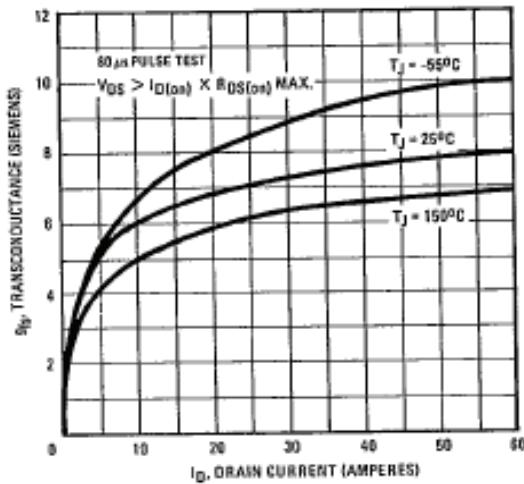


Fig. 13 - Typical Transconductance vs. Drain Current

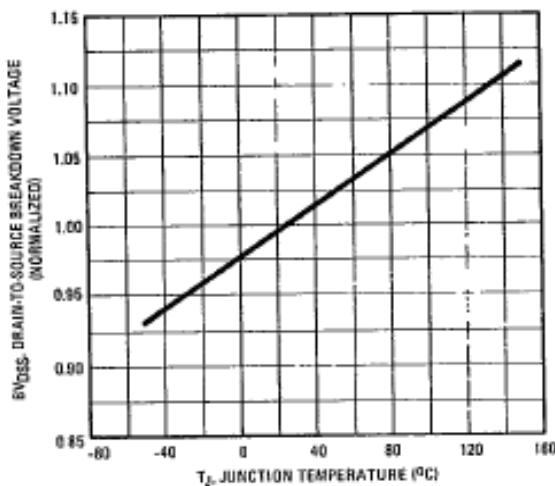


Fig. 14 - Breakdown Voltage vs. Temperature

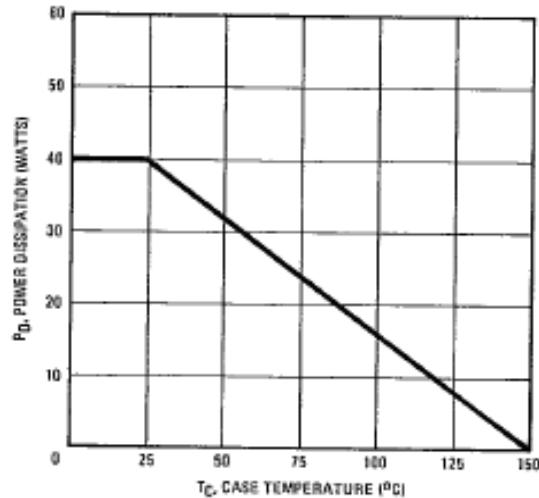


Fig. 16 - Power vs. Temperature Derating Curve

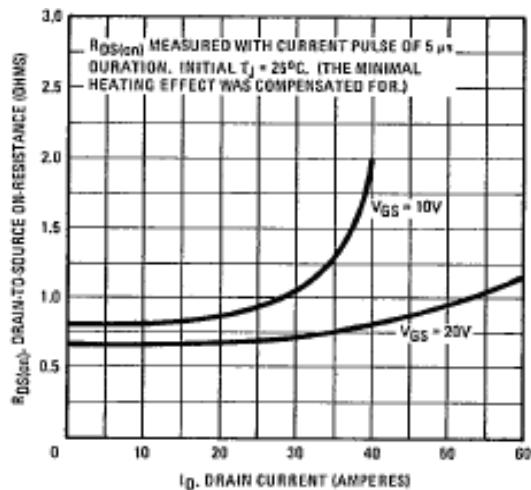


Fig. 15 - Typical On-Resistance vs. Drain Current

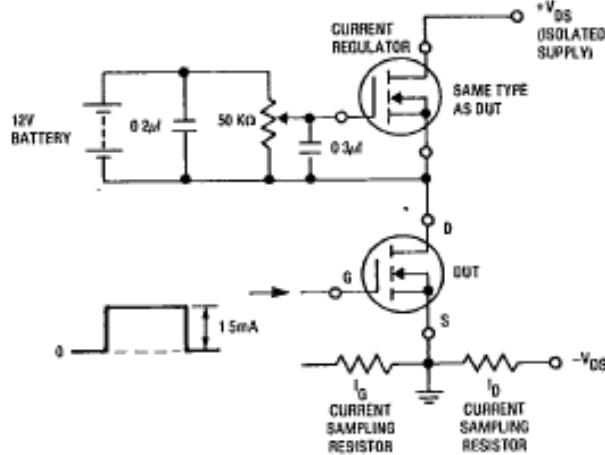
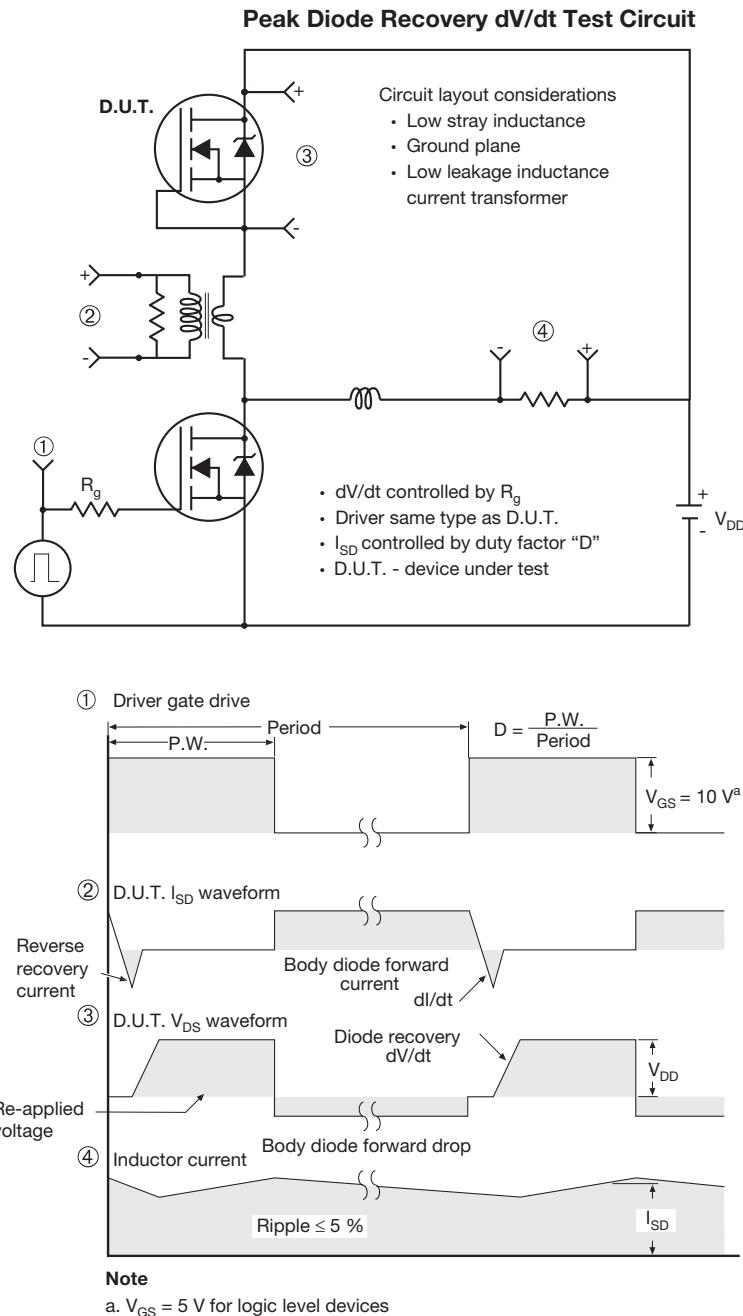


Fig. 17 - Gate Charge Test Circuit


Fig. 14 - For N-Channel

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- Подбор аналогов;
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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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