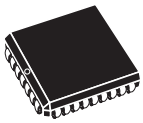
M50FW080

8-Mbit (1 Mb ×8, Uniform Block) 3-V supply, Firmware Hub Flash memory

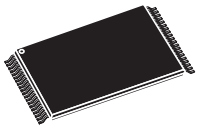
Feature summary

- Supply voltage
  - V_{CC} = 3 V to 3.6 V for Program, Erase and Read operations
  - V_{PP} = 12 V for fast program and fast erase (optional)
- Two interfaces
  - Firmware Hub (FWH) Interface for embedded operation with PC Chipsets
  - Address/Address Multiplexed (A/A Mux) Interface for programming equipment compatibility
- Firmware hub (FWH) hardware interface mode
  - 5 signal communication interface supporting Read and Write operations
  - Hardware Write Protect pins for block protection
  - Register-based Read and Write Protection
  - 5 additional general-purpose inputs for platform design flexibility
  - Synchronized with 33 MHz PCI clock
- Programming time
  - 10 µs typical
  - Quadruple Byte Programming option
- 16 uniform 64 Kbyte memory blocks
- Program/Erase Controller
  - Embedded Byte Program and Block/Chip Erase algorithms
  - Status Register bits
- Program and Erase Suspend
  - Read other Blocks during Program/Erase Suspend
  - Program other Blocks during Erase Suspend
- For use in PC BIOS applications



PLCC32 (K)

TSOP32 (NB)
8 x 14mm



TSOP40 (N)
10 x 20mm

- Electronic signature
  - Manufacturer code: 20h
  - Device Code: 2Dh
- Packages
  - ECOPACK® (RoHS compliant)

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1 Summary description

The M50FW080 is an 8 Mbit (1Mbit x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (3.0 to 3.6V) supply. For fast programming and fast erasing in production lines an optional 12V power supply can be used to reduce the programming and the erasing times.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Blocks can be protected individually to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Two different bus interfaces are supported by the memory. The primary interface, the Firmware Hub (or FWH) Interface, uses Intel's proprietary FWH protocol. This has been designed to remove the need for the ISA bus in current PC Chipsets; the M50FW080 acts as the PC BIOS on the Low Pin Count bus for these PC Chipsets.

The secondary interface, the Address/Address Multiplexed (or A/A Mux) Interface, is designed to be compatible with current Flash Programmers for production line programming prior to fitting to a PC Motherboard.

In order to meet environmental requirements, ST offers the M50FW080 in ECOPACK® packages. ECOPACK® packages are Lead-free and RoHS compliant. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram (FWH interface)

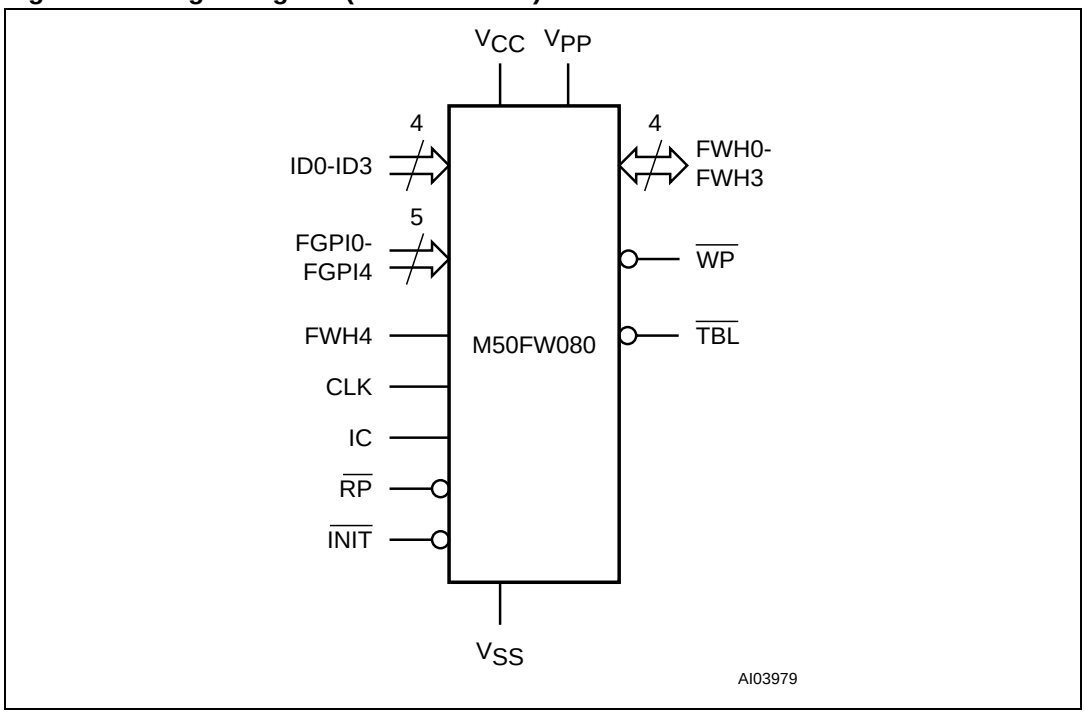


Table 1. Signal names (FWH Interface)

FWH0-FWH3	Input/Output Communications
FWH4	Input Communication Frame
ID0-ID3	Identification Inputs
FGPI0-FGPI4	General Purpose Inputs
IC	Interface Configuration
$\overline{RP}$	Interface Reset
$\overline{INIT}$	CPU Reset
CLK	Clock
$\overline{TBL}$	Top Block Lock
$\overline{WP}$	Write Protect
RFU	Reserved for Future Use. Leave disconnected
V_{CC}	Supply Voltage
V_{PP}	Optional Supply Voltage for Fast Erase Operations
V_{SS}	Ground
NC	Not Connected Internally

Figure 2. Logic diagram (A/A Mux interface)

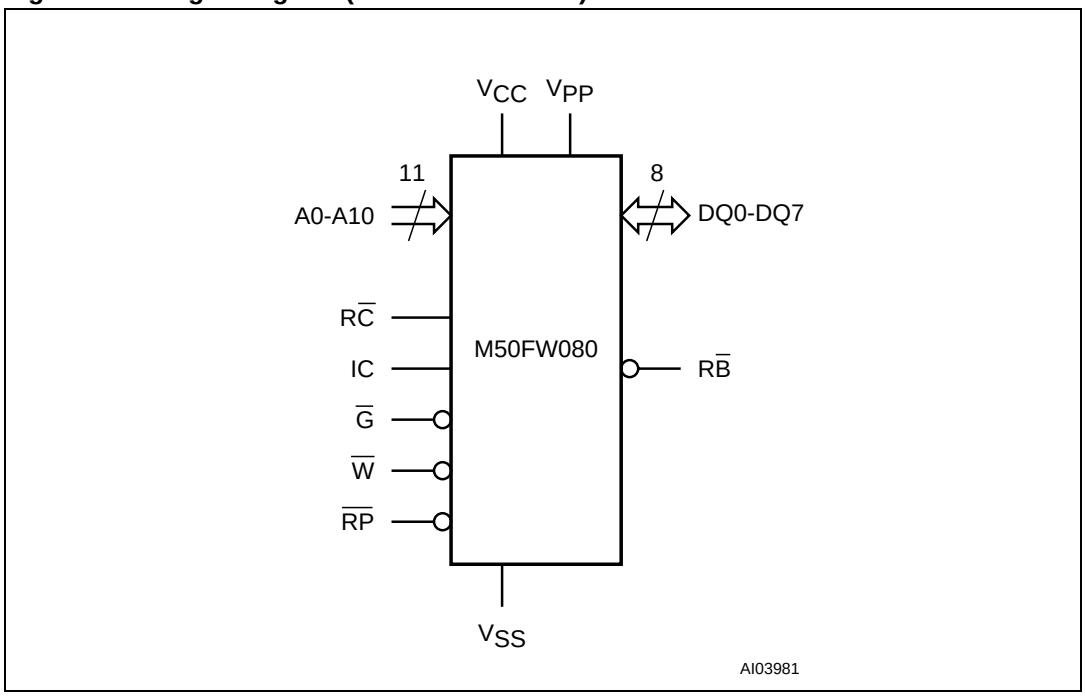
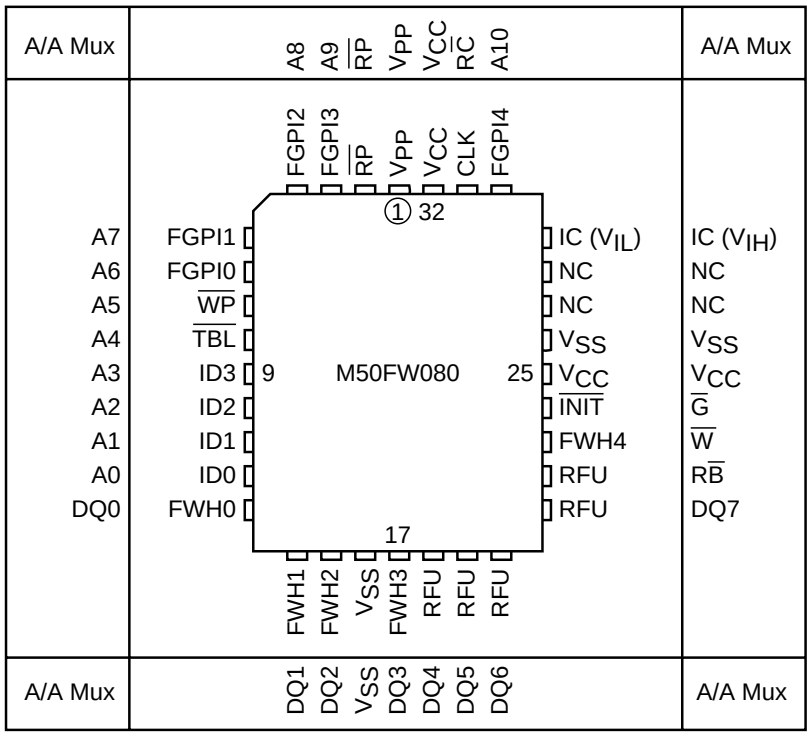


Table 2. Signal names (A/A Mux Interface)

IC	Interface Configuration
A0-A10	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
R$\overline{C}$	Row/Column Address Select
R$\overline{B}$	Ready/Busy Output
$\overline{RP}$	Interface Reset
V_{CC}	Supply Voltage
V_{PP}	Optional Supply Voltage for Fast Program and Fast Erase Operations
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. PLCC connections



1. Pins 27 and 28 are not internally connected.

Figure 4. TSOP32 connections

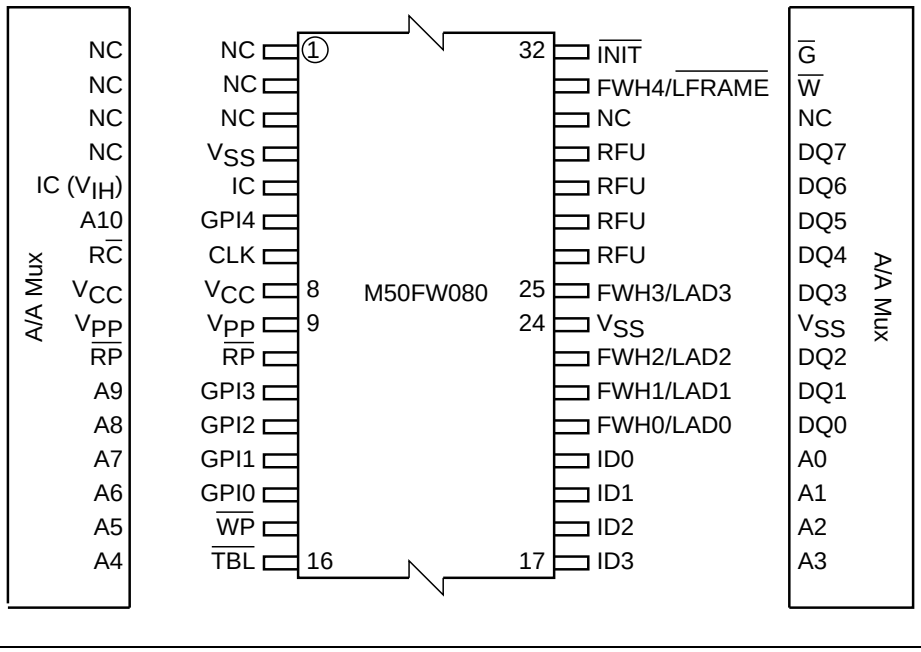
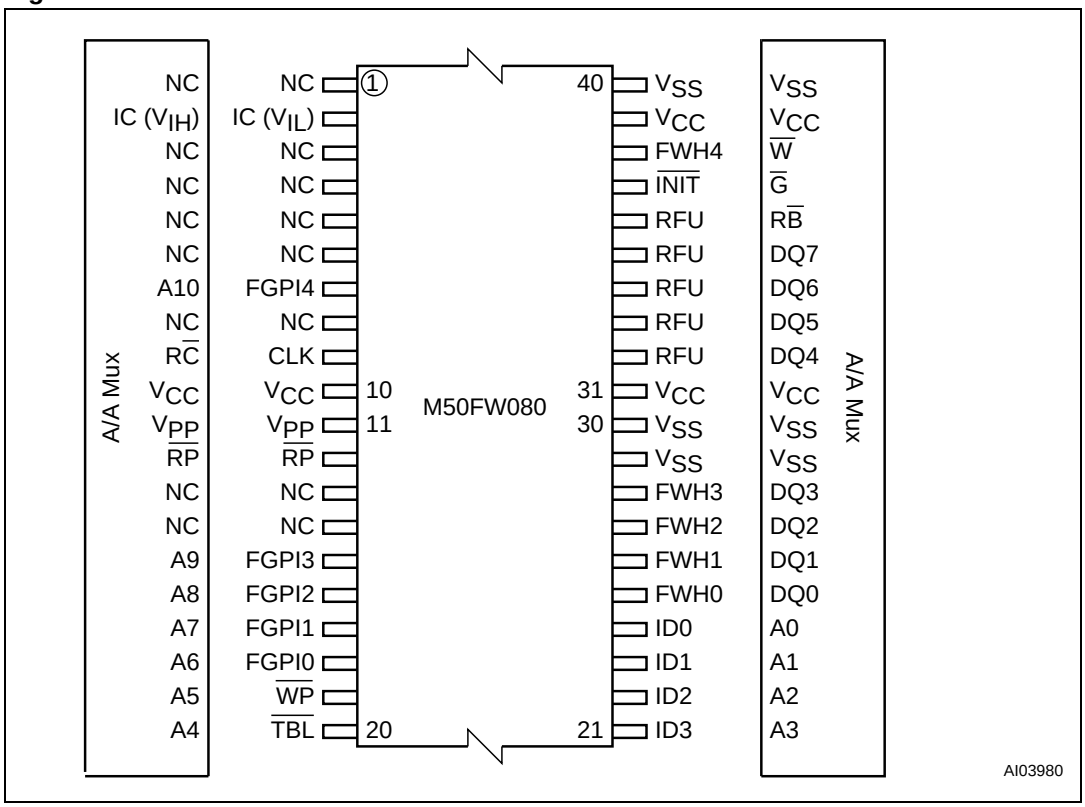


Figure 5. TSOP40 connections



2 Signal descriptions

There are two distinct bus interfaces available on this device. The active interface is selected before power-up, or during Reset, using the Interface Configuration Pin, IC.

The signals for each interface are discussed in the *Firmware Hub (FWH) signal descriptions* section and the *Address/Address Multiplexed (A/A Mux) signal descriptions* section, respectively, while the supply signals are discussed in the *Supply signal descriptions* section.

2.1 Firmware Hub (FWH) signal descriptions

For the Firmware Hub (FWH) Interface see *Figure 1* and *Table 1*.

2.1.1 Input/Output communications (FWH0-FWH3)

All Input and Output Communication with the memory take place on these pins. Addresses and Data for Bus Read and Bus Write operations are encoded on these pins.

2.1.2 Input communication frame (FWH4)

The Input Communication Frame (FWH4) signals the start of a bus operation. When Input Communication Frame is Low, V_{IL}, on the rising edge of the Clock a new bus operation is initiated. If Input Communication Frame is Low, V_{IL}, during a bus operation then the operation is aborted. When Input Communication Frame is High, V_{IH}, the current bus operation is proceeding or the bus is idle.

2.1.3 Identification inputs (ID0-ID3)

The Identification Inputs select the address that the memory responds to. Up to 16 memories can be addressed on a bus. For an address bit to be ‘0’ the pin can be left floating or driven Low, V_{IL}; an internal pull-down resistor is included with a value of R_{IL}. For an address bit to be ‘1’ the pin must be driven High, V_{IH}; there will be a leakage current of I_{LI2} through each pin when pulled to V_{IH}; see *Table 20*.

By convention the boot memory must have address ‘0000’ and all additional memories take sequential addresses starting from ‘0001’.

2.1.4 General-purpose inputs (FGPI0-FGPI4)

The General Purpose Inputs can be used as digital inputs for the CPU to read. The General Purpose Input Register holds the values on these pins. The pins must have stable data from before the start of the cycle that reads the General Purpose Input Register until after the cycle is complete. These pins must not be left to float, they should be driven Low, $V_{IL,}$ or High, V_{IH}.

2.1.5 Interface configuration (IC)

The Interface Configuration input selects whether the Firmware Hub (FWH) or the Address/Address Multiplexed (A/A Mux) Interface is used. The chosen interface must be selected before power-up or during a Reset and, thereafter, cannot be changed. The state of the Interface Configuration, IC, should not be changed during operation.

To select the Firmware Hub (FWH) Interface the Interface Configuration pin should be left to float or driven Low, V_{IL}; to select the Address/Address Multiplexed (A/A Mux) Interface the pin should be driven High, V_{IH}. An internal pull-down resistor is included with a value of R_{IL}; there will be a leakage current of I_{LI2} through each pin when pulled to V_{IH}; see *Table 20*.

2.1.6 Interface Reset ($\overline{RP}$)

The Interface Reset ($\overline{RP}$) input is used to reset the memory. When Interface Reset ($\overline{RP}$) is set Low, V_{IL}, the memory is in Reset mode: the outputs are put to high impedance and the current consumption is minimized. When $\overline{RP}$ is set High, V_{IH}, the memory is in normal operation. After exiting Reset mode, the memory enters Read mode.

2.1.7 CPU Reset ($\overline{INIT}$)

The CPU Reset, $\overline{INIT}$, pin is used to Reset the memory when the CPU is reset. It behaves identically to Interface Reset, $\overline{RP}$, and the internal Reset line is the logical OR (electrical AND) of $\overline{RP}$ and $\overline{INIT}$.

2.1.8 Clock (CLK)

The Clock, CLK, input is used to clock the signals in and out of the Input/Output Communication Pins, FWH0-FWH3. The Clock conforms to the PCI specification.

2.1.9 Top Block Lock ($\overline{TBL}$)

The Top Block Lock input is used to prevent the Top Block (Block 15) from being changed. When Top Block Lock, $\overline{TBL}$, is set Low, V_{IL}, Program and Block Erase operations in the Top Block have no effect, regardless of the state of the Lock Register. When Top Block Lock, $\overline{TBL}$, is set High, V_{IH}, the protection of the Block is determined by the Lock Register. The state of Top Block Lock, $\overline{TBL}$, does not affect the protection of the Main Blocks (Blocks 0 to 14).

Top Block Lock, $\overline{TBL}$, must be set prior to a Program or Block Erase operation is initiated and must not be changed until the operation completes or unpredictable results may occur. Care should be taken to avoid unpredictable behavior by changing $\overline{TBL}$ during Program or Erase Suspend.

2.1.10 Write Protect ($\overline{WP}$)

The Write Protect input is used to prevent the Main Blocks (Blocks 0 to 14) from being changed. When Write Protect, $\overline{WP}$, is set Low, V_{IL}, Program and Block Erase operations in the Main Blocks have no effect, regardless of the state of the Lock Register. When Write Protect, $\overline{WP}$, is set High, V_{IH}, the protection of the Block determined by the Lock Register. The state of Write Protect, $\overline{WP}$, does not affect the protection of the Top Block (Block 15).

Write Protect, $\overline{WP}$, must be set prior to a Program or Block Erase operation is initiated and must not be changed until the operation completes or unpredictable results may occur. Care should be taken to avoid unpredictable behavior by changing $\overline{WP}$ during Program or Erase Suspend.

2.1.11 Reserved for Future Use (RFU)

These pins do not have assigned functions in this revision of the part. They must be left disconnected.

Table 3. Block addresses

Size (Kbytes)	Address Range	Block Number	Block Type
64	F0000h-FFFFFh	15	Top Block
64	E0000h-EFFFFh	14	Main Block
64	D0000h-DFFFFh	13	Main Block
64	C0000h-CFFFFh	12	Main Block
64	B0000h-BFFFFh	11	Main Block
64	A0000h-AFFFFh	10	Main Block
64	90000h-9FFFFh	9	Main Block
64	80000h-8FFFFh	8	Main Block
64	70000h-7FFFFh	7	Main Block
64	60000h-6FFFFh	6	Main Block
64	50000h-5FFFFh	5	Main Block
64	40000h-4FFFFh	4	Main Block
64	30000h-3FFFFh	3	Main Block
64	20000h-2FFFFh	2	Main Block
64	10000h-1FFFFh	1	Main Block
64	00000h-0FFFFh	0	Main Block

2.2 Address/Address Multiplexed (A/A Mux) signal descriptions

For the Address/Address Multiplexed (A/A Mux) Interface see *Figure 2* and *Table 2*.

2.2.1 Address inputs (A0-A10)

The Address Inputs are used to set the Row Address bits (A0-A10) and the Column Address bits (A11-A19). They are latched during any bus operation by the Row/Column Address Select input, $R\overline{C}$.

2.2.2 Data inputs/outputs (DQ0-DQ7)

The Data Inputs/Outputs hold the data that is written to or read from the memory. They output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. The Data Inputs/Outputs, DQ0-DQ7, are latched during a Bus Write operation.

2.2.3 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

2.2.4 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

2.2.5 Row/Column Address Select ($R\overline{C}$)

The Row/Column Address Select input selects whether the Address Inputs should be latched into the Row Address bits (A0-A10) or the Column Address bits (A11-A19). The Row Address bits are latched on the falling edge of $R\overline{C}$ whereas the Column Address bits are latched on the rising edge.

2.2.6 Ready/Busy Output ($R\overline{B}$)

The Ready/Busy pin gives the status of the memory's Program/Erase Controller. When Ready/Busy is Low, V_{OL}, the memory is busy with a Program or Erase operation and it will not accept any additional Program or Erase command except the Program/Erase Suspend command. When Ready/Busy is High, V_{OH}, the memory is ready for any Read, Program or Erase operation.

2.3 Supply signal descriptions

The Supply Signals are the same for both interfaces.

2.3.1 V_{CC} supply voltage

The V_{CC} Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid. After V_{CC} becomes valid the Command Interface is reset to Read mode.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pins and the V_{SS} Ground pin to decouple the current surges from the power supply. Both V_{CC} Supply Voltage pins must be connected to the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

2.3.2 V_{PP} optional supply voltage

The V_{PP} Optional Supply Voltage pin is used to select the Fast Program (see the Quadruple Byte Program Command description) and Fast Erase options of the memory and to protect the memory. When $V_{PP} < V_{PPLK}$ Program and Erase operations cannot be performed and an error is reported in the Status Register if an attempt to change the memory contents is made. When $V_{PP} = V_{CC}$ Program and Erase operations take place as normal. When $V_{PP} = V_{PPH}$ Fast Program (if A/A Mux interface is selected) and Fast Erase operations are used. Any other voltage input to V_{PP} will result in undefined behavior and should not be used.

V_{PP} should not be set to V_{PPH} for more than 80 hours during the life of the memory.

2.3.3 V_{SS} ground

V_{SS} is the reference for all the voltage measurements.

3 Bus operations

The two interfaces have similar bus operations but the signals and timings are completely different. The Firmware Hub (FWH) Interface is the usual interface and all of the functionality of the part is available through this interface. Only a subset of functions are available through the Address/Address Multiplexed (A/A Mux) Interface.

See the sections: The *Firmware Hub (FWH) bus operations* and *Address/Address Multiplexed (A/A Mux) bus operations*, for details of the bus operations on each interface.

3.1 Firmware Hub (FWH) bus operations

The Firmware Hub (FWH) Interface consists of four data signals (FWH0-FWH3), one control line (FWH4) and a clock (CLK). In addition protection against accidental or malicious data corruption can be achieved using two further signals ($\overline{TBL}$ and $\overline{WP}$). Finally two reset signals ($\overline{RP}$ and $\overline{INIT}$) are available to put the memory into a known state.

The data signals, control signal and clock are designed to be compatible with PCI electrical specifications. The interface operates with clock speeds up to 33MHz.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Standby, Reset and Block Protection.

3.1.1 Bus Read

Bus Read operations read from the memory cells, specific registers in the Command Interface or Firmware Hub Registers. A valid Bus Read operation starts when Input Communication Frame, FWH4, is Low, V_{IL}, as Clock rises and the correct Start cycle is on FWH0-FWH3. On the following clock cycles the Host will send the Memory ID Select, Address and other control bits on FWH0-FWH3. The memory responds by outputting Sync data until the wait-states have elapsed followed by Data0-Data3 and Data4-Data7.

See *Table 4* and *Figure 6*, for a description of the Field definitions for each clock cycle of the transfer. See *Table 22* and *Figure 11*, for details on the timings of the signals.

3.1.2 Bus Write

Bus Write operations write to the Command Interface or Firmware Hub Registers. A valid Bus Write operation starts when Input Communication Frame, FWH4, is Low, V_{IL}, as Clock rises and the correct Start cycle is on FWH0-FWH3. On the following Clock cycles the Host will send the Memory ID Select, Address, other control bits, Data0-Data3 and Data4-Data7 on FWH0-FWH3. The memory outputs Sync data until the wait-states have elapsed.

See *Table 5* and *Figure 7*, for a description of the Field definitions for each clock cycle of the transfer. See *Table 22* and *Figure 11*, for details on the timings of the signals.

3.1.3 Bus Abort

The Bus Abort operation can be used to immediately abort the current bus operation. A Bus Abort occurs when FWH4 is driven Low, V_{IL}, during the bus operation; the memory will tri-state the Input/Output Communication pins, FWH0-FWH3.

Note that, during a Bus Write operation, the Command Interface starts executing the command as soon as the data is fully received; a Bus Abort during the final TAR cycles is not guaranteed to abort the command; the bus, however, will be released immediately.

3.1.4 Standby

When FWH4 is High, V_{IH}, the memory is put into Standby mode where FWH0-FWH3 are put into a high-impedance state and the Supply Current is reduced to the Standby level, I_{CC1}.

3.1.5 Reset

During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high-impedance. The memory is in Reset mode when Interface Reset, $\overline{RP}$, or CPU Reset, $\overline{INIT}$, is Low, V_{IL}. $\overline{RP}$ or $\overline{INIT}$ must be held Low, V_{IL}, for t_{PLPH}. The memory resets to Read mode upon return from Reset mode and the Lock Registers return to their default states regardless of their state before Reset, see *Table 14*. If $\overline{RP}$ or $\overline{INIT}$ goes Low, V_{IL}, during a Program or Erase operation, the operation is aborted and the memory cells affected no longer contain valid data; the memory can take up to t_{PLRH} to abort a Program or Erase operation.

3.1.6 Block Protection

Block Protection can be forced using the signals Top Block Lock, $\overline{TBL}$, and Write Protect, $\overline{WP}$, regardless of the state of the Lock Registers.

3.2 Address/Address Multiplexed (A/A Mux) bus operations

The Address/Address Multiplexed (A/A Mux) Interface has a more traditional style interface. The signals consist of a multiplexed address signals (A0-A10), data signals, (DQ0-DQ7) and three control signals ($\overline{RC}$, $\overline{G}$, $\overline{W}$). An additional signal, $\overline{RP}$, can be used to reset the memory.

The Address/Address Multiplexed (A/A Mux) Interface is included for use by Flash Programming equipment for faster factory programming. Only a subset of the features available to the Firmware Hub (FWH) Interface are available; these include all the Commands but exclude the Security features and other registers.

The following operations can be performed using the appropriate bus cycles: Bus Read, Bus Write, Output Disable and Reset.

When the Address/Address Multiplexed (A/A Mux) Interface is selected all the blocks are unprotected. It is not possible to protect any blocks through this interface.

3.2.1 Bus Read

Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature and the Status Register. A valid Bus Read operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select $\overline{RC}$. Then Write Enable ($\overline{W}$) and Interface Reset ($\overline{RP}$) must be High, V_{IH}, and Output Enable, $\overline{G}$, Low, V_{IL}, in order to perform a Bus Read operation. The Data Inputs/Outputs will output the value, see *Figure 13* and *Table 24*, for details of when the output becomes valid.

3.2.2 Bus Write

Bus Write operations write to the Command Interface. A valid Bus Write operation begins by latching the Row Address and Column Address signals into the memory using the Address Inputs, A0-A10, and the Row/Column Address Select $\overline{RC}$. The data should be set up on the Data Inputs/Outputs; Output Enable, $\overline{G}$, and Interface Reset, $\overline{RP}$, must be High, V_{IH} and Write Enable, $\overline{W}$, must be Low, V_{IL}. The Data Inputs/Outputs are latched on the rising edge of Write Enable, $\overline{W}$. See *Figure 14* and *Table 25*, for details of the timing requirements.

3.2.3 Output Disable

The data outputs are high-impedance when the Output Enable, $\overline{G}$, is at V_{IH}.

3.2.4 Reset

During Reset mode all internal circuits are switched off, the memory is deselected and the outputs are put in high-impedance. The memory is in Reset mode when $\overline{RP}$ is Low, V_{IL}. $\overline{RP}$ must be held Low, V_{IL} for t_{PLPH}. If $\overline{RP}$ is goes Low, V_{IL}, during a Program or Erase operation, the operation is aborted and the memory cells affected no longer contain valid data; the memory can take up to t_{PLRH} to abort a Program or Erase operation.

Table 4. FWH Bus Read field definitions

Clock Cycle Number	Clock Cycle Count	Field	FWH0-FWH3	Memory I/O	Description
1	1	START	1101b	I	On the rising edge of CLK with FWH4 Low, the contents of FWH0-FWH3 indicate the start of a FWH Read cycle.
2	1	IDSEL	XXXX	I	Indicates which FWH Flash Memory is selected. The value on FWH0-FWH3 is compared to the IDSEL strapping on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed.
3-9	7	ADDR	XXXX	I	A 28-bit address phase is transferred starting with the most significant nibble first.
10	1	MSIZE	0000b	I	Always 0000b (only single byte transfers are supported).
11	1	TAR	1111b	I	The host drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
12	1	TAR	1111b (float)	O	The FWH Flash Memory takes control of FWH0-FWH3 during this cycle.
13-14	2	WSYNC	0101b	O	The FWH Flash Memory drives FWH0-FWH3 to 0101b (short wait-sync) for two clock cycles, indicating that the data is not yet available. Two wait-states are always included.
15	1	RSYNC	0000b	O	The FWH Flash Memory drives FWH0-FWH3 to 0000b, indicating that data will be available during the next clock cycle.
16-17	2	DATA	XXXX	O	Data transfer is two CLK cycles, starting with the least significant nibble.
18	1	TAR	1111b	O	The FWH Flash Memory drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
19	1	TAR	1111b (float)	N/A	The FWH Flash Memory floats its outputs, the host takes control of FWH0-FWH3.

Figure 6. FWH Bus Read waveforms

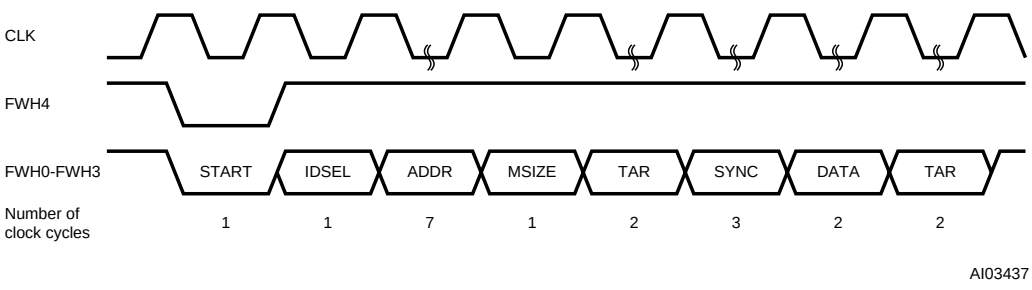


Table 5. FWH Bus Write field definitions

Clock Cycle Number	Clock Cycle Count	Field	FWH0-FWH3	Memory I/O	Description
1	1	START	1110b	I	On the rising edge of CLK with FWH4 Low, the contents of FWH0-FWH3 indicate the start of a FWH Write Cycle.
2	1	IDSEL	XXXX	I	Indicates which FWH Flash Memory is selected. The value on FWH0-FWH3 is compared to the IDSEL strapping on the FWH Flash Memory pins to select which FWH Flash Memory is being addressed.
3-9	7	ADDR	XXXX	I	A 28-bit address phase is transferred starting with the most significant nibble first.
10	1	MSIZE	0000b	I	Always 0000b (single byte transfer).
11-12	2	DATA	XXXX	I	Data transfer is two cycles, starting with the least significant nibble.
13	1	TAR	1111b	I	The host drives FWH0-FWH3 to 1111b to indicate a turnaround cycle.
14	1	TAR	1111b (float)	O	The FWH Flash Memory takes control of FWH0-FWH3 during this cycle.
15	1	SYNC	0000b	O	The FWH Flash Memory drives FWH0-FWH3 to 0000b, indicating it has received data or a command.
16	1	TAR	1111b	O	The FWH Flash Memory drives FWH0-FWH3 to 1111b, indicating a turnaround cycle.
17	1	TAR	1111b (float)	N/A	The FWH Flash Memory floats its outputs and the host takes control of FWH0-FWH3.

Figure 7. FWH Bus Write waveforms

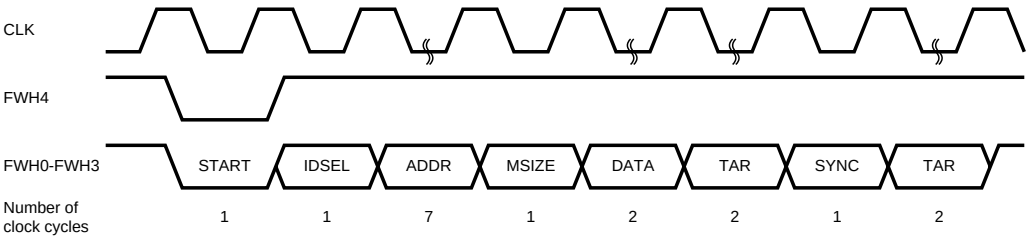


Table 6. A/A Mux bus operations

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	V_{PP}	DQ7-DQ0
Bus Read	V_{IL}	V_{IH}	V_{IH}	Don't Care	Data Output
Bus Write	V_{IH}	V_{IL}	V_{IH}	V_{CC} or V_{PPH}	Data Input
Output Disable	V_{IH}	V_{IH}	V_{IH}	Don't Care	Hi-Z
Reset	V_{IL} or V_{IH}	V_{IL} or V_{IH}	V_{IL}	Don't Care	Hi-Z

Table 7. Manufacturer and device codes

Operation	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A19-A1	A0	DQ7-DQ0
Manufacturer Code	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	20h
Device Code	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	2Dh

4 Command interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations.

After power-up or a Reset operation the memory enters Read mode.

The commands are summarized in *Table 9*, Commands. The following text descriptions should be read in conjunction with *Table 9*.

4.1 Read Memory Array command

The Read Memory Array command returns the memory to its Read mode where it behaves like a ROM or EPROM. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read operations will access the memory array.

While the Program/Erase Controller is executing a Program or Erase operation the memory will not accept the Read Memory Array command until the operation completes.

4.2 Read Status Register command

The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued. See the section on the Status Register for details on the definitions of the Status Register bits.

4.3 Read Electronic Signature command

The Read Electronic Signature command is used to read the Manufacturer Code and the Device Code. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code or the Device Code until another command is issued.

After the Read Electronic Signature Command is issued the Manufacturer Code and Device Code can be read using Bus Read operations using the addresses in *Table 8*.

Table 8. Read Electronic Signature

Code	Address	Data
Manufacturer Code	00000h	20h
Device Code	00001h	2Dh

4.4 Program command

The Program command can be used to program a value to one address in the memory array at a time. Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the address and data in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

If the address falls in a protected block then the Program operation will abort, the data in the memory array will not be changed and the Status Register will output the error.

During the Program operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Program times are given in *Table 14*.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so will not cause any modification on its value. One of the Erase commands must be used to set all of the bits in the block to '1'.

See *Figure 18*, for a suggested flowchart on using the Program command.

4.5 Quadruple Byte Program command

The Qua-druple Byte Program Command can be only used in A/A Mux mode to program four adjacent bytes in the memory array at a time. The four bytes must differ only for the addresses A0 and A10. Programming should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH}, but result could be uncertain. Five Bus Write operations are required to issue the command. The second, the third and the fourth Bus Write cycle latches respectively the address and data of the first, the second and the third byte in the internal state machine. The fifth Bus Write cycle latches the address and data of the fourth byte in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Quadruple Byte Program operation the memory will only accept the Read Status register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Quadruple Byte Program times are given in *Table 8*.

Note that the Quadruple Byte Program command cannot change a bit set to '0' back to '1' and attempting to do so will not cause any modification on its value. One of the Erase commands must be used to set all of the bits in the block to '1'.

See *Figure 19*, Quadruple Byte Program Flowchart and Pseudo Code, for a suggested flowchart on using the Quadruple Byte Program command.

4.6 Chip Erase command

The Chip Erase Command can be only used in A/A Mux mode to erase the entire chip at a time. Erasing should not be attempted when V_{PP} is not at V_{PPH}. The operation can also be executed if V_{PP} is below V_{PPH}, but result could be uncertain. Two Bus Write operations are required to issue the command and start the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits. During the Chip Erase operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Chip Erase times are given in *Table 14*. The Chip Erase command sets all of the bits in the memory to '1'. See *Figure 21*, for a suggested flowchart on using the Chip Erase command.

4.7 Block Erase command

The Block Erase command can be used to erase a block. Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

If the block is protected then the Block Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

During the Block Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Block Erase times are given in *Table 14*.

The Block Erase command sets all of the bits in the block to '1'. All previous data in the block is lost.

See *Figure 21*, for a suggested flowchart on using the Erase command.

4.8 Clear Status Register command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. Once the command is issued the memory returns to its previous mode, subsequent Bus Read operations continue to output the same data.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Program or Erase command is issued. If an error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program or Erase command.

4.9 Program/Erase Suspend command

The Program/Erase Suspend command can be used to pause a Program or Block Erase operation. One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once Program/Erase Controller Status bit indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit or the Erase Suspend Status bit can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see *Table 14*.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Block Erase then the Program command will also be accepted; only the blocks not being erased may be read or programmed correctly.

See *Figure 20*, and *Figure 23*, for suggested flowcharts on using the Program/Erase Suspend command.

4.10 Program/Erase Resume command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Table 9. Commands(1)

Command	Cycles	Bus Write operations									
		1st		2nd		3rd		4th		5th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read Memory Array(2)	1	X	FFh								
Read Status Register(3)	1	X	70h								
Read Electronic Signature(4)	1	X	90h								
	1	X	98h								
Program(5)	2	X	40h	PA	PD						
	2	X	10h	PA	PD						
Quadruple Byte Program(6)	5	X	30h	A_1	PD	A_2	PD	A_3	PD	A_4	PD
Chip Erase (7)	2	X	80h	X	10h						
Block Erase(5)	2	X	20h	BA	D0h						
Clear Status Register(8)	1	X	50h								
Program/Erase Suspend(9)	1	X	B0h								
Program/Erase Resume(10)	1	X	D0h								
Invalid/Reserved(11)	1	X	00h								
	1	X	01h								
	1	X	60h								
	1	X	2Fh								
	1	X	C0h								

1. X Don't Care, PA Program Address, PD Program Data, $A_{1,2,3,4}$ Consecutive Addresses, BA Any address in the Block.
2. **Read Memory Array**. After a Read Memory Array command, read the memory as normal until another command is issued.
3. **Read Status Register**. After a Read Status Register command, read the Status Register as normal until another command is issued.
4. **Read Electronic Signature**. After a Read Electronic Signature command, read Manufacturer Code, Device Code until another command is issued.
5. **Block Erase, Program**. After these commands read the Status Register until the command completes and another command is issued.
6. **Quadruple Byte Program.** This command is only valid in A/A Mux mode. Addresses A_1, A_2, A_3 and A_4 must be consecutive addresses differing only for address bit A0 and A10. After this command read the Status Register until the command completes and another command is issued.
7. **Chip Erase.** This command is only valid in A/A Mux mode. After this command read the Status Register until the command completes and another command is issued.
8. **Clear Status Register**. After the Clear Status Register command bits 1, 3, 4 and 5 in the Status Register are reset to '0'.
9. **Program/Erase Suspend**. After the Program/Erase Suspend command has been accepted, issue Read Memory Array, Read Status Register, Program (during Erase suspend) and Program/Erase resume commands.
10. **Program/Erase Resume**. After the Program/Erase Resume command the suspended Program/Erase operation resumes, read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.
11. **Invalid/Reserved**. Do not use Invalid or Reserved commands.

5 Status Register

The Status Register provides information on the current or previous Program or Erase operation. Different bits in the Status Register convey different information and errors on the operation.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase and Program/Erase Resume commands are issued. The Status Register can be read from any address.

The Status Register bits are summarized in *Table 10*. The following text descriptions should be read in conjunction with *Table 10*.

5.1 Program/Erase Controller status (bit 7)

The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is '0', the Program/Erase Controller is active; when the bit is '1', the Program/Erase Controller is inactive.

The Program/Erase Controller Status is '0' immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is '1'.

During Program and Erase operation the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is '1'.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Protection Status bits should be tested for errors.

5.2 Erase Suspend status (bit 6)

The Erase Suspend Status bit indicates that a Block Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is '1' (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is '0' the Program/Erase Controller is active or has completed its operation; when the bit is '1' a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns to '0'.

5.3 Erase status (bit 5)

The Erase Status bit can be used to identify if the memory has applied the maximum number of erase pulses to the block(s) and still failed to verify that the block(s) has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is ‘1’ (Program/Erase Controller inactive).

When the Erase Status bit is ‘0’ the memory has successfully verified that the block(s) has erased correctly; when the Erase Status bit is ‘1’ the Program/Erase Controller has applied the maximum number of pulses to the block(s) and still failed to verify that the block(s) has erased correctly.

Once the Erase Status bit is set to ‘1’ it can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If it is set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.4 Program status (bit 4)

The Program Status bit can be used to identify if the memory has applied the maximum number of program pulses to the byte and still failed to verify that the byte has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is ‘1’ (Program/Erase Controller inactive).

When the Program Status bit is ‘0’ the memory has successfully verified that the byte has programmed correctly; when the Program Status bit is ‘1’ the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the byte has programmed correctly.

Once the Program Status bit is set to ‘1’ it can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If it is set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.5 V_{PP} status (bit 3)

The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during a Program or Erase operation.

When the V_{PP} Status bit is ‘0’ the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is ‘1’ the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected; Program and Erase operation cannot be performed.

Once the V_{PP} Status bit set to ‘1’ it can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If it is set to ‘1’ it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

5.6 Program Suspend status (bit 2)

The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is ‘1’ (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is ‘0’ the Program/Erase Controller is active or has completed its operation; when the bit is ‘1’ a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns to ‘0’.

5.7 Block Protection status (bit 1)

The Block Protection Status bit can be used to identify if the Program or Block Erase operation has tried to modify the contents of a protected block. When the Block Protection Status bit is to ‘0’ no Program or Block Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is ‘1’ a Program or Block Erase operation has been attempted on a protected block.

Once it is set to ‘1’ the Block Protection Status bit can only be reset to ‘0’ by a Clear Status Register command or a hardware reset. If it is set to ‘1’ it should be reset before a new Program or Block Erase command is issued, otherwise the new command will appear to fail.

Using the A/A Mux Interface the Block Protection Status bit is always ‘0’.

5.7.1 Reserved (Bit 0)

Bit 0 of the Status Register is reserved. Its value should be masked.

Table 10. Status Register bits

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
Program active	'0'	X(1)	'0'	'0'	'0'	'0'	'0'
Program suspended	'1	X(1)	'0'	'0'	'0'	'1'	'0'
Program completed successfully	'1'	X(1)	'0'	'0'	'0'	'0'	'0'
Program failure due to V_{PP} Error	'1'	X(1)	'0'	'0'	'1'	'0'	'0'
Program failure due to Block Protection (FWH Interface only)	'1'	X(1)	'0'	'0'	'0'	'0'	'1'
Program failure due to cell failure	'1'	X(1)	'0'	'1'	'0'	'0'	'0'
Erase active	'0'	'0'	'0'	'0'	'0'	'0'	'0'
Block Erase suspended	'1'	'1'	'0'	'0'	'0'	'0'	'0'
Erase completed successfully	'1'	'0'	'0'	'0'	'0'	'0'	'0'
Erase failure due to V_{PP} Error	'1'	'0'	'0'	'0'	'1'	'0'	'0'
Block Erase failure due to Block Protection (FWH Interface only)	'1'	'0'	'0'	'0'	'0'	'0'	'1'
Erase failure due to failed cell(s)	'1'	'0'	'1'	'0'	'0'	'0'	'0'

1. For Program operations during Erase Suspend Bit 6 is '1', otherwise Bit 6 is '0'.

6 Firmware Hub (FWH) interface Configuration Registers

When the Firmware Hub Interface is selected several additional registers can be accessed. These registers control the protection status of the Blocks, read the General Purpose Input pins and identify the memory using the Electronic Signature codes. See *Table 11* for the memory map of the Configuration Registers.

6.1 Lock Registers

The Lock Registers control the protection status of the Blocks. Each Block has its own Lock Register. Three bits within each Lock Register control the protection of each block, the Write Lock Bit, the Read Lock Bit and the Lock Down Bit.

The Lock Registers can be read and written, though care should be taken when writing as, once the Lock Down Bit is set, ‘1’, further modifications to the Lock Register cannot be made until cleared, to ‘0’, by a reset or power-up.

See *Table 12* for details on the bit definitions of the Lock Registers.

6.1.1 Write Lock

The Write Lock Bit determines whether the contents of the Block can be modified (using the Program or Block Erase Command). When the Write Lock Bit is set, ‘1’, the block is write protected; any operations that attempt to change the data in the block will fail and the Status Register will report the error. When the Write Lock Bit is reset, ‘0’, the block is not write protected through the Lock Register and may be modified unless write protected through some other means.

When V_{PP} is less than V_{PPLK} all blocks are protected and cannot be modified, regardless of the state of the Write Lock Bit. If Top Block Lock, $\overline{TBL}$, is Low, V_{IL}, then the Top Block (Block 15) is write protected and cannot be modified. Similarly, if Write Protect, $\overline{WP}$, is Low, V_{IL}, then the Main Blocks (Blocks 0 to 14) are write protected and cannot be modified.

After power-up or reset the Write Lock Bit is always set to ‘1’ (write protected).

6.1.2 Read Lock

The Read Lock bit determines whether the contents of the Block can be read (from Read mode). When the Read Lock Bit is set, ‘1’, the block is read protected; any operation that attempts to read the contents of the block will read 00h instead. When the Read Lock Bit is reset, ‘0’, read operations in the Block return the data programmed into the block as expected.

After power-up or reset the Read Lock Bit is always reset to ‘0’ (not read protected).

6.1.3 Lock Down

The Lock Down Bit provides a mechanism for protecting software data from simple hacking and malicious attack. When the Lock Down Bit is set, '1', further modification to the Write Lock, Read Lock and Lock Down Bits cannot be performed. A reset or power-up is required before changes to these bits can be made. When the Lock Down Bit is reset, '0', the Write Lock, Read Lock and Lock Down Bits can be changed.

Table 11. Firmware Hub Register Configuration map

Mnemonic	Register Name	Memory Address	Default Value	Access
T_BLOCK_LK	Top Block Lock Register (Block 15)	FBF0002h	01h	R/W
T_MINUS01_LK	Top Block [-1] Lock Register (Block 14)	FBE0002h	01h	R/W
T_MINUS02_LK	Top Block [-2] Lock Register (Block 13)	FBD0002h	01h	R/W
T_MINUS03_LK	Top Block [-3] Lock Register (Block 12)	FBC0002h	01h	R/W
T_MINUS04_LK	Top Block [-4] Lock Register (Block 11)	FBB0002h	01h	R/W
T_MINUS05_LK	Top Block [-5] Lock Register (Block 10)	FBA0002h	01h	R/W
T_MINUS06_LK	Top Block [-6] Lock Register (Block 9)	FB90002h	01h	R/W
T_MINUS07_LK	Top Block [-7] Lock Register (Block 8)	FB80002h	01h	R/W
T_MINUS08_LK	Top Block [-8] Lock Register (Block 7)	FB70002h	01h	R/W
T_MINUS09_LK	Top Block [-9] Lock Register (Block 6)	FB60002h	01h	R/W
T_MINUS10_LK	Top Block [-10] Lock Register (Block 5)	FB50002h	01h	R/W
T_MINUS11_LK	Top Block [-11] Lock Register (Block 4)	FB40002h	01h	R/W
T_MINUS12_LK	Top Block [-12] Lock Register (Block 3)	FB30002h	01h	R/W
T_MINUS13_LK	Top Block [-13] Lock Register (Block 2)	FB20002h	01h	R/W
T_MINUS14_LK	Top Block [-14] Lock Register (Block 1)	FB10002h	01h	R/W
T_MINUS15_LK	Top Block [-15] Lock Register (Block 0)	FB00002h	01h	R/W
FGPI_REG	Firmware Hub (FWH) General Purpose Input Register	FBC0100h	N/A	R
MANUF_REG	Manufacturer Code Register	FBC0000h	20h	R
DEV_REG	Device Code Register	FBC0001h	2Dh	R

6.2 Firmware Hub (FWH) General-Purpose Input Register

The Firmware Hub (FWH) General Purpose Input Register holds the state of the Firmware Hub Interface General Purpose Input pins, FGPI0-FGPI4. When this register is read, the state of these pins is returned. This register is read-only and writing to it has no effect.

The signals on the Firmware Hub Interface General Purpose Input pins should remain constant throughout the whole Bus Read cycle in order to guarantee that the correct data is read.

6.3 Manufacturer Code Register

Reading the Manufacturer Code Register returns the manufacturer code for the memory. The manufacturer code for STMicroelectronics is 20h. This register is read-only and writing to it has no effect.

6.4 Device Code Register

Reading the Device Code Register returns the device code for the memory, 2Dh. This register is read-only and writing to it has no effect.

Table 12. Lock Register bit definitions(1)

Bit	Bit name	Value	Function
7-3			Reserved
2	Read-Lock	‘1’	Bus Read operations in this Block always return 00h.
		‘0’	Bus read operations in this Block return the Memory Array contents. (Default value).
1	Lock-Down	‘1’	Changes to the Read-Lock bit and the Write-Lock bit cannot be performed. Once a ‘1’ is written to the Lock-Down bit it cannot be cleared to ‘0’; the bit is always reset to ‘0’ following a Reset (using $\overline{RP}$ or $\overline{INIT}$) or after power-up.
		‘0’	Read-Lock and Write-Lock can be changed by writing new values to them. (Default value).
0	Write-Lock	‘1’	Program and Block Erase operations in this Block will set an error in the Status Register. The memory contents will not be changed. (Default value).
		‘0’	Program and Block Erase operations in this Block are executed and will modify the Block contents.

1. Applies to Top Block Lock Register (T_BLOCK_LK) and Top Block [-1] Lock Register (T_MINUS01_LK) to Top Block [-15] Lock Register (T_MINUS15_LK).

Table 13. General-Purpose Input Register definition(1)

Bit	Bit Name	Value	Function
7-5			Reserved
4	FGPI4	‘1’	Input Pin FGPI4 is at V_{IH}
		‘0’	Input Pin FGPI4 is at V_{IL}
3	FGPI3	‘1’	Input Pin FGPI3 is at V_{IH}
		‘0’	Input Pin FGPI3 is at V_{IL}
2	FGPI2	‘1’	Input Pin FGPI2 is at V_{IH}
		‘0’	Input Pin FGPI2 is at V_{IL}
1	FGPI1	‘1’	Input Pin FGPI1 is at V_{IH}
		‘0’	Input Pin FGPI1 is at V_{IL}
0	FGPI0	‘1’	Input Pin FGPI0 is at V_{IH}
		‘0’	Input Pin FGPI0 is at V_{IL}

1. Applies to the General Purpose Input Register (FGPI_REG).

7 Program and Erase times

The Program and Erase times are shown in *Table 14*.

Table 14. Program and Erase times

Parameter	Interface	Test Condition	Min	Typ(1)	Max	Unit
Byte Program				10	200	µs
Quadruple Byte Program	A/A Mux	V_{PP} = 12V ± 5%		10	200	µs
Chip Erase	A/A Mux	V_{PP} = 12V ± 5%		9		sec
Block Program	A/A Mux	V_{PP} = 12V ± 5%		0.1(2)	5	sec
		V_{PP} = V_{CC}		0.4	5	sec
Block Erase		V_{PP} = 12V ± 5%		0.75	8	sec
		V_{PP} = V_{CC}		1	10	sec
Program/Erase Suspend to Program pause(3)					5	µs
Program/Erase Suspend to Block Erase pause(3)					30	µs

1. T_A = 25°C, V_{CC} = 3.3V
2. This time is obtained executing the Quadruple Byte Program Command.
3. Sampled only, not 100% tested.

8 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 15. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output range (1)	–0.50	V_{CC} + 0.6	V
V_{CC}	Supply Voltage	–0.50	4	V
V_{PP}	Program Voltage	–0.6	13	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model)(2)	–2000	2000	V

1. Minimum voltage may undershoot to –2V for less than 20ns during transitions. Maximum voltage may overshoot to V_{CC} + 2V for less than 20ns during transitions.
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

9 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 16*, *Table 17* and *Table 18*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 16. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
T_A	Ambient Operating Temperature (Device Grade 5)	–20	85	°C

Table 17. FWH interface AC measurement conditions

Parameter	Value	Unit
Load Capacitance (C_L)	10	pF
Input Rise and Fall Times	≤1.4	ns
Input Pulse Voltages	0.2 V_{CC} and 0.6 V_{CC}	V
Input and Output Timing Ref. Voltages	0.4 V_{CC}	V

Table 18. A/A Mux interface AC measurement conditions

Parameter	Value	Unit
Load Capacitance (C_L)	30	pF
Input Rise and Fall Times	≤10	ns
Input Pulse Voltages	0 to 3	V
Input and Output Timing Ref. Voltages	1.5	V

Figure 8. FWH interface AC testing input output waveforms

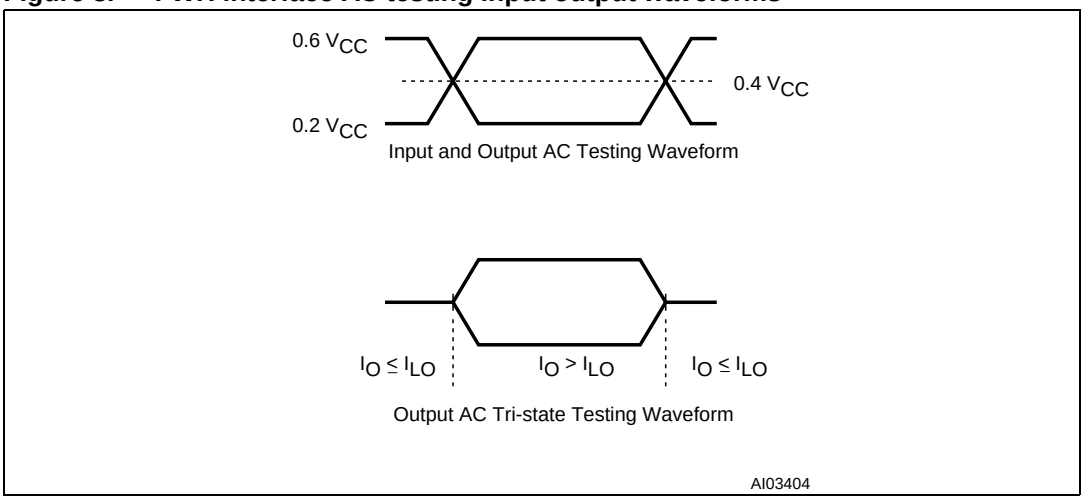


Figure 9. A/A Mux interface AC testing input output waveform

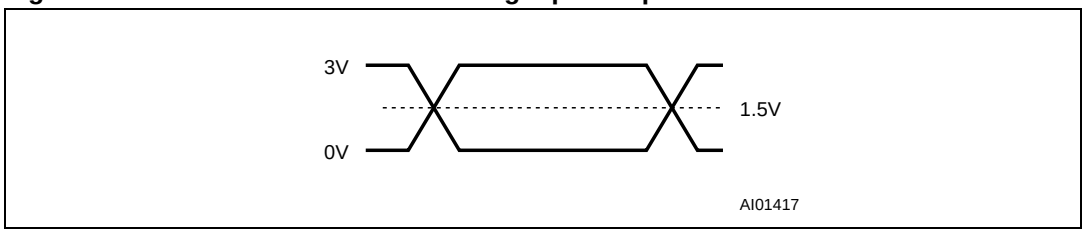


Table 19. Impedance(1)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V		13	pF
C_{CLK}(2)	Clock Capacitance	V_{IN} = 0V	3	12	pF
L_{PIN}(3)	Recommended Pin Inductance			20	nH

1. T_A = 25°C, f = 1MHz.
2. Sampled only, not 100% tested.
3. See PCI Specification.

Table 20. DC characteristics

Symbol	Parameter	Interface	Test condition	Min	Max	Unit
V_{IH}	Input High Voltage	FWH		0.5 V_{CC}	V_{CC} + 0.5	V
		A/A Mux		0.7 V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	FWH		–0.5	0.3 V_{CC}	V
		A/A Mux		-0.5	0.8	V
$V_{IH}(\overline{INIT})$	$\overline{INIT}$ Input High Voltage	FWH		1.35	V_{CC} + 0.5	V
$V_{IL}(\overline{INIT})$	$\overline{INIT}$ Input Low Voltage	FWH		–0.5	0.2 V_{CC}	V
I_{LI}(1)	Input Leakage Current		$0V \leq V_{IN} \leq V_{CC}$		±10	µA
I_{LI2}	IC, IDx Input Leakage Current		IC, ID0, ID1, ID2, ID3 = V_{CC}		200	µA
R_{IL}	IC, IDx Input Pull Low Resistor			20	100	kΩ
V_{OH}	Output High Voltage	FWH	I_{OH} = –500µA	0.9 V_{CC}		V
		A/A Mux	I_{OH} = –100µA	V_{CC} – 0.4		V
V_{OL}	Output Low Voltage	FWH	I_{OL} = 1.5mA		0.1 V_{CC}	V
		A/A Mux	I_{OL} = 1.8mA		0.45	V
I_{LO}	Output Leakage Current		$0V \leq V_{OUT} \leq V_{CC}$		±10	µA
V_{PP1}	V_{PP} Voltage			3	3.6	V
V_{PPH}	V_{PP} Voltage (Fast Program/Fast Erase)			11.4	12.6	V
V_{PPLK}(2)	V_{PP} Lockout Voltage			1.5		V
V_{LKO}(2)	V_{CC} Lockout Voltage			1.8	2.3	V
I_{CC1}	Supply Current (Standby)	FWH	FWH4 = 0.9V_{CC}, V_{PP} = V_{CC} All other inputs 0.9V_{CC} to 0.1V_{CC} V_{CC} = 3.6 V, f(CLK) = 33 MHz		100	µA
I_{CC2}	Supply Current (Standby)	FWH	FWH4 = 0.1V_{CC}, V_{PP} = V_{CC} All other inputs 0.9V_{CC} to 0.1V_{CC} V_{CC} = 3.6 V, f(CLK) = 33 MHz		10	mA
I_{CC3}	Supply Current (Any internal operation active)	FWH	V_{CC} = V_{CC} max, V_{PP} = V_{CC} f(CLK) = 33 MHz I_{OUT} = 0 mA		60	mA
I_{CC4}	Supply Current (Read)	A/A Mux	$\overline{G}$ = V_{IH}, f = 6MHz		20	mA
I_{CC5}(2)	Supply Current (Program/Erase)	A/A Mux	Program/Erase Controller Active		20	mA
I_{PP}	V_{PP} Supply Current (Read/Standby)		$V_{PP} \geq V_{CC}$		400	µA
I_{PP1}(2)	V_{PP} Supply Current (Program/Erase active)		V_{PP} = V_{CC}		40	mA
			V_{PP} = 12V ± 5%		15	mA

1. Input leakage currents include High-Z output leakage for all bi-directional buffers with tri-state outputs.
2. Sampled only, not 100% tested.

Figure 10. FWH interface clock waveform

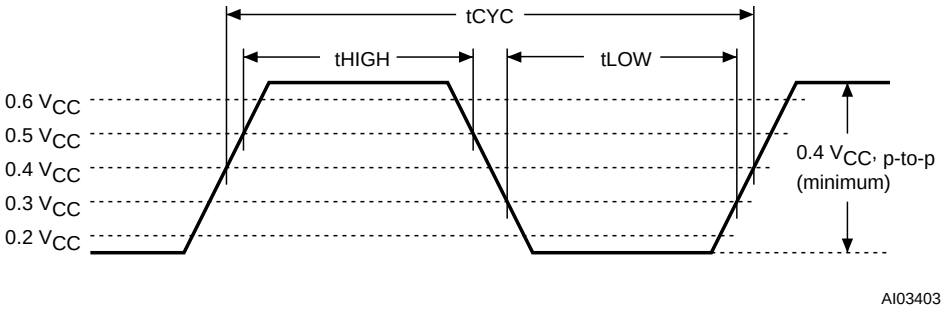


Table 21. FWH interface clock characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{CYC}	CLK Cycle Time(1)		Min	30	ns
t_{HIGH}	CLK High Time		Min	11	ns
t_{LOW}	CLK Low Time		Min	11	ns
	CLK Slew Rate	peak to peak	Min	1	V/ns
			Max	4	V/ns

1. Devices on the PCI Bus must work with any clock frequency between DC and 33MHz. Below 16MHz devices may be guaranteed by design rather than tested. Refer to PCI Specification.

Figure 11. FWH interface AC signal timing waveforms

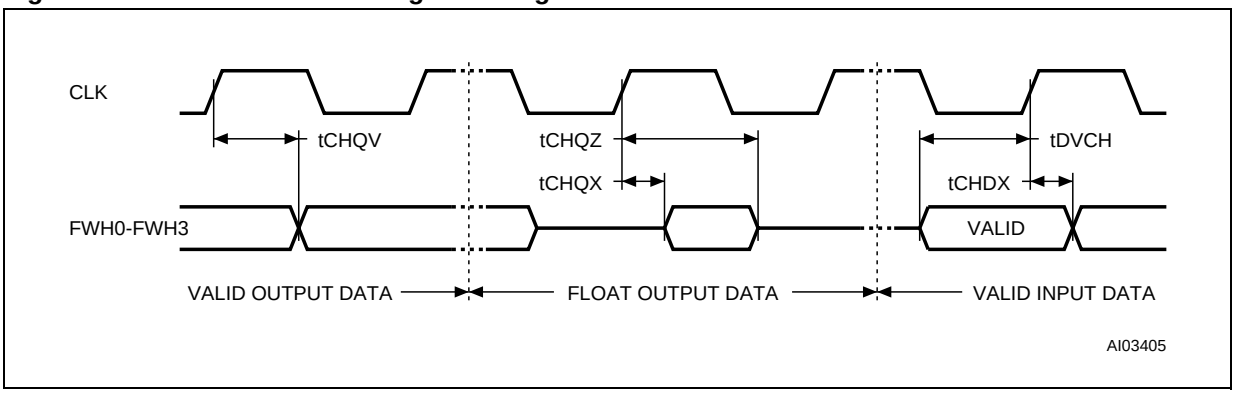


Table 22. FWH interface AC signal timing characteristics

Symbol	PCI Symbol	Parameter	Test condition		Value	Unit
t_{CHQV}	t_{val}	CLK to Data Out		Min	2	ns
				Max	11	ns
t_{CHQX}(1)	t_{on}	CLK to Active (Float to Active Delay)		Min	2	ns
t_{CHQZ}	t_{off}	CLK to Inactive (Active to Float Delay)		Max	28	ns
t_{AVCH} t_{DVCH}	t_{su}	Input Set-up Time(2)		Min	7	ns
t_{CHAX} t_{CHDX}	t_h	Input Hold Time(2)		Min	0	ns

1. The timing measurements for Active/Float transitions are defined when the current through the pin equals the leakage current specification.
2. Applies to all inputs except CLK.

Figure 12. Reset AC waveforms

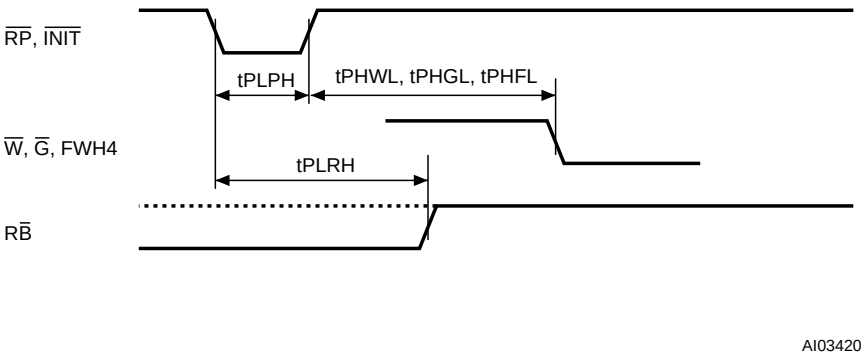


Table 23. Reset AC characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{PLPH}	RP or INIT Reset Pulse Width		Min	100	ns
t_{PLRH}	RP or INIT Low to Reset	Program/Erase Inactive	Max	100	ns
		Program/Erase Active	Max	30	µs
	RP or INIT Slew Rate(1)	Rising edge only	Min	50	mV/ns
t_{PHFL}	RP or INIT High to FWH4 Low	FWH Interface only	Min	30	µs
t_{PHWL} t_{PHGL}	RP High to Write Enable or Output Enable Low	A/A Mux Interface only	Min	50	µs

1. See Chapter 4 of the PCI Specification.

Figure 13. A/A Mux interface Read AC waveforms

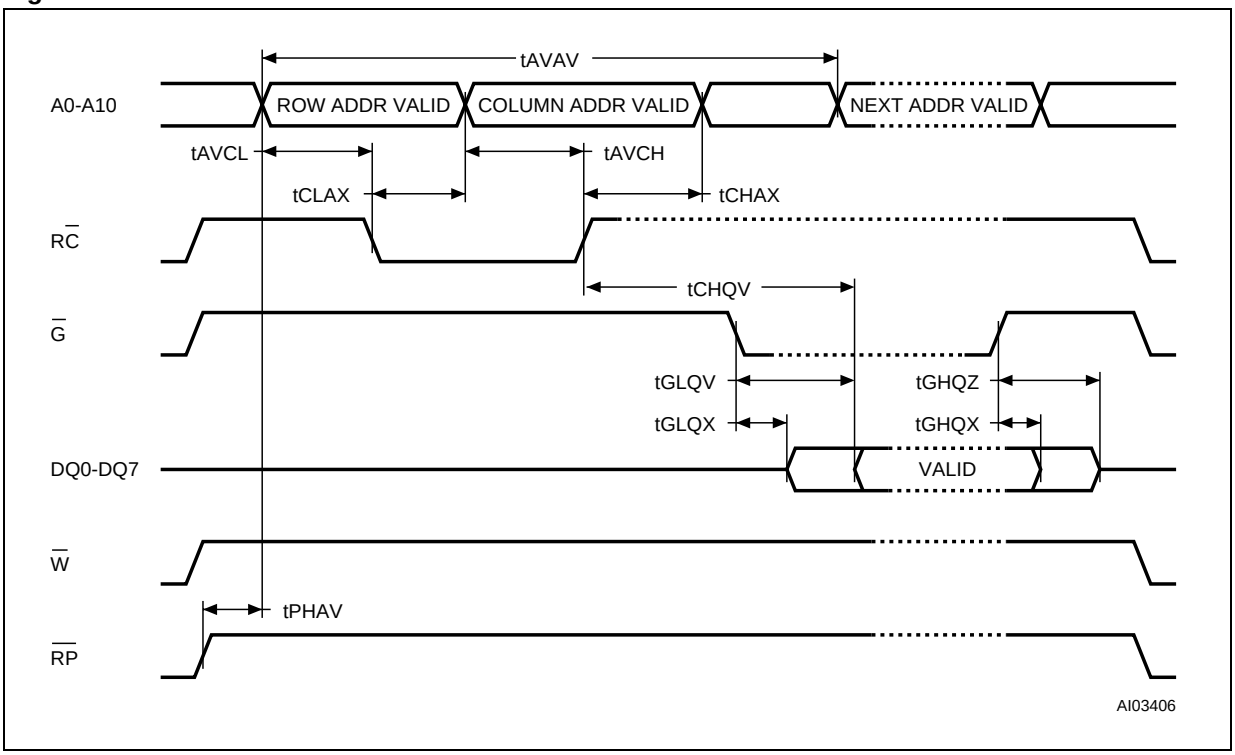


Table 24. A/A Mux interface Read AC characteristics

Symbol	Parameter	Test Condition		Value	Unit
t_{AVAV}	Read Cycle Time		Min	250	ns
t_{AVCL}	Row Address Valid to $\overline{RC}$ Low		Min	50	ns
t_{CLAX}	$\overline{RC}$ Low to Row Address Transition		Min	50	ns
t_{AVCH}	Column Address Valid to $\overline{RC}$ high		Min	50	ns
t_{CHAX}	$\overline{RC}$ High to Column Address Transition		Min	50	ns
t_{CHQV}(1)	$\overline{RC}$ High to Output Valid		Max	150	ns
t_{GLQV}(1)	Output Enable Low to Output Valid		Max	50	ns
t_{PHAV}	$\overline{RP}$ High to Row Address Valid		Min	1	µs
t_{GLQX}	Output Enable Low to Output Transition		Min	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z		Max	50	ns
t_{GHQX}	Output Hold from Output Enable High		Min	0	ns

1. $\overline{G}$ may be delayed up to $t_{CHQV} - t_{GLQV}$ after the rising edge of $\overline{RC}$ without impact on t_{CHQV}.

Figure 14. A/A Mux interface Write AC waveforms

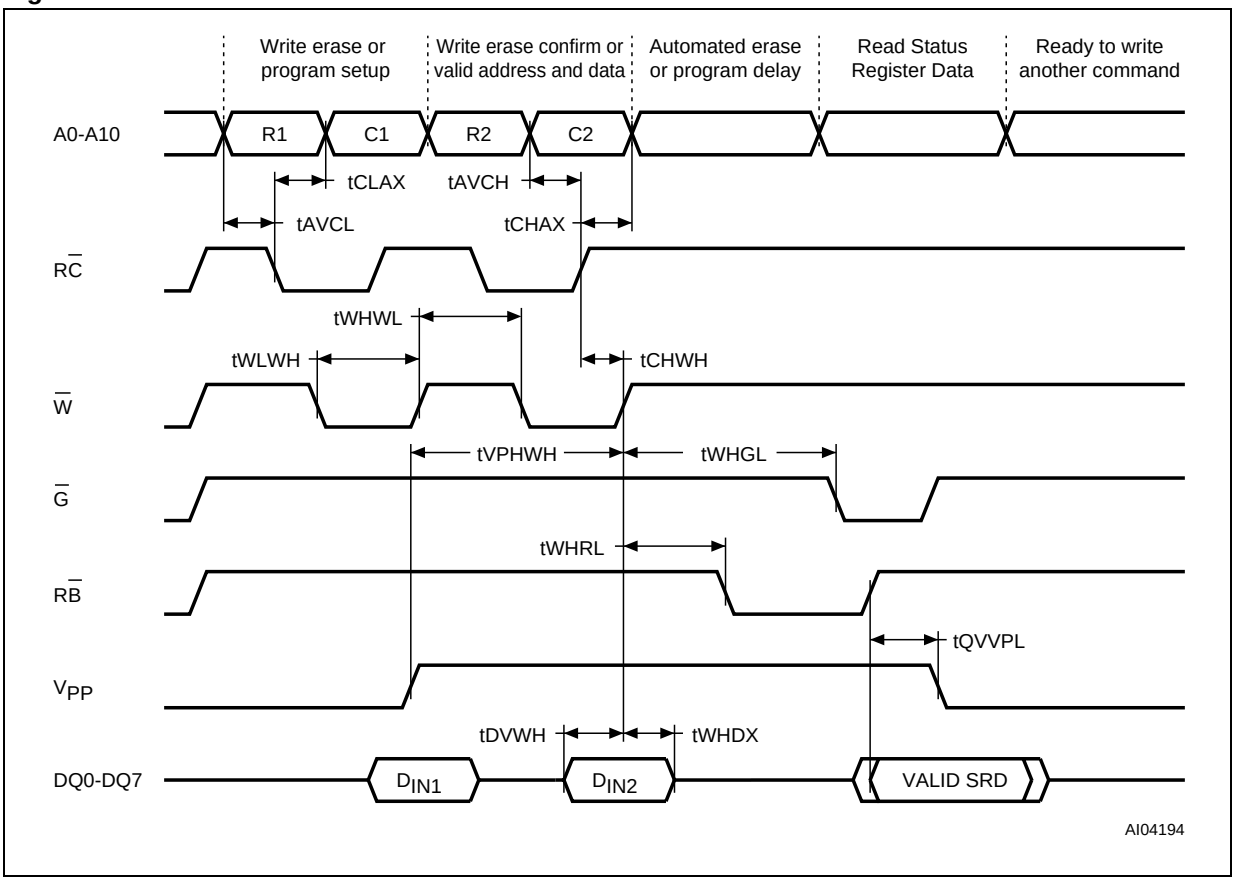


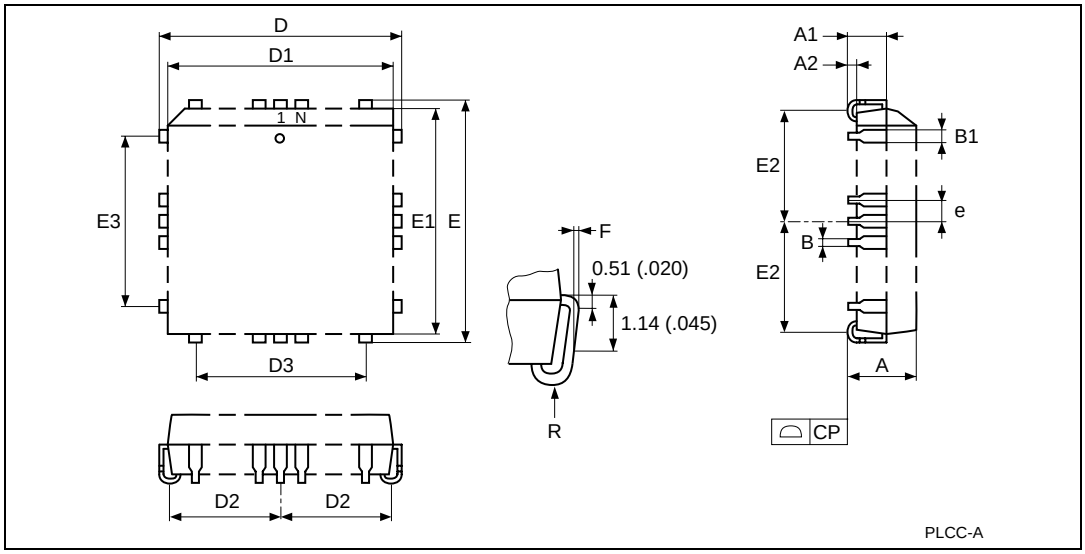
Table 25. A/A Mux interface Write AC characteristics

Symbol	Parameter	Test condition		Value	Unit
t_{WLWH}	Write Enable Low to Write Enable High		Min	100	ns
t_{DVWH}	Data Valid to Write Enable High		Min	50	ns
t_{WHDX}	Write Enable High to Data Transition		Min	5	ns
t_{AVCL}	Row Address Valid to $\overline{RC}$ Low		Min	50	ns
t_{CLAX}	$\overline{RC}$ Low to Row Address Transition		Min	50	ns
t_{AVCH}	Column Address Valid to $\overline{RC}$ High		Min	50	ns
t_{CHAX}	$\overline{RC}$ High to Column Address Transition		Min	50	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	100	ns
t_{CHWH}	$\overline{RC}$ High to Write Enable High		Min	50	ns
t_{VPHWH} (1)	V_{PP} High to Write Enable High		Min	100	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	30	ns
t_{WHRL}	Write Enable High to $\overline{RB}$ Low		Min	0	ns
t_{QVVPL} (1),(2)	Output Valid, $\overline{RB}$ High to V_{PP} Low		Min	0	ns

1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

10 Package mechanical

Figure 15. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, package outline

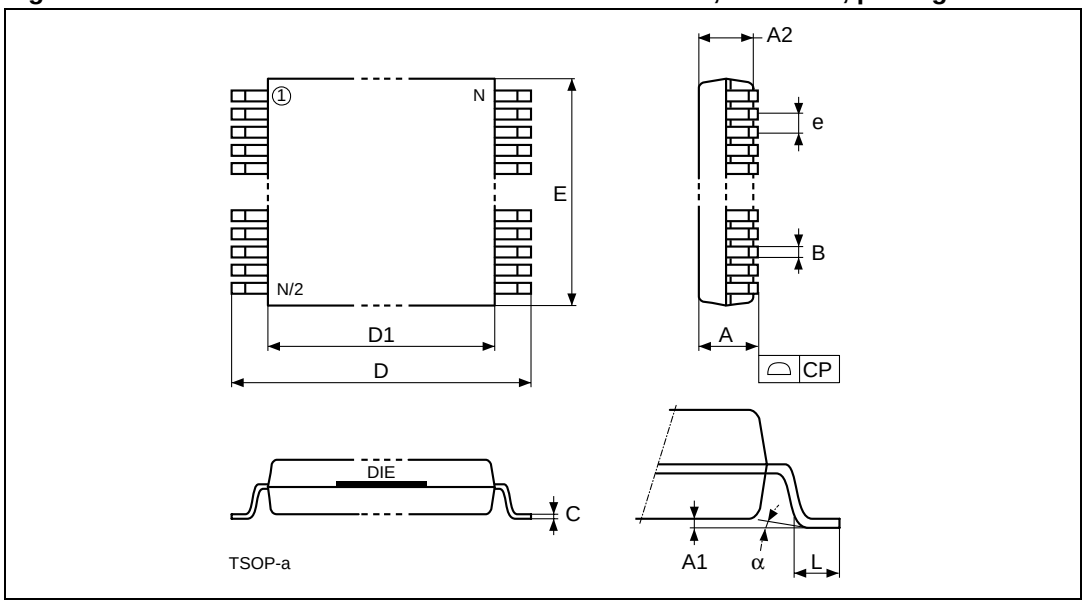


1. Drawing is not to scale.

Table 26. PLCC32 – 32 pin Rectangular Plastic Leaded Chip Carrier, package data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A		3.18	3.56		0.125	0.140
A1		1.53	2.41		0.060	0.095
A2		0.38	–		0.015	–
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
CP			0.10			0.004
D		12.32	12.57		0.485	0.495
D1		11.35	11.51		0.447	0.453
D2		4.78	5.66		0.188	0.223
D3	7.62	–	–	0.300	–	–
E		14.86	15.11		0.585	0.595
E1		13.89	14.05		0.547	0.553
E2		6.05	6.93		0.238	0.273
E3	10.16	–	–	0.400	–	–
e	1.27	–	–	0.050	–	–
F		0.00	0.13		0.000	0.005
R	0.89	–	–	0.035	–	–
N	32			32		

Figure 16. TSOP32 – 32 lead Plastic Thin Small Outline, 8x14 mm, package outline

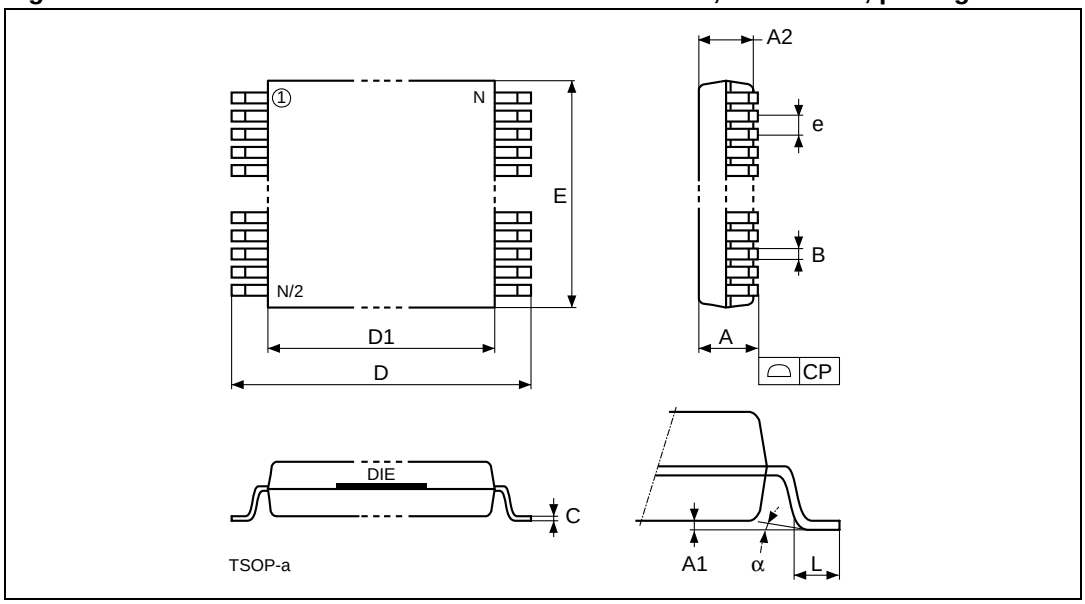


1. Drawing is not to scale.

Table 27. TSOP32 – 32 lead Plastic Thin Small Outline, 8x14 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
α		0°	5°		0°	5°
B		0.170	0.270		0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
CP			0.100			0.0039
D		13.800	14.200		0.5433	0.5591
D1		12.300	12.500		0.4843	0.4921
e	0.500	–	–	0.0197	–	–
E		7.900	8.100		0.3110	0.3189
L		0.500	0.700		0.0197	0.0276
N	32			32		

Figure 17. TSOP40 – 40 lead Plastic Thin Small Outline, 10 x 20mm, package outline



1. Drawing is not to scale.

Table 28. TSOP40 – 40 lead Plastic Thin Small Outline, 10 x 20mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0
A1		0.050	0.150		0	0
A2		0.950	1.050		0	0
B		0.170	0.270		0	0
C		0.100	0.210		0	0
CP			0.100			0
D		19.800	20.200		1	1
D1		18.300	18.500		1	1
e	0.500	–	–	0	–	–
E		9.900	10.100		0	0
L		0.500	0.700		0	0
α		0°	5°		0°	5°
N	40			40		

11 Part numbering

Table 29. Ordering information scheme

Example: M50FW080 N 5 T G

Device Type

M50 = Flash Memory for PC BIOS

Architecture

F = Firmware Hub Interface

Operating Voltage

W = V_{CC} = 3.0 to 3.6V

Device Function

080 = 8 Mbit (1Mbx8), Uniform Blocks

Package

K = PLCC32

NB = TSOP32: 8 x 14mm(1)

N = TSOP40: 10 x 20mm

Device Grade

5 = Temperature range –20 to 85 °C.

Device tested with standard test flow

Option

blank = Standard Packing

T = Tape and Reel Packing

Plating Technology

P or G = ECOPACK® (RoHs compliant)

1. Devices sold in this package are Not Recommended for New Design.

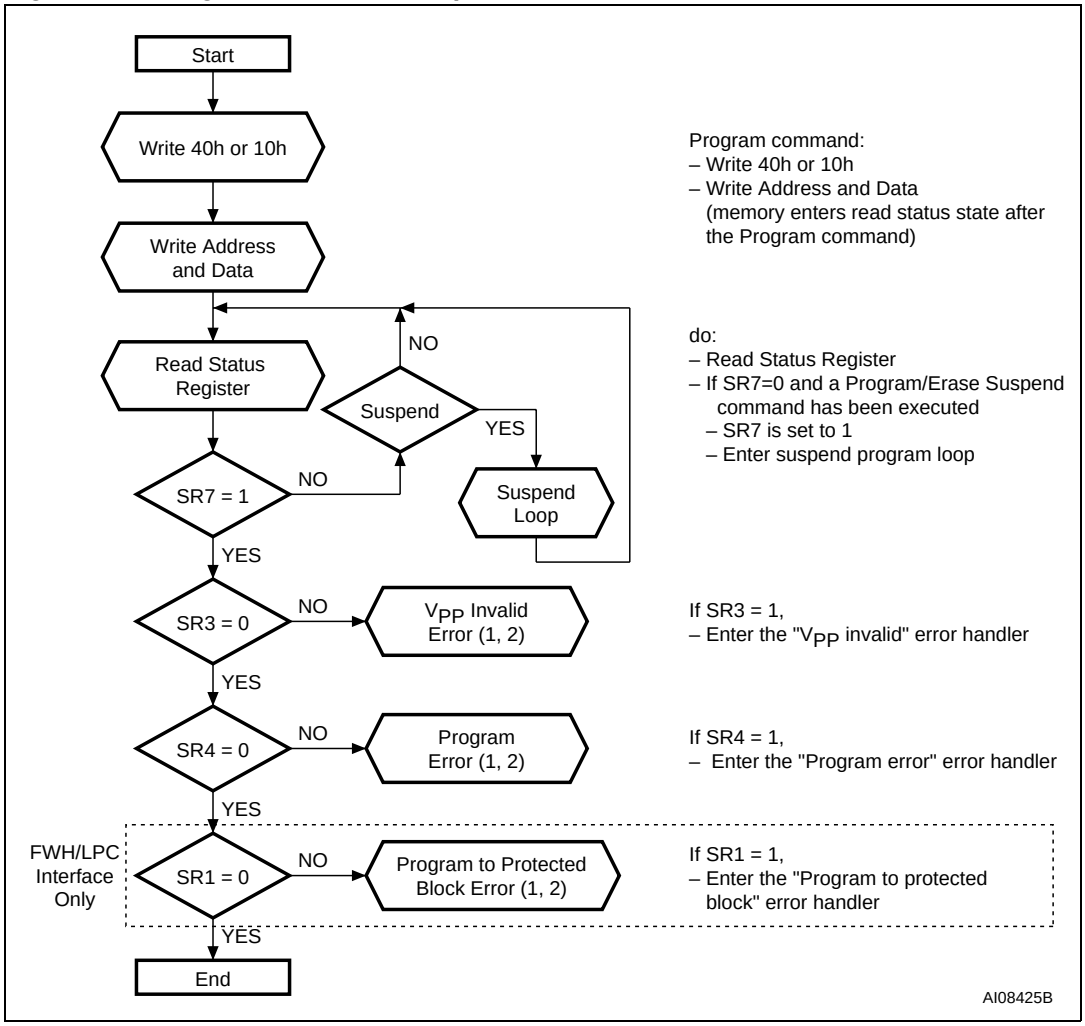
Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

The category of second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

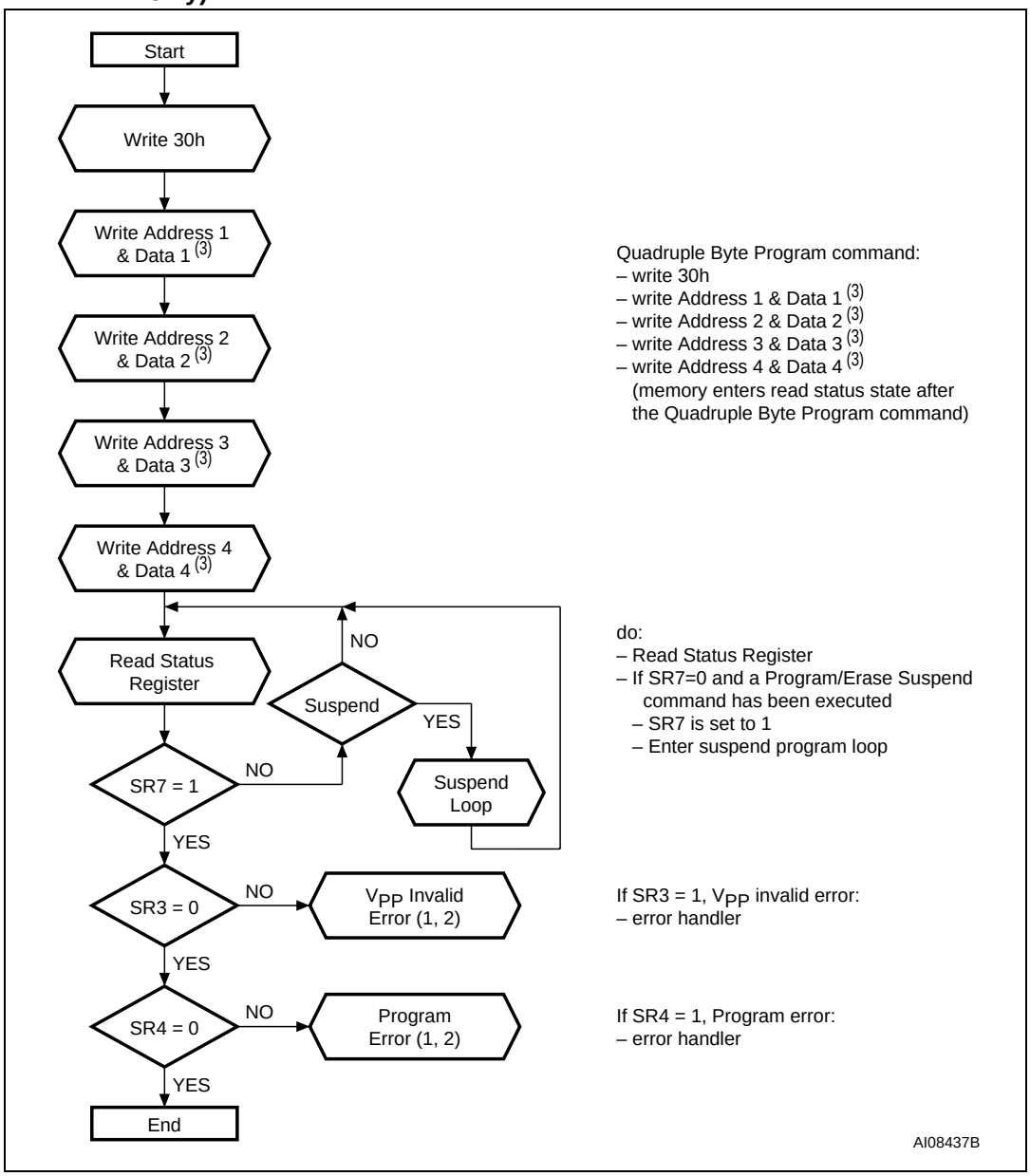
Appendix A Flowcharts and pseudo codes

Figure 18. Program flowchart and pseudo code



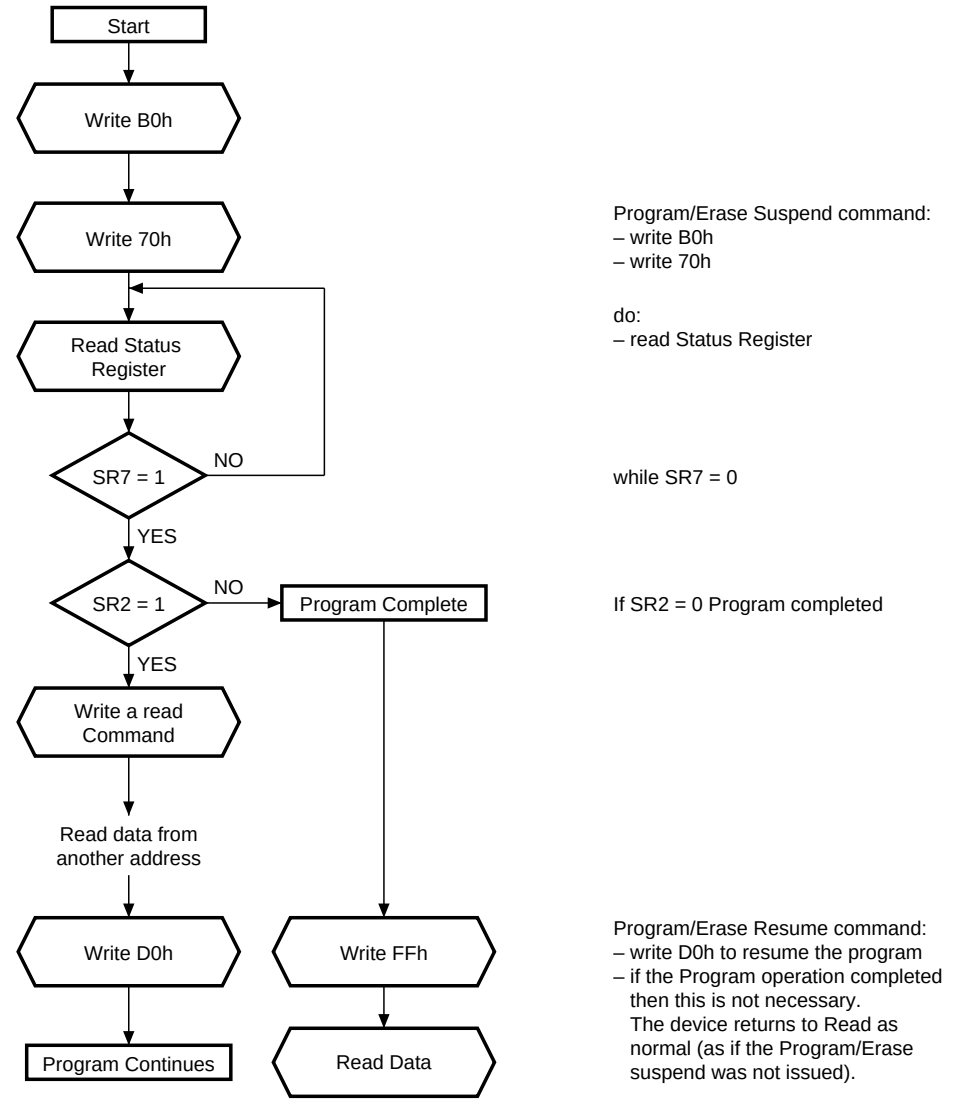
1. A Status check of SR1 (Protected Block), SR3 (V_{PP} invalid) and SR4 (Program Error) can be made after each Program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 19. Quadruple Byte Program flowchart and pseudo code (A/A Mux interface only)



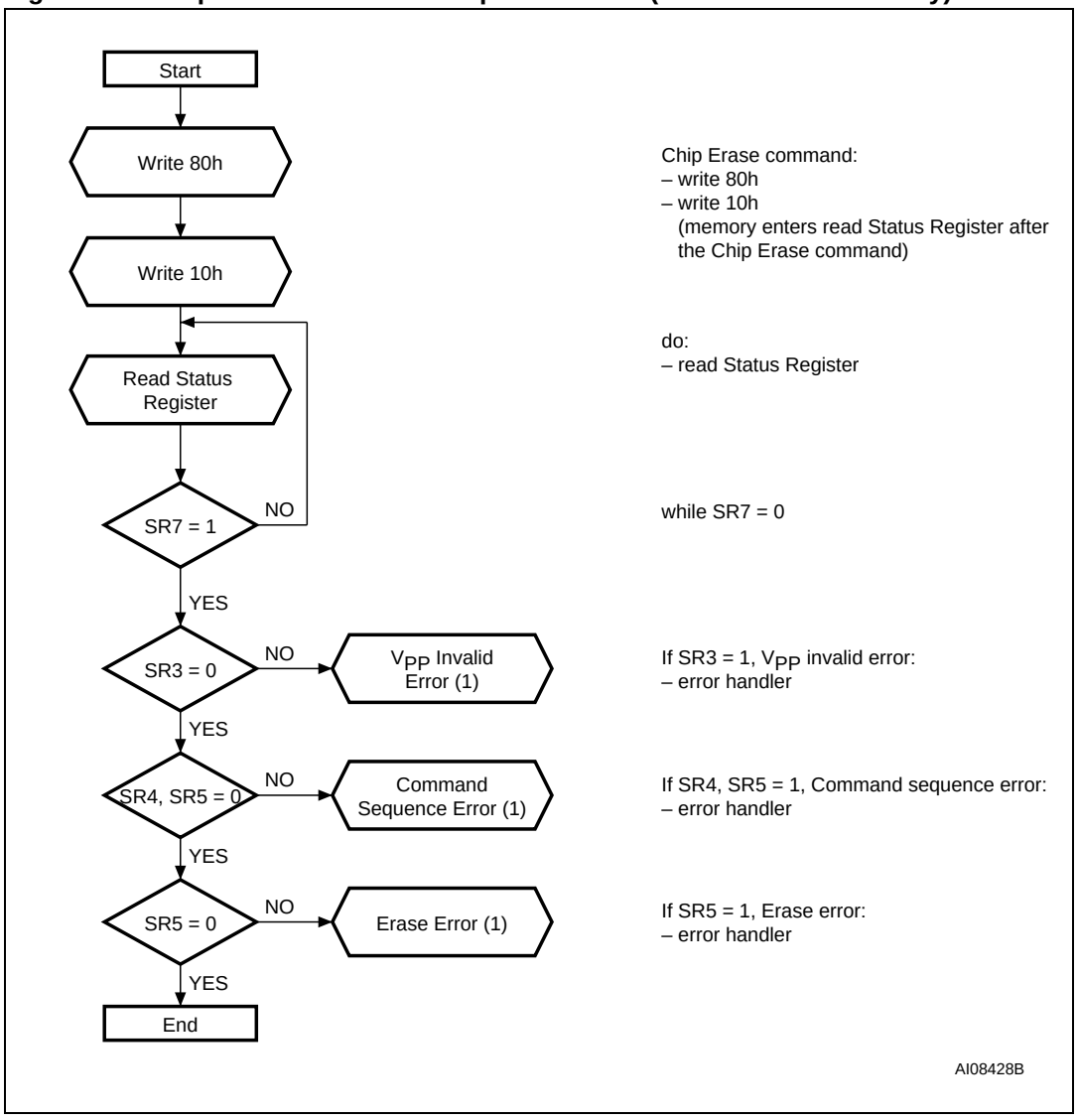
1. A Status check of SR3 (V_{PP} invalid) and SR4 (Program Error) can be made after each Program operation by following the correct command sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.
3. Address1, Address 2, Address 3 and Address 4 must be consecutive addresses differing only for address bits A0 and A1.

Figure 20. Program Suspend and Resume flowchart and pseudo code



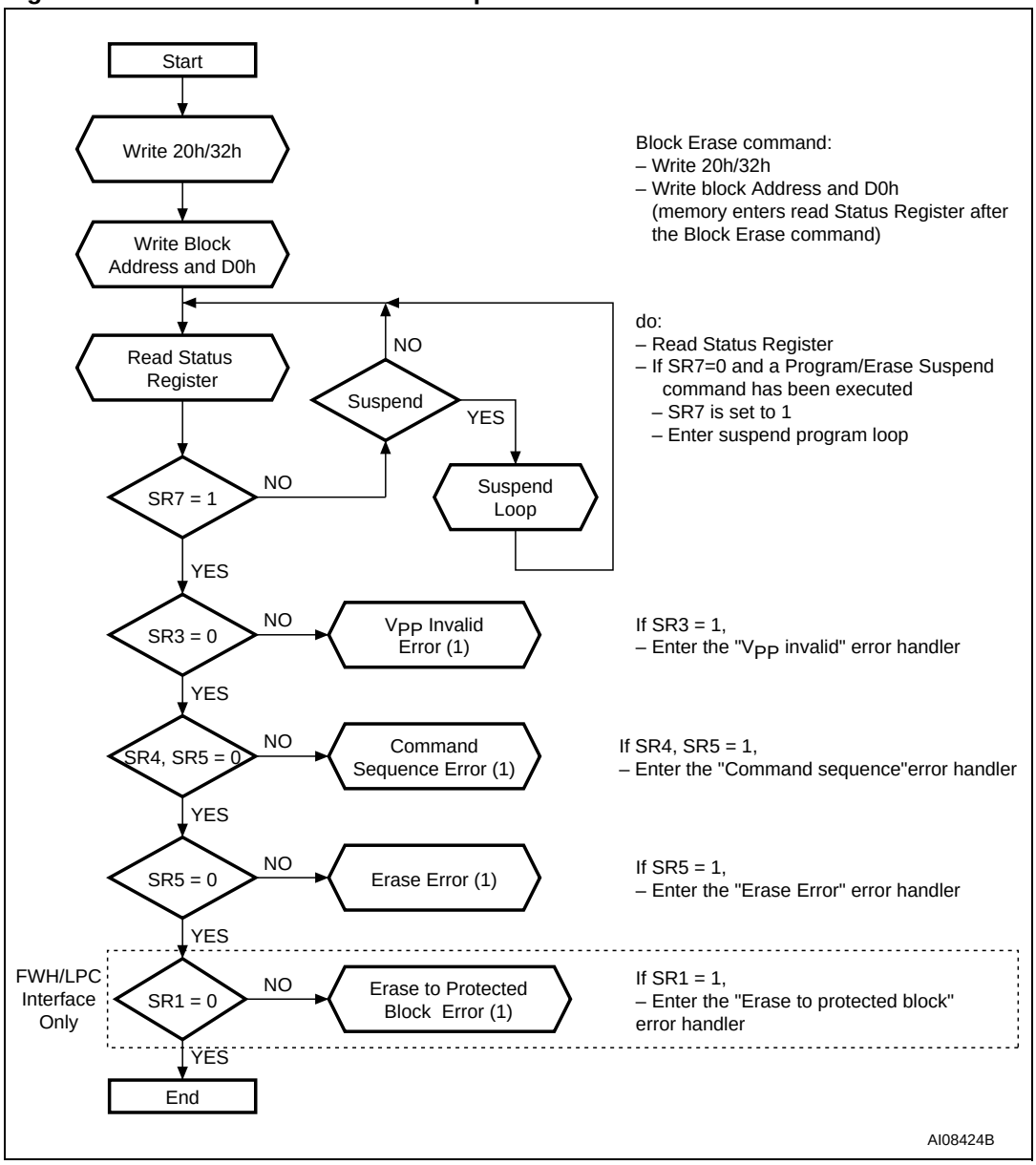
1. If an error is found, the Status Register must be cleared before further Program/Erase operations.
2. Any address within the bank can equally be used.

Figure 21. Chip Erase flowchart and pseudo code (A/A Mux interface only)



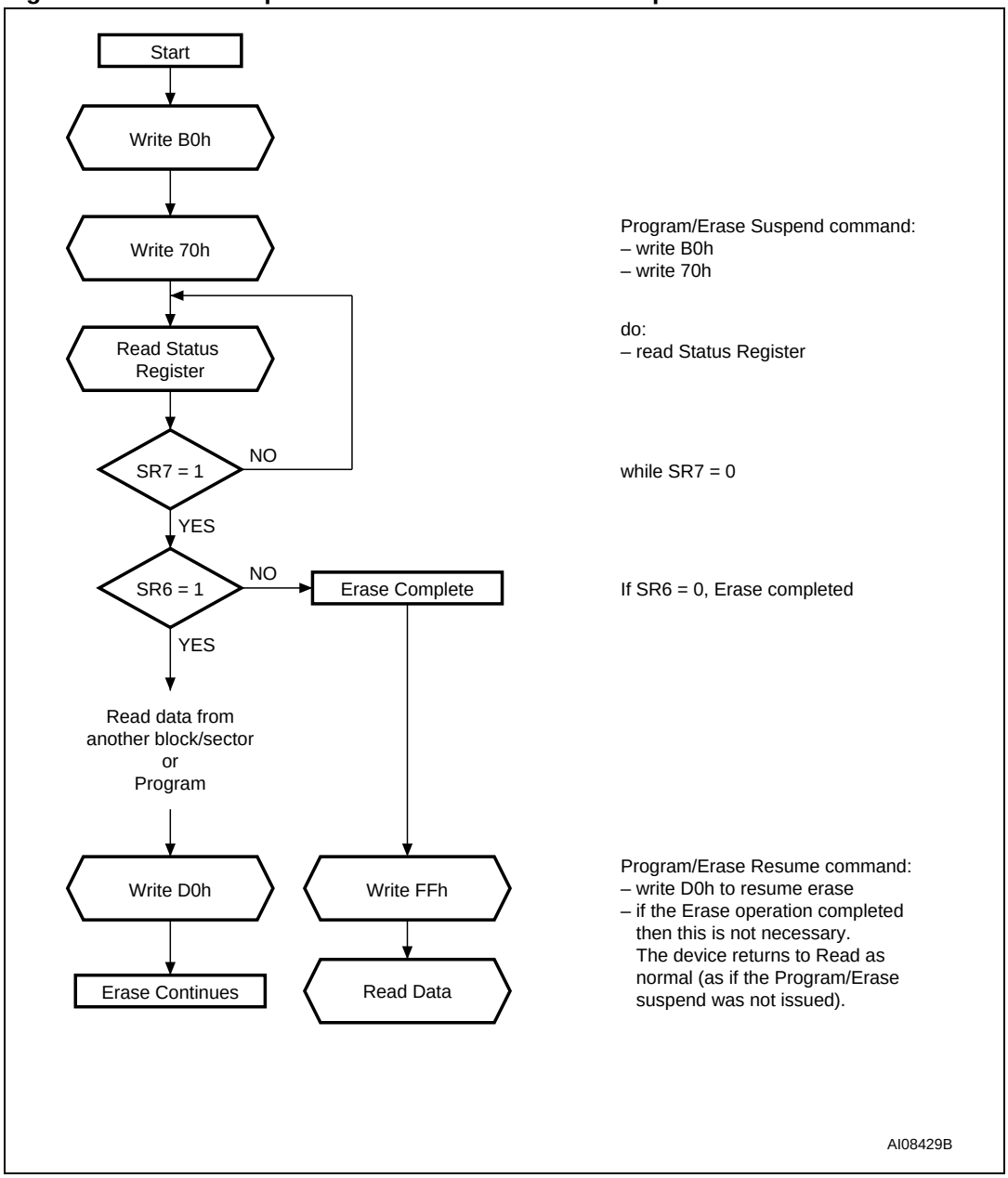
1. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 22. Block Erase flowchart and pseudo code



1. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 23. Erase Suspend and Resume flowchart and pseudo code



12 Revision history

Table 30. Document revision history

Date	Version	Changes
April 2001	-01	First Issue
18-May-2001	-02	Document type: from Product Preview to Preliminary Data
22-Jun-2001	-03	PLCC32 package added
6-Jul-2001	-04	Note 2 changed (*Table 15*, Absolute Maximum Ratings)
30-Jan-2002	-05	Document promoted from Preliminary Data to Full Data Sheet
01-Mar-2002	-06	RFU pins must be left disconnected
12-Mar-2002	-07	Specification of PLCC32 package mechanical data revised
19-May-2004	8.0	TSOP32 package added. Part numbering information updated. Flow-chart illustrations, in Appendix, updated. Document reformatted
19-Aug-2004	9.0	Pins 2 and 5 of the TSOP32 Connections illustration corrected
24-Oct-2006	10	Document converted to new ST template. Small text changes. Device Grade 1 removed. Packages are ECOPACK® compliant. T_{LEAD} removed from *Table 15: Absolute maximum ratings*. Blank option removed from below *Plating Technology* in *Table 29: Ordering information scheme*.

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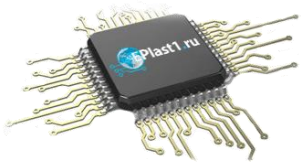
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.