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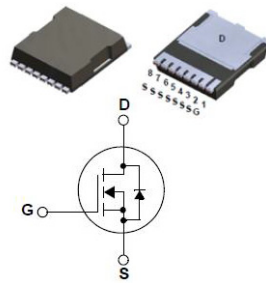
# FDBL86063-F085 N-Channel Power Trench® MOSFET 100 V, 240 A, 2.6 mΩ

## Features

- Typical  $R_{DS(on)} = 2\text{ m}\Omega$  at  $V_{GS} = 10\text{V}$ ,  $I_D = 80\text{ A}$
- Typical  $Q_{g(tot)} = 73\text{ nC}$  at  $V_{GS} = 10\text{V}$ ,  $I_D = 80\text{ A}$
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

## Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems



## MOSFET Maximum Ratings $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Drain Current - Continuous ( $V_{GS}=10$ ) (Note 1)	$T_C = 25^\circ\text{C}$ 240	A
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$ See Figure 4	
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	160	mJ
$P_D$	Power Dissipation	357	W
	Derate Above $25^\circ\text{C}$	2.38	$\text{W}/^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to + 175	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.42	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information Notes:

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL86063	FDBL86063-F085	MO-299A	13"	24mm	2000 units

### Notes:

- 1: Current is limited by bondwire configuration.
- 2: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 50\mu\text{H}$ ,  $I_{AS} = 80\text{A}$ ,  $V_{DD} = 100\text{V}$  during inductor charging and  $V_{DD} = 0\text{V}$  during time in avalanche.
- 3:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a  $1\text{ in}^2$  pad of 2oz copper.

**Electrical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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**Off Characteristics**

$V_{DSS}$	Drain-to-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	100	-	-	V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{DS} = 100\text{V}, T_J = 25^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	-	1.5	mA
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	$\pm 100$	nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	2.9	4	V
$r_{DS(on)}$	Drain-to-Source On-Resistance	$I_D = 80\text{A}, T_J = 25^\circ\text{C}$	-	2.0	2.6	$\text{m}\Omega$
		$V_{GS} = 10\text{V}, T_J = 175^\circ\text{C}$ (Note 4)	-	4.2	5.6	$\text{m}\Omega$

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	-	5120	-	pF
$C_{oss}$	Output Capacitance		-	3220	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	32	-	pF
$R_g$	Gate Resistance	$V_{GS} = 0.5\text{V}, f = 1\text{MHz}$	-	0.4	-	$\Omega$
$Q_{g(ToT)}$	Total Gate Charge	$V_{GS} = 0$ to 10V	-	73	95	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	-	9	-	nC
$Q_{gs}$	Gate-to-Source Gate Charge	$V_{DD} = 50\text{V}, I_D = 80\text{A}$	-	22	-	nC
$Q_{gd}$	Gate-to-Drain "Miller" Charge		-	17	-	nC

**Switching Characteristics**

$t_{on}$	Turn-On Time	$V_{DD} = 50\text{V}, I_D = 80\text{A}$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	-	-	53	ns
$t_{d(on)}$	Turn-On Delay		-	25	-	ns
$t_r$	Rise Time		-	16	-	ns
$t_{d(off)}$	Turn-Off Delay		-	32	-	ns
$t_f$	Fall Time		-	8	-	ns
$t_{off}$	Turn-Off Time		-	-	51	ns

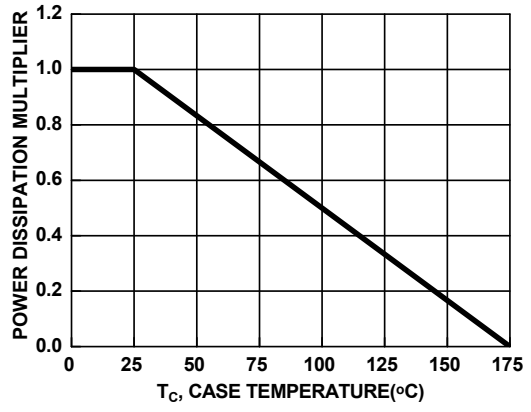
**Drain-Source Diode Characteristics**

$V_{SD}$	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{A}, V_{GS} = 0\text{V}$	-	0.9	1.25	V
		$I_{SD} = 40\text{A}, V_{GS} = 0\text{V}$	-	0.8	1.2	V
$t_{rr}$	Reverse-Recovery Time	$I_F = 80\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	107	139	ns
$Q_{rr}$	Reverse-Recovery Charge		-	175	260	nC

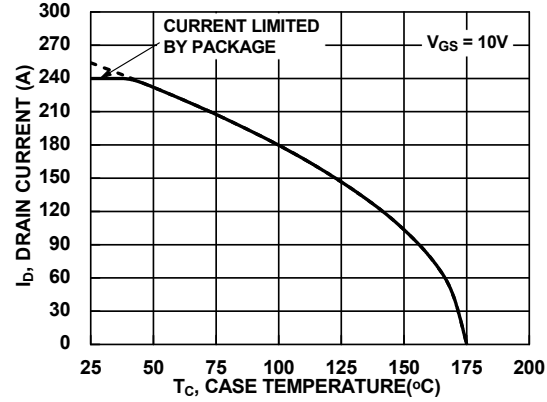
**Note:**

 4: The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production.

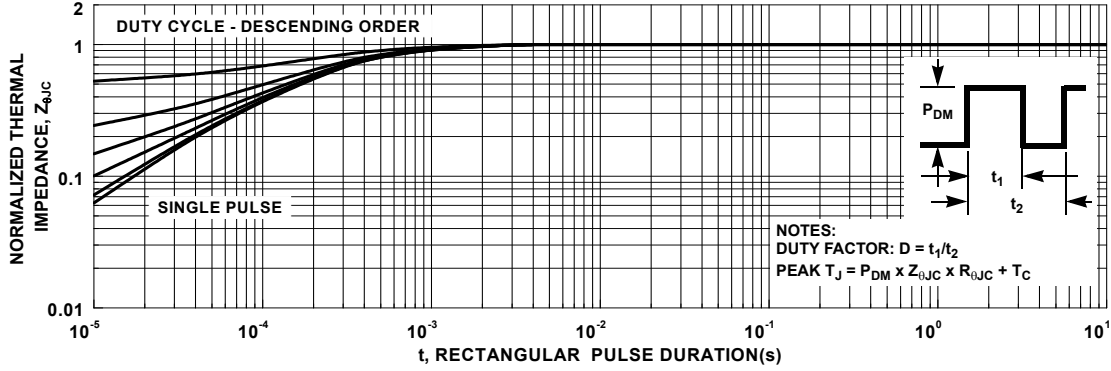
**Typical Characteristics**



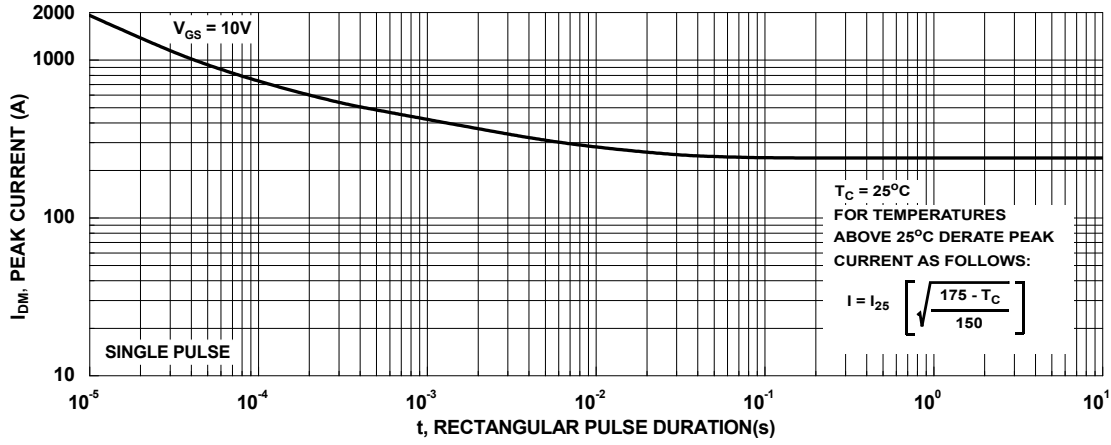
**Figure 1. Normalized Power Dissipation vs. Case Temperature**



**Figure 2. Maximum Continuous Drain Current vs. Case Temperature**



**Figure 3. Normalized Maximum Transient Thermal Impedance**



**Figure 4. Peak Current Capability**

## Typical Characteristics

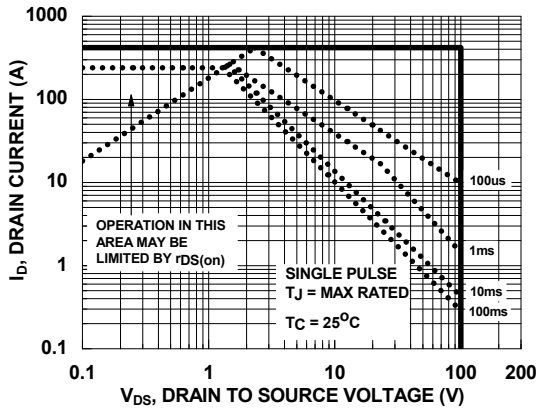
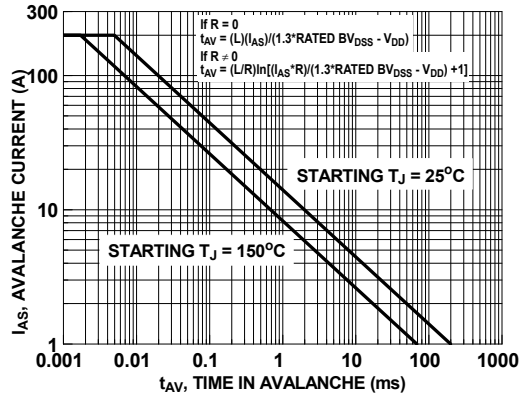


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to S u t Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

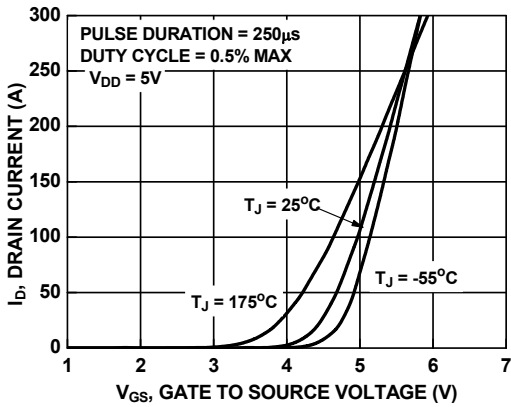


Figure 7. Transfer Characteristics

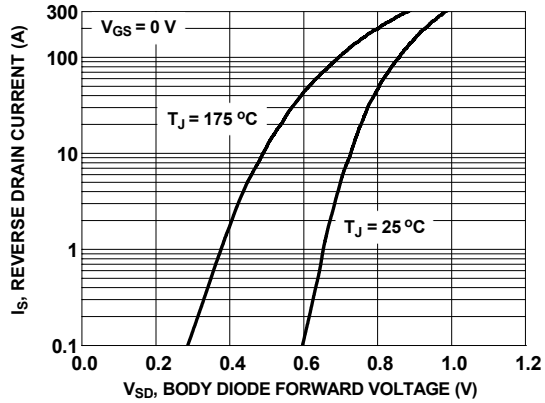


Figure 8. Forward Diode Characteristics

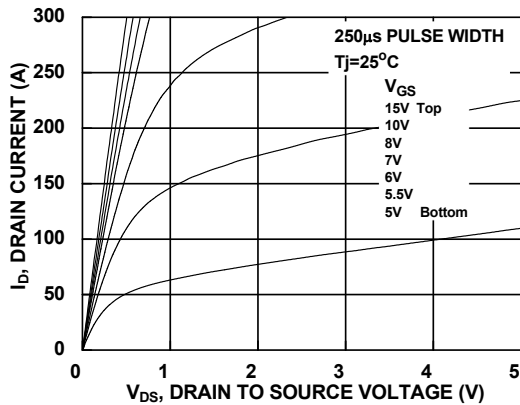


Figure 9. Saturation Characteristics

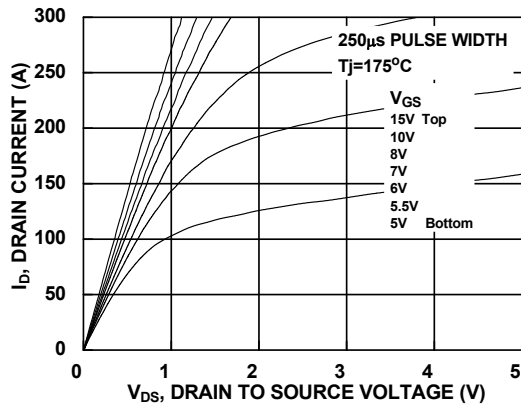
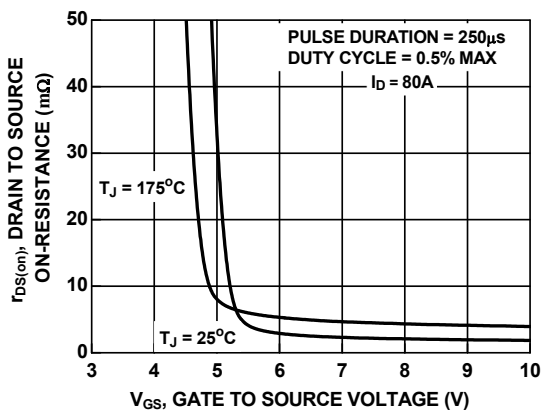
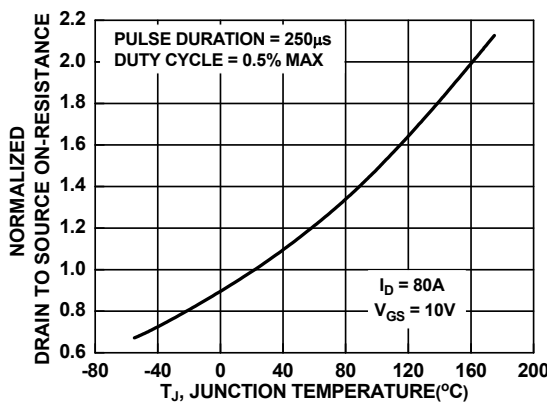


Figure 10. Saturation Characteristics

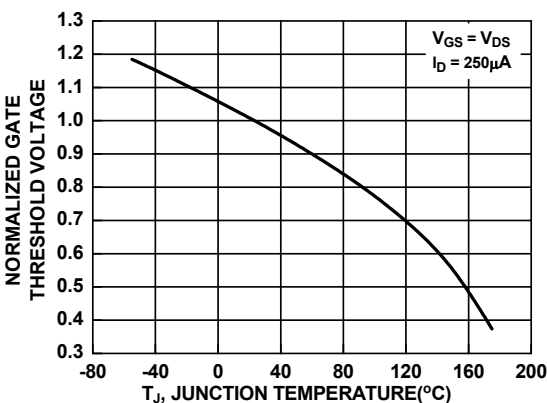
**Typical Characteristics**



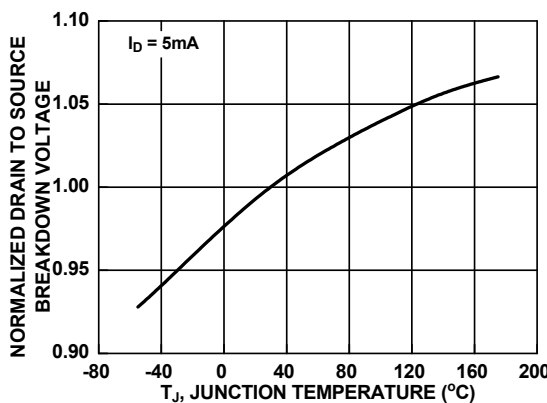
**Figure 11.  $R_{DS(on)}$  vs. Gate Voltage**



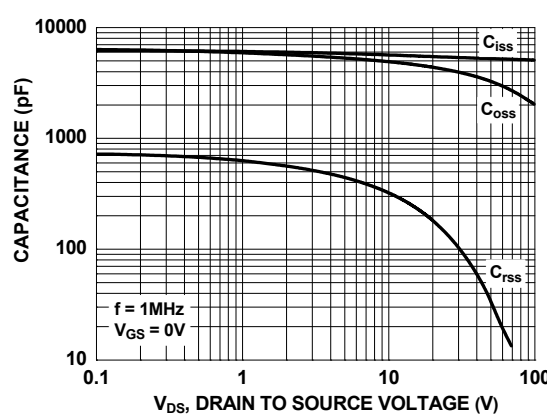
**Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature**



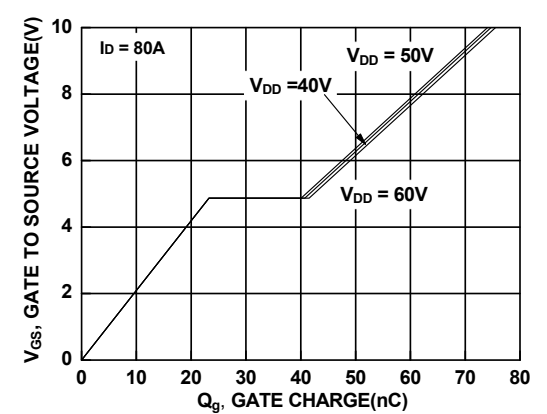
**Figure 13. Normalized Gate Threshold Voltage vs. Temperature**



**Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**



**Figure 15. Capacitance vs. Drain to Source Voltage**



**Figure 16. Gate Charge vs. Gate to Source Voltage**

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