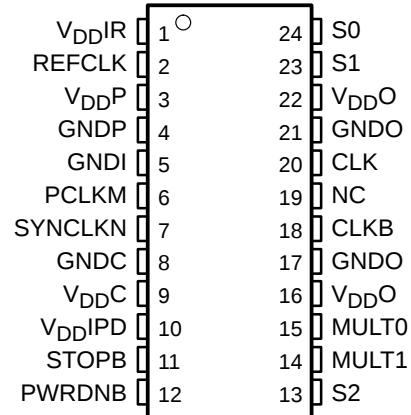


- 533-MHz Differential Clock Source for Direct Rambus™ Memory Systems for an 1066-MHz Data Transfer Rate
- Synchronizes the Clock Domains of the Rambus Channel With an External System or Processor Clock
- Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications
- Operates From a Single 3.3-V Supply and 120 mW at 300 MHz (Typ)
- Packaged in a Shrink Small-Outline Package (DBQ)
- Supports Frequency Multipliers: 4, 6, 8, 16/3
- No External Components Required for PLL
- Supports Independent Channel Clocking
- Spread Spectrum Clocking Tracking Capability to Reduce EMI
- Designed for Use With TI's 133-MHz Clock Synthesizers CDC924 and CDC921
- Cycle-Cycle Jitter Is Less Than 40 ps at 533 MHz
- Certified by Gigatest Labs to Exceed the Rambus DRCG Validation Requirement
- Supports Industrial Temperature Range of –40°C to 85°C

DBQ PACKAGE
(TOP VIEW)



NC – No internal connection

description

The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on a desktop, workstation, server, and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLKM = SYNCLKN, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLKM and SYNCLKN and adjusts the phase of BUSCLK such that the skew between PCLKM and SYNCLKN is minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 533 MHz with clock references ranging from 33 MHz to 100 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.

The CDCFR83 is characterized for operation over free-air temperatures of –40°C to 85°C.



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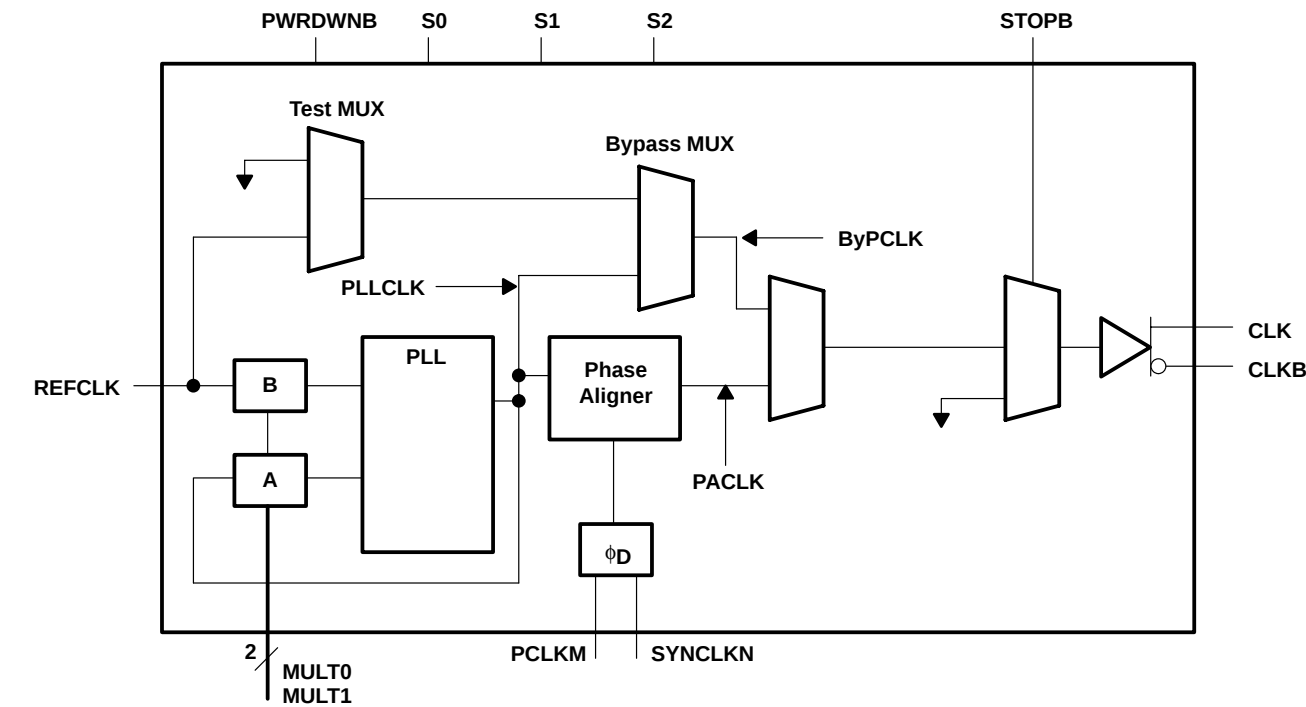
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CDCFR83
DIRECT RAMBUS™ CLOCK GENERATOR

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functional block diagram



FUNCTION TABLE†

MODE	S0	S1	S2	CLK	CLKB
Normal	0	0	0	Phase aligned clock	Phase aligned clock B
Bypass	1	0	0	PLLCLK	PLLCLKB
Test	1	1	0	REFCLK	REFCLKB
Output test (OE)	0	1	X	Hi-Z	Hi-Z
Reserved	0	0	1	—	—
Reserved	1	0	1	—	—
Reserved	1	1	1	Hi-Z	Hi-Z

† X = don't care, Hi-Z = high impedance

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	20	O	Output clock
CLKB	18	O	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	I	PLL multiplier select
MULT1	14	I	PLL multiplier select
NC	19		Not used
PCLKM	6	I	Phase detector input
PWRDNB	12	I	Active low power down
REFCLK	2	I	Reference clock
S0	24	I	Mode control
S1	23	I	Mode control
S2	13	I	Mode control
STOPB	11	I	Active low output disable
SYNCLKN	7	I	Phase detector input
V _{DDC}	9		V _{DD} for phase aligner
V _{DDIPD}	10		Reference voltage for phase detector inputs and STOPB
V _{DDIR}	1		Reference voltage for REFCLK
V _{DDO}	16, 22		V _{DD} for clock outputs
V _{DDP}	3		V _{DD} for PLL

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PLL divider selection

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 533 MHz) and (33 MHz < REFCLK < 100 MHz).

Table 1. REFCLK and BUSCLK Frequencies

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK (MHz)
0	0	67	4	267
0	1	50	6	300
0	1	67	6	400
1	1	33	8	267
1	1	50	8	400
1	1	67	8	533
1	0	67	16/3	356

Table 2. Clock Output Driver States

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	X	GND	GND
CLK stop	1	0	V _X , STOP	V _X , STOP
Normal	1	1	PACLK/PLLCLK/ REFCLK†	PACLB/PLLB/ REFCLKB

† Depending on the state of S0, S1, and S2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) –0.5 V to 4 V
 Output voltage range, V_O, at any output terminal –0.5 V to V_{DD} + 0.5 V
 Input voltage range, V_I, at any input terminal –0.5 V to V_{DD} + 0.5 V
 Continuous total power dissipation see Dissipation Rating Table
 Operating free-air temperature range, T_A –40°C to 85°C
 Storage temperature range, T_{stg} –65°C to 150°C
 Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C‡	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW	740 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3.135	3.3	3.465	V
High-level input voltage, V_{IH} (CMOS)	$0.7 \times V_{DD}$			V
Low-level input voltage, V_{IL} (CMOS)	$0.3 \times V_{DD}$			V
Initial phase error at phase detector inputs (required range for phase aligner)	$-0.5 \times t_{c(PD)}$ to $0.5 \times t_{c(PD)}$			
REFCLK low-level input voltage, V_{IL}	$0.3 \times V_{DDIR}$			V
REFCLK high-level input voltage, V_{IH}	$0.7 \times V_{DDIR}$			V
Input signal low voltage, V_{IL} (STOPB)	$0.3 \times V_{DDIPD}$			V
Input signal high voltage, V_{IH} (STOPB)	$0.7 \times V_{DDIPD}$			V
Input reference voltage for (REFCLK) (V_{DDIR})	1.235		3.465	V
Input reference voltage for (PCLKM and SYSCLKN) (V_{DDIPD})	1.235		3.465	V
High-level output current, I_{OH}			-16	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	-40		85	°C

timing requirements

	MIN	MAX	UNIT
Input cycle time, $t_{c(in)}$	10	40	ns
Input cycle-to-cycle jitter		250	ps
Input duty cycle over 10,000 cycles	40%	60%	
Input frequency modulation, f_{mod}	30	33	kHz
Modulation index, nonlinear maximum 0.5%		0.6%	
Phase detector input cycle time (PCLKM and SYNCLKN)	30	100	ns
Input slew rate, SR	1	4	V/ns
Input duty cycle (PCLKM and SYNCLKN)	25%	75%	

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V _{O(STOP)}	Output voltage during CLK Stop (STOPB = 0)		See Figure 1		1.1		2	
V _{O(X)}	Output crossing-point voltage		See Figure 1 and Figure 6		1.3		1.8	V
V _O	Output voltage swing		See Figure 1		0.4		0.6	V
V _{IK}	Input clamp voltage		V _{DD} = 3.135 V, I _I = –18 mA				–1.2	V
V _{OH}	High-level output voltage		See Figure 1				2	V
			V _{DD} = min to max, I _{OH} = –1 mA		V _{DD} – 0.1 V			
			V _{DD} = 3.135 V, I _{OH} = –16 mA		2.4			
V _{OL}	Low-level output voltage		See Figure 1		1			V
			V _{DD} = min to max, I _{OL} = 1 mA		0.1			
			V _{DD} = 3.135 V, I _{OL} = 16 mA		0.5			
I _{OH}	High-level output current		V _{DD} = 3.135 V, V _O = 1 V		–32	–52		mA
			V _{DD} = 3.3 V, V _O = 1.65 V		–51			
			V _{DD} = 3.465 V, V _O = 3.135 V		–14.5	–21		
I _{OL}	Low-level output current		V _{DD} = 3.135 V, V _O = 1.95 V		43	61.5		mA
			V _{DD} = 3.3 V, V _O = 1.65 V		65			
			V _{DD} = 3.465 V, V _O = 0.4 V		25.5	36		
I _{OZ}	High-impedance-state output current		S0 = 0, S1 = 1				±10	μA
I _{OZ(STOP)}	High-impedance-state output current during CLK stop		Stop = 0, V _O = GND or V _{DD}				±100	μA
I _{OZ(PD)}	High-impedance-state output current in power-down state		PWRDNB = 0, V _O = GND or V _{DD}		–10		100	μA
I _{IH}	High-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V _{DD} = 3.465 V, V _I = V _{DD}				10	μA
		PWRDNB, S0, S1, S2, MULT0, MULT1	V _{DD} = 3.465 V, V _I = V _{DD}				10	
I _{IL}	Low-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V _{DD} = 3.465 V, V _I = 0				–10	μA
		PWRDNB, S0, S1, S2, MULT0, MULT1	V _{DD} = 3.465 V, V _I = 0				–10	
Z _O	Output impedance	High state	R _I at I _O –14.5 mA to –16.5 mA		15	35	50	Ω
		Low state	R _I at I _O 14.5 mA to 16.5 mA		11	17	35	
	Reference current	V _{DD} I _R , V _{DD} I _{PD}	V _{DD} = 3.465 V	PWRDNB = 0			50	μA
				PWRDNB = 1			0.5	mA
C _I	Input capacitance		V _I = V _{DD} or GND		2			pF
C _O	Output capacitance		V _O = V _{DD} or GND		3			pF
I _{DD(PD)}	Supply current in power-down state		REFCLK = 0 MHz to 100 MHz, PWDNB = 0, STOPB = 1				100	μA
I _{DD(CLKSTOP)}	Supply current in CLK stop state		BUSCLK configured for 533 MHz				45	mA
I _{DD(NORMAL)}	Supply current in normal state		BUSCLK = 533 MHz				100	mA

† V_{DD} refers to any of the following; V_{DD}, V_{DD}I_{PD}, V_{DD}I_R, V_{DD}O, V_{DD}C, and V_{DD}P

‡ All typical values are at V_{DD} = 3.3 V, T_A = 25°C.



switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _{c(out)}	Clock output cycle time				1.87		3.75	ns
t _(jitter)	Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles	Infinite and stopped phase alignment	267 MHz	See Figure 3			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
			533 MHz§				40	
t _(phase)	Phase detector phase error for distributed loop			Static phase error [‡]	–100		100	ps
t _(phase, SSC)	PLL output phase error when tracking SSC			Dynamic phase error [‡]	–100		100	ps
t _(DC)	Output duty cycle over 10,000 cycles			See Figure 4	45%		55%	
t _(DC, err)	Output cycle-to-cycle duty cycle error	Infinite and stopped phase alignment	267 MHz	See Figure 5			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
			533 MHz				50	
t _r , t _f	Output rise and fall times (measured at 20%–80% of output voltage)			See Figure 7	160		400	ps
Δt	Difference between rise and fall times on a single device (20%–80%) t _f – t _r			See Figure 7			100	ps

[†] All typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Assured by design

[§] Jitter measurement according to Rambus validation specification

state transition latency specifications

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB $\uparrow$ to CLK/CLKB output settled (excluding $t_{(DISTLOCK)}$)	Powerdown	Normal	See Figure 8			3	ms
	Delay time, PWRDNB $\uparrow$ to internal PLL and clock are on and settled						3	
$t_{(VDDpowerup)}$	Delay time, power up to CLK/CLKB output settled	V_{DD}	Normal	See Figure 8			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLK/CLKB output resettled (excluding $t_{(DISTLOCK)}$)	Normal	Normal	See Figure 9			1	ms
$t_{(CLKON)}$	STOPB $\uparrow$ to CLK/CLKB glitch-free clock edges	CLK Stop	Normal	See Figure 10			10	ns
$t_{(CLKSETL)}$	STOPB $\uparrow$ to CLK/CLKB output settled to within 50 ps of the phase before STOPB was disabled	CLK Stop	Normal	See Figure 10			20	cycles
$t_{(CLKOFF)}$	STOPB $\downarrow$ to CLK/CLKB output disabled	Normal	CLK Stop	See Figure 10			5	ns

[†] All typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

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state transition latency specifications (continued)

PARAMETER	FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(\text{powerdown})}$	Normal	Powerdown	See Figure 8			1	ms
$t_{(\text{STOP})}$	STOPB	Normal	See Figure 10			100	μs
$t_{(\text{ON})}$	Normal	CLK stop	See Figure 10	100			ms
$t_{(\text{DISTLOCK})}$	Unlocked	Locked				5	ms

† All typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION

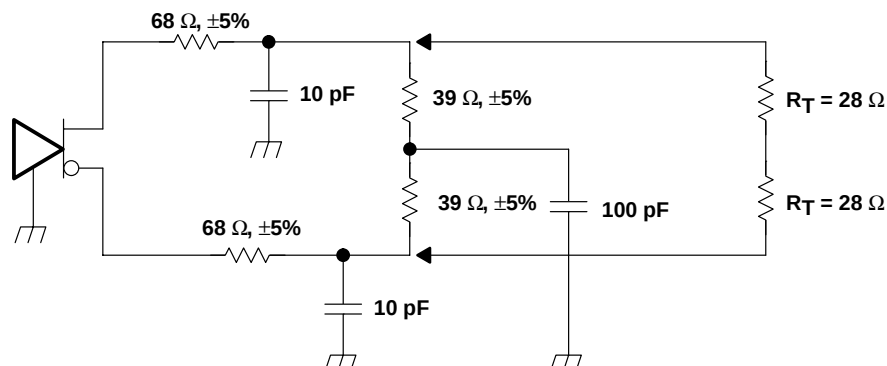
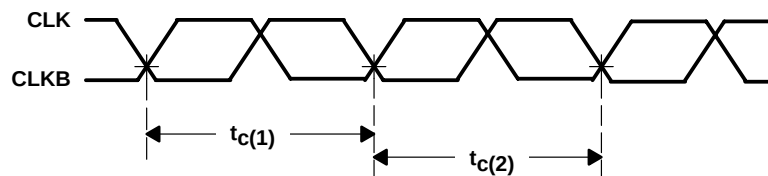


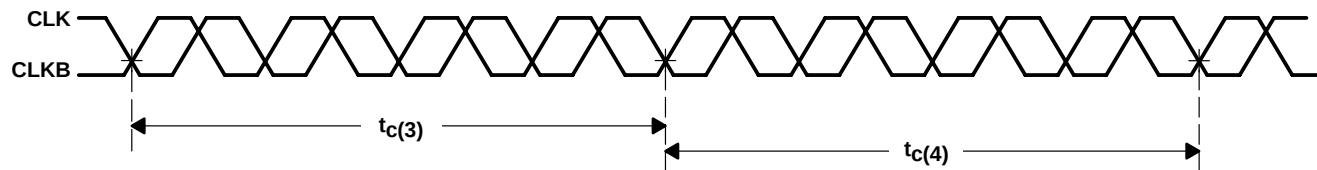
Figure 1. Test Load and Voltage Definitions ($V_{O(\text{STOP})}$, $V_{O(X)}$, V_O , V_{OH} , V_{OL})



Cycle-to-cycle jitter = $|t_{c(1)} - t_{c(2)}|$ over 10000 consecutive cycles

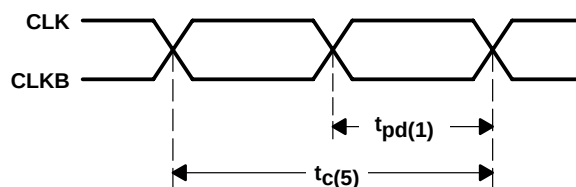
Figure 2. Cycle-to-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION



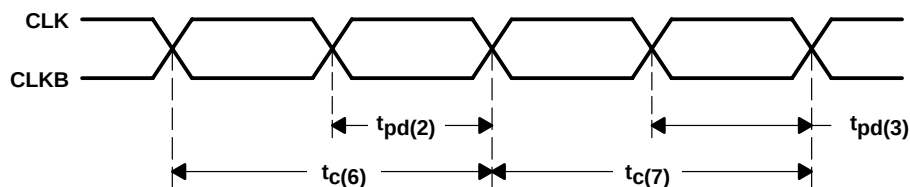
Cycle-to-cycle jitter = $|t_{c(3)} - t_{c(4)}|$ over 10000 consecutive cycles

Figure 3. Short Term Cycle-to-Cycle Jitter Over Four Cycles



Duty cycle = $(t_{pd(1)}/t_{c(5)})$

Figure 4. Output Duty Cycle



Duty cycle error = $t_{pd(2)} - t_{pd(3)}$

Figure 5. Duty Cycle Error (Cycle-to-Cycle)

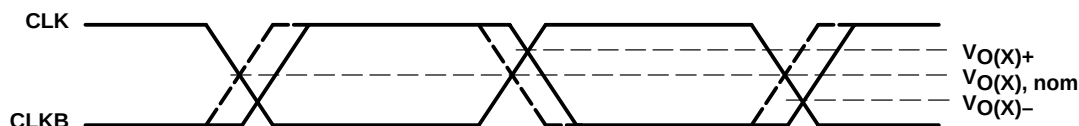


Figure 6. Crossing-Point Voltage



Figure 7. Voltage Waveforms

The diagram shows two signals over time. The top signal, PWRDNB, is a pulse that transitions from low to high and then back to low. The bottom signal, CLK/CLKB, is a periodic square wave. The period of the clock is indicated by a double-headed arrow labeled $t_{(power\ up)}$ during the high phase of PWRDNB. The period of the clock is also indicated by a double-headed arrow labeled $t_{(power\ down)}$ during the low phase of PWRDNB. The clock signal is shown as a continuous wave during the high phase of PWRDNB and as a shaded area during the low phase of PWRDNB.

The diagram shows the relationship between the STOPB signal and the CLK/CLKB signal. The STOPB signal is high for a duration $t_{(ON)}$ and then transitions to low for a duration $t_{(STOP)}$. The CLK/CLKB signal is a square wave that is enabled when STOPB is high. The timing parameters are defined as follows:

- $t_{(ON)}$: Duration of the STOPB signal being high.
- $t_{(STOP)}$: Duration of the STOPB signal being low.
- $t_{(CLKSETL)}$: Time from the rising edge of STOPB to the first rising edge of CLK/CLKB.
- $t_{(CLKON)}$ (see Note A): Duration of the CLK/CLKB signal being high.
- $t_{(CLKOFF)}$ (see Note A): Time from the falling edge of STOPB to the last falling edge of CLK/CLKB.

Annotations for the CLK/CLKB signal:

- Output clock not specified glitches ok: Points to the initial rising edge of the clock signal.
- Clock enabled and glitch free: Points to the period of the clock signal during which STOPB is high.
- Clock output settled within 50 ps of the phase before disabled: Points to the final falling edge of the clock signal.

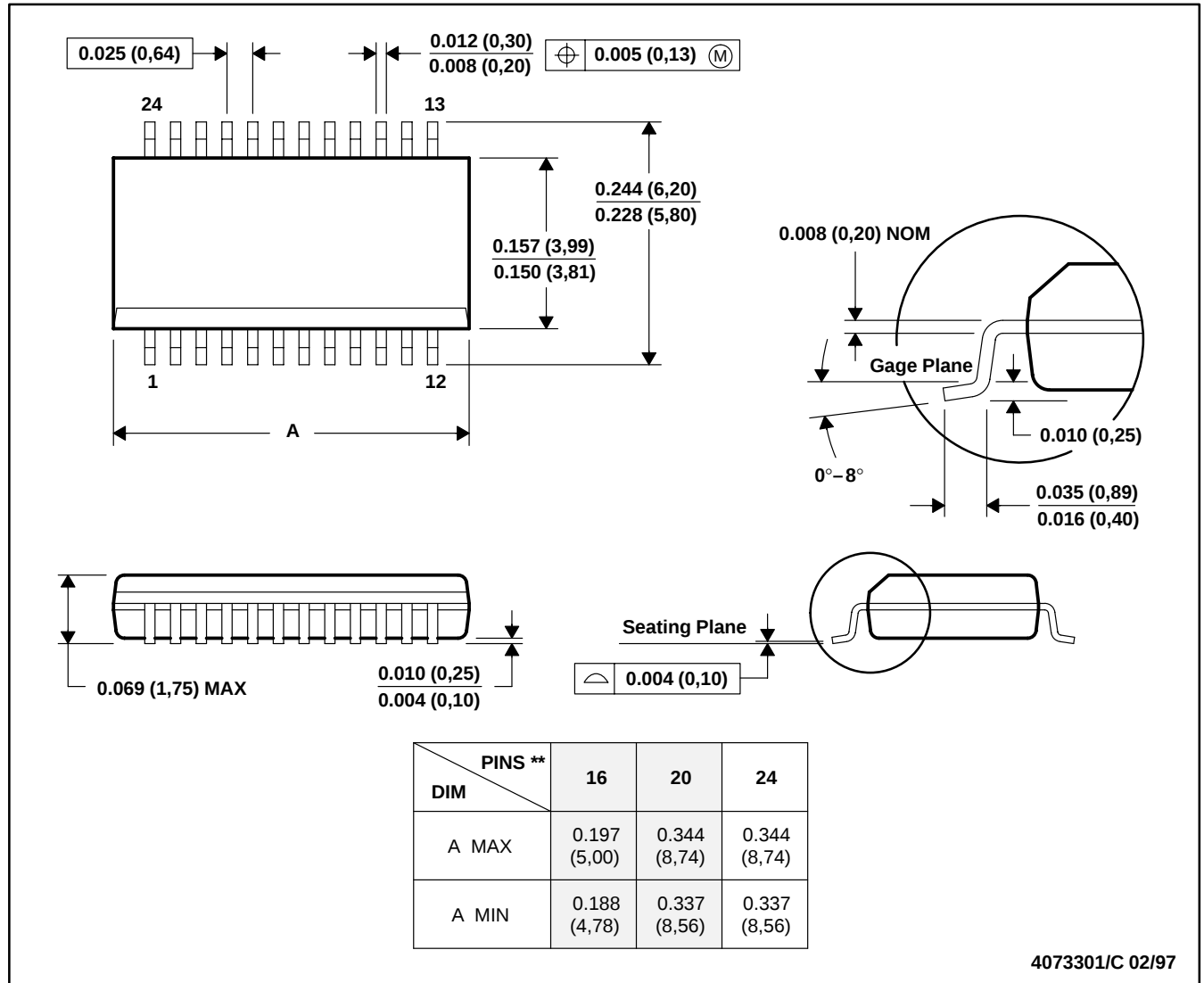
Figure 10. STOPB Transition Timings

MECHANICAL DATA

DBQ (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

24-PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-137

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Mailing Address:

Texas Instruments
Post Office Box 655303
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.