



Rev.3.0

AS7C316098B-10TIN AS7C316098B-10BIN

1024K X 16 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

| <u>Revision</u> | <u>Description</u> | <u>Issue Date</u> |
|-----------------|---|-------------------|
| Rev. 1.0 | Initial Issued | June 2014 |
| Rev. 2.0 | Modified page5 "AC ELECTRICAL CHARACTERISTIC" We can offer special screened part "tested and passed for 8ns@ 25°C yield - shown with custom label on packaging as AS7C316098B-10TIN" | November 2017 |
| Rev. 3.0 | Added 48-ball TFBGA package as AS7C316098B-10BIN | July 2018 |

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Alliance Memory Inc. reserves the right to change products or specification without notice



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FEATURES

- Fast access time : 10ns
- **low power consumption:**
Operating current : 70mA (TYP.)
Standby current : 4mA(TYP.)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data byte control : LB# (DQ0 ~ DQ7)
UB# (DQ8 ~ DQ15)
- Data retention voltage : 1.5V (MIN.)
- **All parts are ROHS Compliant**
- Package : 54-pin 400 mil TSOP-II
48-ball 6mm x 8mm TFBGA

GENERAL DESCRIPTION

The AS7C316098B is a 16M-bit high speed CMOS static random access memory organized as 1024K words by 16 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C316098B operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

Table 1. Speed Grade Information

| Product Family | Vcc Range | Speed | Power Dissipation | |
|----------------|------------|-------|---------------------------------|----------------------------------|
| | | | Standby(I _{SB1} ,TYP.) | Operating(I _{CC} ,TYP.) |
| AS7C316098B | 2.7 ~ 3.6V | 10ns | 4mA | 70mA |

Table 2. Ordering Information

| Product part No | Org | Temperature | Package |
|-------------------|------------|--------------------------|-----------------------|
| AS7C316098B-10BIN | 1024K x 16 | Industrial -40°C to 85°C | 48-ball TFGBA |
| AS7C316098B-10TIN | 1024K x 16 | Industrial -40°C to 85°C | 54-pin 400mil TSOP-II |

Please note: we can also offer a custom part - 'specially screened' part at 8ns at 25°C defined by specific labeling on package as AS7C316098B-10TIN*

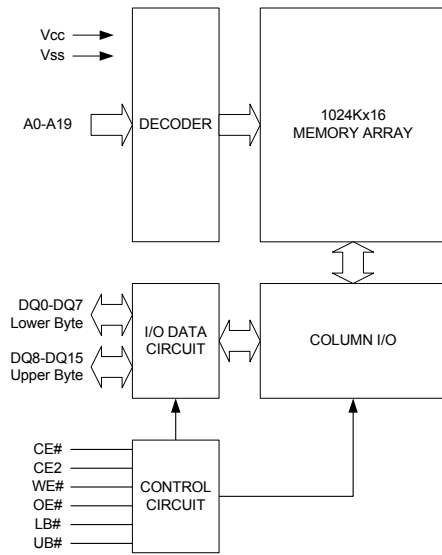


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FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| SYMBOL | DESCRIPTION |
|------------|---------------------|
| A0 - A19 | Address Inputs |
| DQ0 - DQ15 | Data Inputs/Outputs |
| CE#, CE2 | Chip Enable Input |
| WE# | Write Enable Input |
| OE# | Output Enable Input |
| LB# | Lower Byte Control |
| UB# | Upper Byte Control |
| Vcc | Power Supply |
| Vss | Ground |

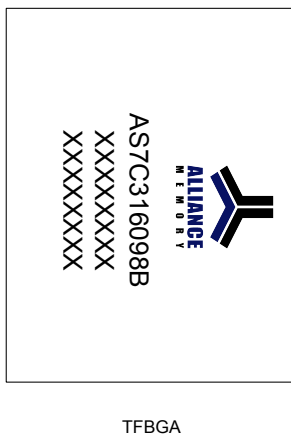
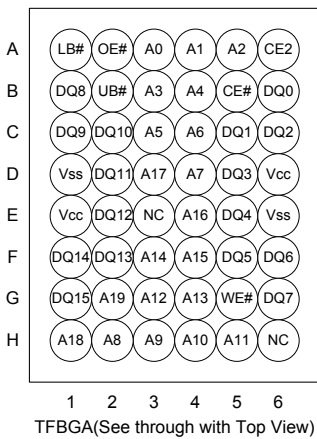
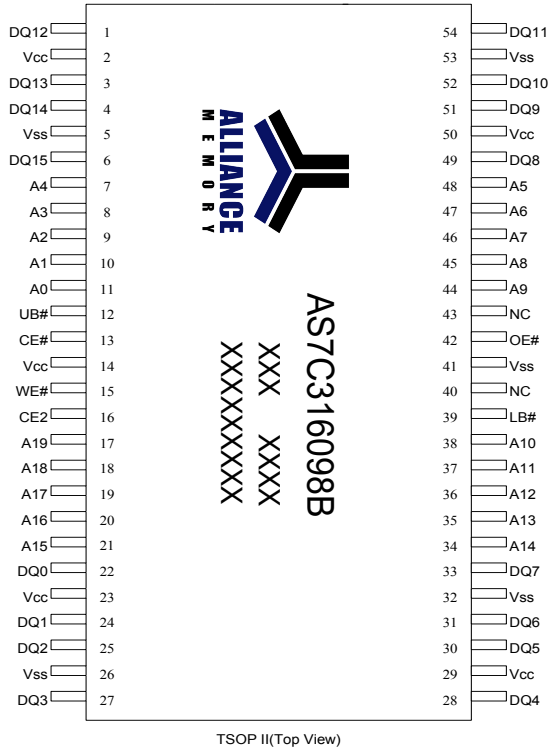


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PIN CONFIGURATION





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ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | SYMBOL | RATING | UNIT |
|--|-----------|--------------------|------|
| Voltage on Vcc relative to Vss | V_{T1} | -0.5 to 4.6 | V |
| Voltage on any other pin relative to Vss | V_{T2} | -0.5 to Vcc+0.5 | V |
| Operating Temperature | T_A | -40 to 85(I grade) | °C |
| Storage Temperature | T_{STG} | -65 to 150 | °C |
| Power Dissipation | P_D | 1 | W |
| DC Output Current | I_{OUT} | 50 | mA |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

| MODE | CE# | CE2 | OE# | WE# | LB# | UB# | I/O OPERATION | | SUPPLY CURRENT |
|----------------|-----|-----|-----|-----|-----|-----|---------------|-----------|----------------|
| | | | | | | | DQ0-DQ7 | DQ8-DQ15 | |
| Standby | H | X | X | X | X | X | High - Z | High - Z | I_{SB1} |
| | X | L | X | X | X | X | High - Z | High - Z | |
| Output Disable | L | H | H | H | L | X | High - Z | High - Z | I_{CC} |
| | L | H | H | H | X | L | High - Z | High - Z | |
| Read | L | H | L | H | L | H | D_{OUT} | High - Z | I_{CC} |
| | L | H | L | H | H | L | High - Z | D_{OUT} | |
| | L | H | L | H | L | L | D_{OUT} | D_{OUT} | |
| Write | L | H | X | L | L | H | D_{IN} | High - Z | I_{CC} |
| | L | H | X | L | H | L | High - Z | D_{IN} | |
| | L | H | X | L | L | L | D_{IN} | D_{IN} | |

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS (Vcc=2.7V 3.6V)

| PARAMETER | SYM. | TEST CONDITION | MIN. | TYP. ⁴ | MAX. | UNIT | |
|--|----------------|--|-------|-------------------|--------------|---------|----|
| Supply Voltage | V_{CC} | | 2.7 | 3.3 | 3.6 | V | |
| Input High Voltage | $V_{IH}^{1,2}$ | | 2.2 | - | $V_{CC}+0.3$ | V | |
| Input Low Voltage | V_{IL}^{2} | | - 0.3 | - | 0.8 | V | |
| Input Leakage Current | I_{LI} | $V_{CC} \geq V_{IN} \geq V_{SS}$ | - 1 | - | 1 | μA | |
| Output Leakage Current | I_{LO} | $V_{CC} \geq V_{OUT} \geq V_{SS}$, Output Disabled | - 1 | - | 1 | μA | |
| Output High Voltage | V_{OH} | $I_{OH} = -4mA$ | 2.4 | - | - | V | |
| Output Low Voltage | V_{OL} | $I_{OL} = 8mA$ | - | - | 0.4 | V | |
| Average Operating Power supply Current | I_{CC} | CE# $\leq 0.2V$ and CE2 $\geq V_{CC}-0.2V$, other pins at 0.2V or $V_{CC}-0.2V$, $I_{IO} = 0mA$; f=max. | -10 | - | 70 | 120 | mA |
| Standby Power Supply Current | I_{SB1} | CE# $\geq V_{CC} - 0.2V$; other pins at 0.2V or $V_{CC}-0.2V$. | - | 4 | 40 | mA | |

Notes:

- $V_{IH(MAX)} = V_{CC} + 2.0V$ for pulse width less than 6ns.
- $V_{IL(MIN)} = V_{SS} - 2.0V$ for pulse width less than 6ns.
- Over/Undershoot specifications are characterized on engineering evaluation stage, not for mass production test.
- Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at $V_{CC} = V_{CC(TYP)}$ and $T_A = 25^\circ C$



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CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

| PARAMETER | SYMBOL | MIN. | MAX | UNIT |
|--------------------------|-----------|------|-----|------|
| Input Capacitance | C_{IN} | - | 8 | pF |
| Input/Output Capacitance | $C_{I/O}$ | - | 10 | pF |

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

| | |
|--|--|
| speed | 10ns |
| Input Pulse Levels | 0.2V to $V_{CC}-0.2V$ |
| Input Rise and Fall Times | 3ns |
| Input and Output Timing Reference Levels | $V_{CC}/2$ |
| Output Load | $C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -8\text{mA}/4\text{mA}$ |

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=2.7V$ 3.6V)

(1) READ CYCLE

| PARAMETER | SYM. | AS7C316098B-10 | | Special Screened to -8 | | UNIT |
|------------------------------------|-------------|----------------|------|------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Read Cycle Time | t_{RC} | 10 | - | 8 | - | ns |
| Address Access Time | t_{AA} | - | 10 | - | 8 | ns |
| Chip Enable Access Time | t_{ACE} | - | 10 | - | 8 | ns |
| Output Enable Access Time | t_{OE} | - | 4.5 | - | 4.5 | ns |
| Chip Enable to Output in Low-Z | t_{CLZ}^* | 2 | - | 2 | - | ns |
| Output Enable to Output in Low-Z | t_{OLZ}^* | 0 | - | 0 | - | ns |
| Chip Disable to Output in High-Z | t_{CHZ}^* | - | 4 | - | 3 | ns |
| Output Disable to Output in High-Z | t_{OHZ}^* | - | 4 | - | 3 | ns |
| Output Hold from Address Change | t_{OH} | 2 | - | 2 | - | ns |
| LB#, UB# Access Time | t_{BA} | - | 4.5 | - | 4.5 | ns |
| LB#, UB# to High-Z Output | t_{BHZ}^* | - | 4 | - | 3 | ns |
| LB#, UB# to Low-Z Output | t_{BLZ}^* | 0 | - | 0 | - | ns |

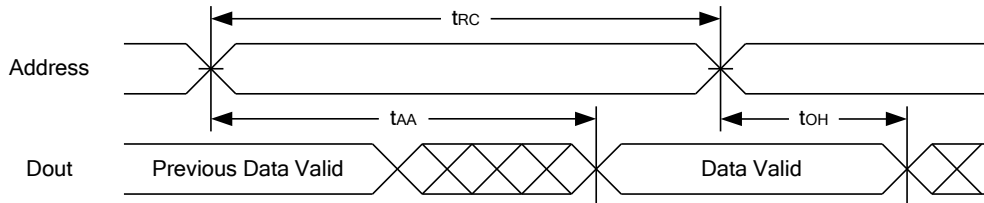
(2) WRITE CYCLE

| PARAMETER | SYM. | AS7C316098B-10 | | Special Screened to -8 | | UNIT |
|----------------------------------|-------------|----------------|------|------------------------|------|------|
| | | MIN. | MAX. | MIN. | MAX. | |
| Write Cycle Time | t_{WC} | 10 | - | 8 | - | ns |
| Address Valid to End of Write | t_{AW} | 8 | - | 6.5 | - | ns |
| Chip Enable to End of Write | t_{CW} | 8 | - | 6.5 | - | ns |
| Address Set-up Time | t_{AS} | 0 | - | 0 | - | ns |
| Write Pulse Width | t_{WP} | 8 | - | 6.5 | - | ns |
| Write Recovery Time | t_{WR} | 0 | - | 0 | - | ns |
| Data to Write Time Overlap | t_{DW} | 6 | - | 5 | - | ns |
| Data Hold from End of Write Time | t_{DH} | 0 | - | 0 | - | ns |
| Output Active from End of Write | t_{OW}^* | 2 | - | 2 | - | ns |
| Write to Output in High-Z | t_{WHZ}^* | - | 4 | - | 3 | ns |
| LB#, UB# Valid to End of Write | t_{BW} | 8 | - | 6.5 | - | ns |

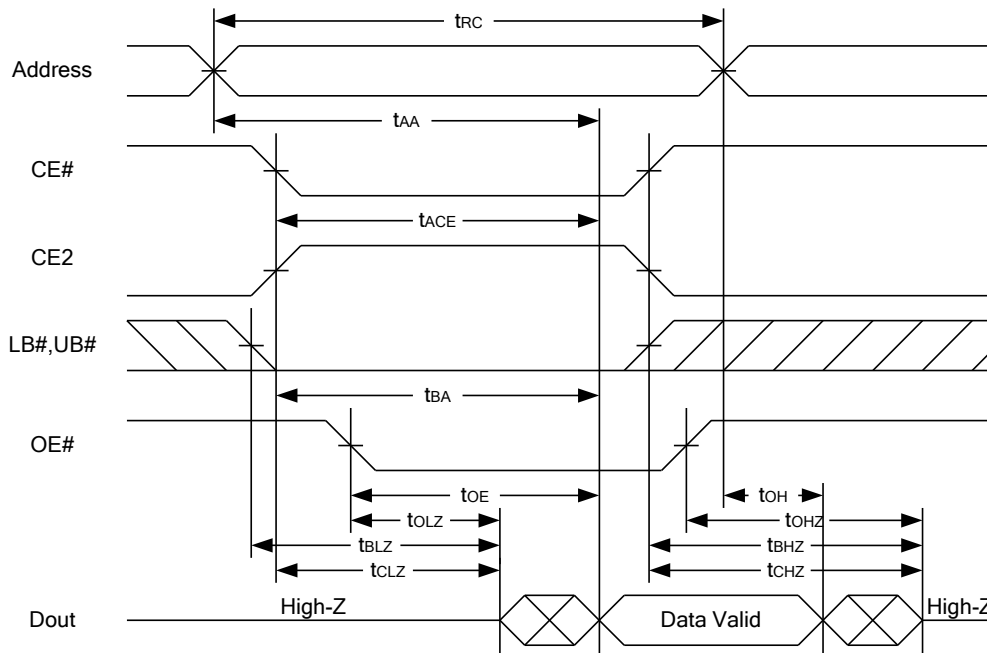
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)



Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low, CE2 = high, LB# or UB# = low.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high, LB# or UB# = low transition; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{BLZ} , t_{OLZ} , t_{CHZ} , t_{BHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{BHZ} is less than t_{BLZ} , t_{OHZ} is less than t_{OLZ} .

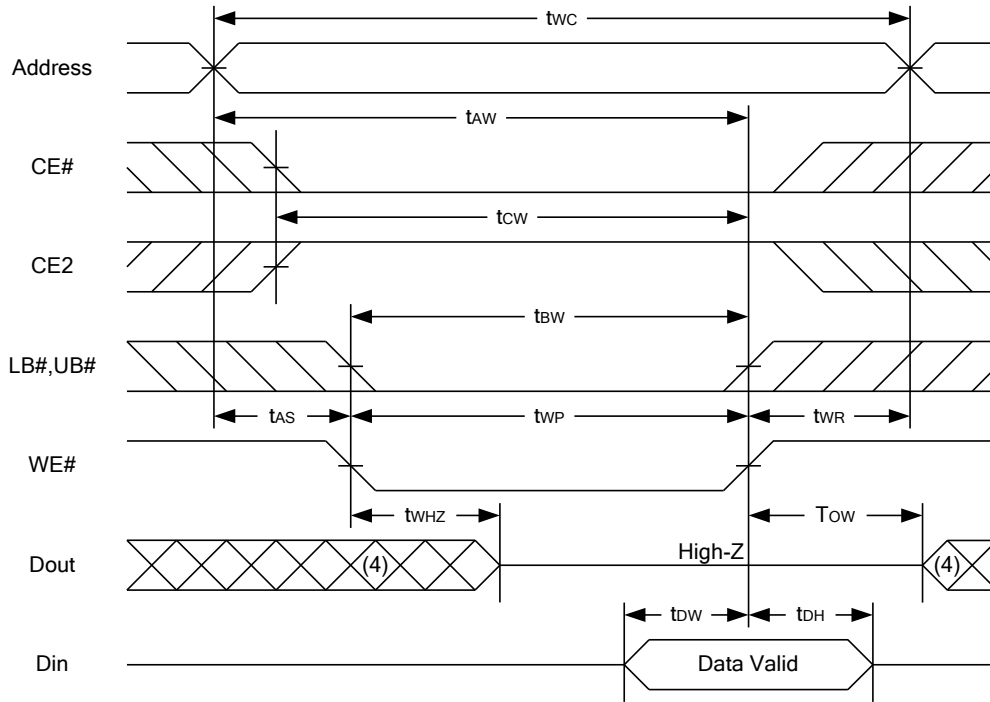


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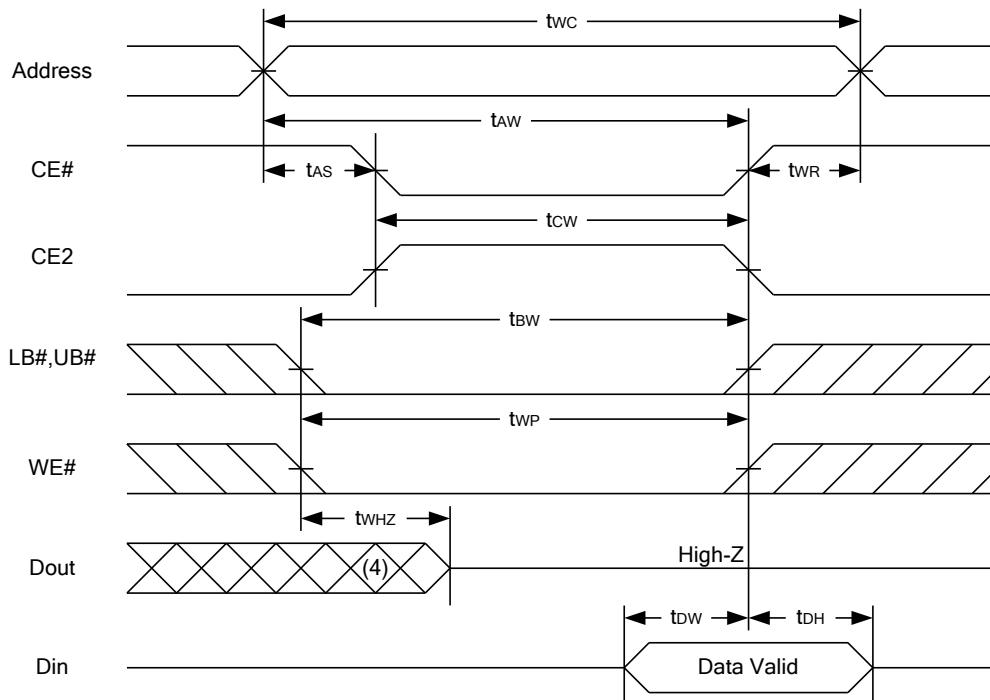
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WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)



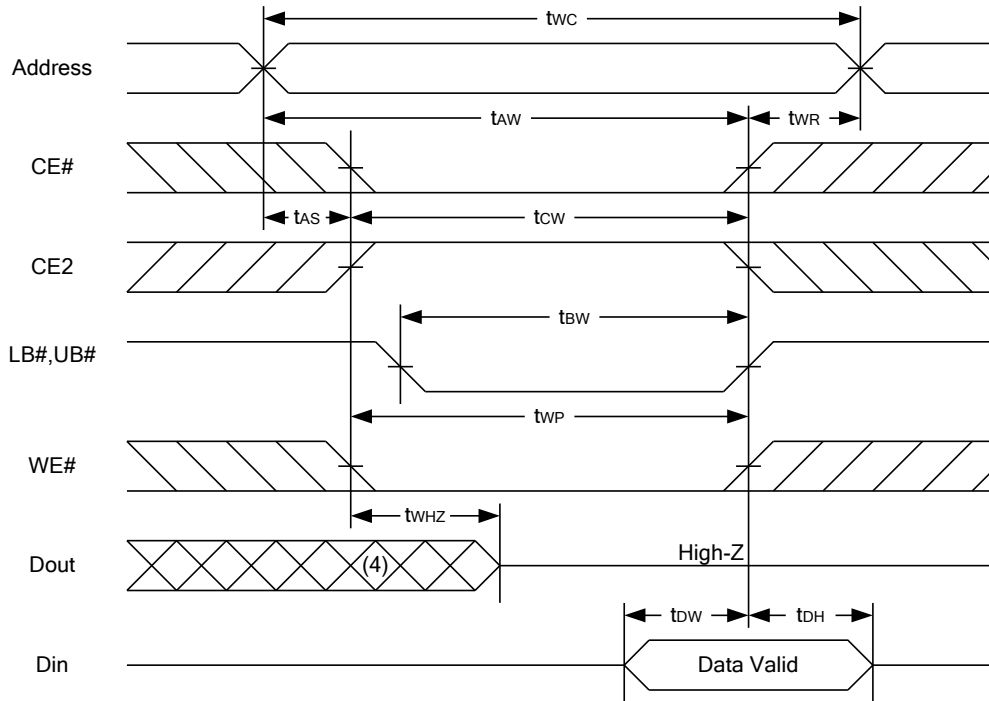


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WRITE CYCLE 3 (LB#,UB# Controlled) (1,2,5,6)



Notes :

1. WE#, CE#, LB#, UB# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#, LB# or UB# = low.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{OW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE#, LB#, UB# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



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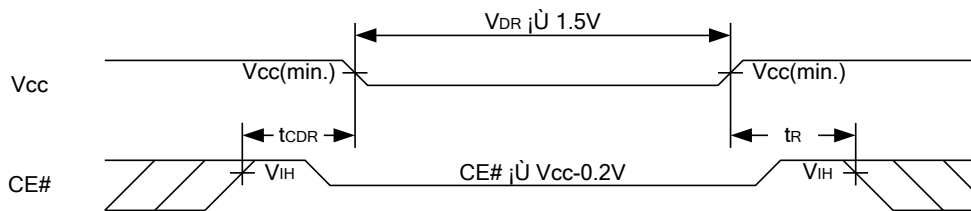
DATA RETENTION CHARACTERISTICS

| PARAMETER | SYMBOL | TEST CONDITION | MIN. | TYP. | MAX. | UNIT |
|-------------------------------------|------------------|--|------------------|------|------|------|
| V _{CC} for Data Retention | V _{DR} | CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V | 1.5 | - | 3.6 | V |
| Data Retention Current | I _{DR} | V _{CC} = 1.5V CE# ≥ V _{CC} - 0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V | - | 4 | 40 | mA |
| Chip Disable to Data Retention Time | t _{CDR} | See Data Retention Waveforms (below) | 0 | - | - | ns |
| Recovery Time | t _R | | t _{RC*} | - | - | ns |

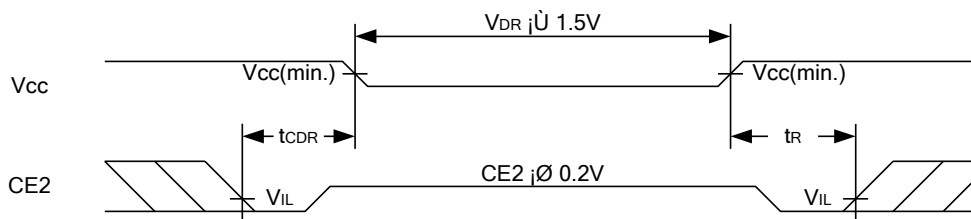
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

Low V_{CC} Data Retention Waveform (1) (CE# controlled)

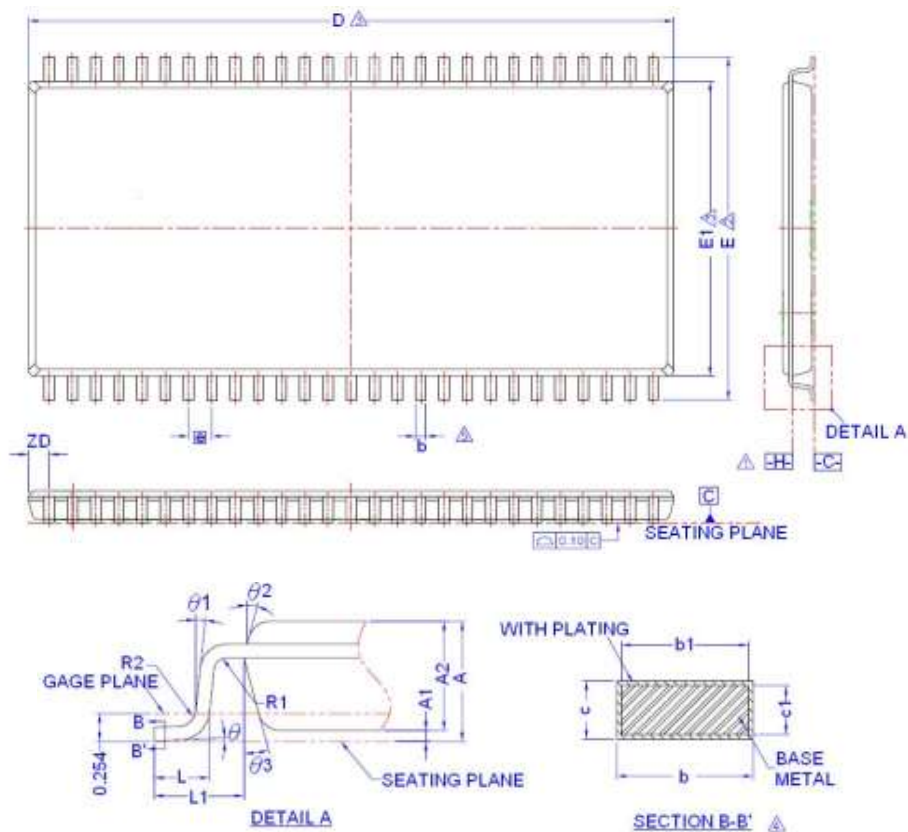


Low V_{CC} Data Retention Waveform (2) (CE2 controlled)



PACKAGE OUTLINE DIMENSION

54-pin 400 mil TSOP-II Package Outline Dimension

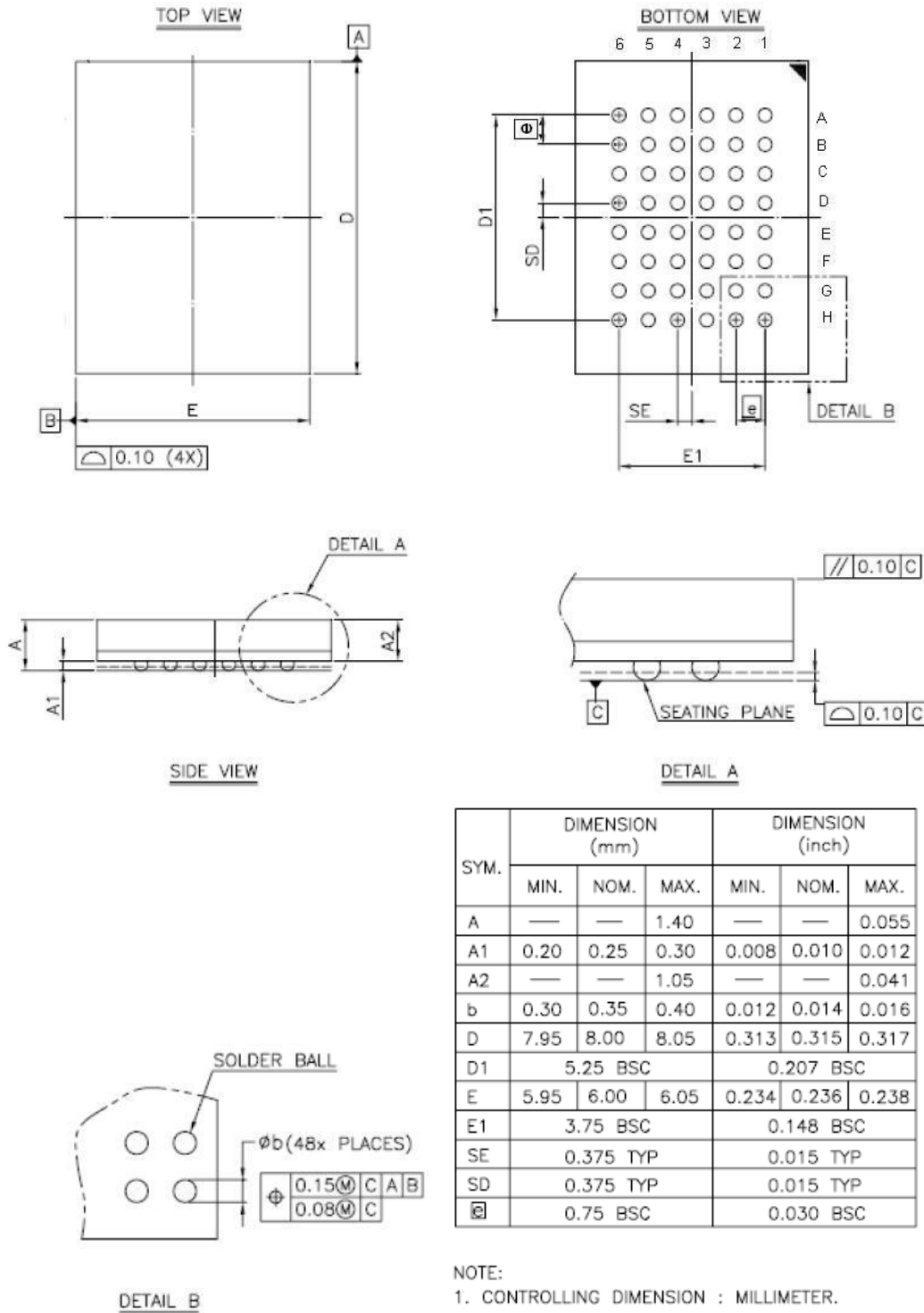


| SYM. | DIMENSION (MM) | | | DIMENSION (INCH) | | |
|------|----------------|-------|------|------------------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | - | - | 1.20 | - | - | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| b | 0.30 | - | 0.45 | 0.012 | - | 0.018 |
| b1 | 0.30 | 0.35 | 0.40 | 0.012 | 0.014 | 0.016 |
| e | 0.12 | - | 0.21 | 0.005 | - | 0.008 |
| c1 | 0.10 | 0.127 | 0.16 | 0.004 | 0.005 | 0.006 |
| D | 22.22 BSC | | | 0.875 BSC | | |
| ZD | 0.71 REF | | | 0.028 REF | | |
| E | 11.76 BSC | | | 0.463 BSC | | |
| E1 | 10.16 BSC | | | 0.400 BSC | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | 0.80 REF | | | 0.031 REF | | |
| ⌀ | 0.80 BSC | | | 0.031 BSC | | |
| R1 | 0.12 | - | - | 0.005 | - | - |
| R2 | 0.12 | - | 0.25 | 0.005 | - | 0.010 |
| θ | 0° | - | 8° | 0° | - | 8° |
| θ1 | 0° | - | - | 0° | - | - |
| θ2 | 10° | 15° | 20° | 10° | 15° | 20° |
| θ3 | 10° | 15° | 20° | 10° | 15° | 20° |

NOTE:

- DATUM PLANE \square COINCIDENT WITH BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
- TO BE DETERMINED AT SEATING PLANE \square .
- DIMENSION D AND E1 ARE DETERMINED AT DATUM \square .
DIMENSION D DOES NOT INCLUDE MOLD PROTRUSIONS OR GATE BURRS. MOLD PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
DIMENSION E1 DOES NOT INCLUDE INTERLEAD MOLD PROTRUSIONS. INTERLEAD MOLD PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
- CONTROLLING DIMENSION: MILLIMETER.
- REFER TO JEDEC STD MS-024, FA.

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1024K X 16 BIT HIGH SPEED CMOS SRAM
48-ball 6mm × 8mm TFBGA Package Outline Dimension




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PART NUMBERING SYSTEM

| AS7C | 316098B | 10 | T/B | I | N |
|------|--|----------|--------------------------------|-------------------------------|--|
| SRAM | 3=3.3V 16098=1Mx16 B= B die option | 10 =10ns | T= 54-pin 400mil TSOP-II | I=Industrial -40°C to 85°C | Indicates Pb and Halogen Free & ROHS Compliant |
| | | | B=48-ball TFBGA | | |

Please note: we can also offer a custom part - 'specially screened' part at 8ns at 25°C defined by specific labeling on package as AS7C316098B-10TIN*



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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