## Data Sheet

## FEATURES

Fully specified rail to rail at $\mathrm{V}_{\mathrm{ccI}}=2.5 \mathrm{~V}$ to 5.5 V
Input common-mode voltage from -0.2 V to $\mathrm{V}_{\mathrm{cc}}+\mathbf{0 . 2} \mathrm{V}$
Low glitch LVDS-compatible output stage
Propagation delay: 1.6 ns
Power dissipation: 37 mW at 2.5 V
Shutdown pin
Single-pin control for programmable hysteresis and latch
Power supply rejection > 60 dB
$-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ operation

## APPLICATIONS

High speed instrumentation
Clock and data signal restoration
Logic level shifting or translation
Pulse spectroscopy
High speed line receivers
Threshold detection
Peak and zero-crossing detectors
High speed trigger circuitry
Pulse-width modulators
Current-/voltage-controlled oscillators
Automatic test equipment (ATE)
Qualified for automotive applications

## GENERAL DESCRIPTION

The AD8465 is a very fast comparator fabricated on the Analog Devices, Inc., proprietary XFCB2 process. This comparator is exceptionally versatile and easy to use. Features include an input range from $\mathrm{V}_{\mathrm{EE}}-0.5 \mathrm{~V}$ to $\mathrm{V}_{\mathrm{CCI}}+0.2 \mathrm{~V}$, low noise, LVDScompatible output drivers, and TTL/CMOS latch inputs with adjustable hysteresis and/or shutdown inputs.
The device offers 1.6 ns propagation delay with 1 ps rms random jitter (RJ). Overdrive and slew rate dispersion are typically less than 50 ps .


Figure 1.

A flexible power supply scheme allows the devices to operate with a single 2.5 V positive supply and a -0.5 V to +2.7 V input signal range up to a 5.5 V positive supply with a -0.5 V to +5.7 V input signal range. Split input/output supplies, with no sequencing restrictions, support a wide input signal range with greatly reduced power consumption.
The LVDS-compatible output stage is designed to drive any standard LVDS input. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. High speed latch and programmable hysteresis features are also provided in a unique single-pin control option.

The AD8465 is available in a 12 -lead LFCSP.

Rev. B
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## TABLE OF CONTENTS

Features 1Applications ..... 1
Functional Block Diagram .....  1
General Description .....  1
Revision History ..... 2
Specifications ..... 3
Electrical Characteristics ..... 3
Timing Information ..... 5
Absolute Maximum Ratings ..... 6
Thermal Resistance ..... 6
ESD Caution ..... 6
Pin Configuration and Function Descriptions ..... 7
Typical Performance Characteristics .....  8
REVISION HISTORY
12/14-Rev. A to Rev. B
Changes to Applications Section ..... 1
Changes to Table 4 ..... 6
Changes to Figure 3 and Table 5 ..... 7
Changes to Figure 26 ..... 14
Updated Outline Dimensions ..... 14
Changes to Ordering Guide ..... 14
Added Automotive Products Section ..... 14
11/11-Rev. 0 to Rev. A
Changed $\mathrm{V}_{\text {IL }}=0.4 \mathrm{~V}$ to $\mathrm{V}_{\text {IL }}=0.8 \mathrm{~V}$ in Conditions of IIL ,
Table 13
Application Information ..... 10
Power/Ground Layout and Bypassing ..... 10
LVDS-Compatible Output Stage ..... 10
Using/Disabling the Latch Feature ..... 10
Optimizing Performance ..... 10
Comparator Propagation Delay Dispersion ..... 11
Comparator Hysteresis ..... 11
Crossover Bias Points ..... 12
Minimum Input Slew Rate Requirement ..... 12
Typical Application Circuits ..... 13
Outline Dimensions ..... 14
Ordering Guide ..... 14
Automotive Products ..... 14

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## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CCO}}=2.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$, typical at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.
Table 1.

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| DC INPUT CHARACTERISTICS <br> Voltage Range <br> Common-Mode Range <br> Differential Voltage <br> Offset Voltage <br> Bias Current <br> Offset Current <br> Capacitance <br> Resistance, Differential Mode <br> Resistance, Common Mode <br> Active Gain <br> Common-Mode Rejection Ratio <br> Hysteresis | $V_{p}, V_{N}$ <br> Vos <br> $\mathrm{I}_{\mathrm{p},} \mathrm{I}_{\mathrm{N}}$ <br> $C_{p}, C_{N}$ <br> $A_{v}$ <br> CMRR | $\begin{aligned} & \mathrm{V}_{\mathrm{Cl}}=2.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{cl}}=2.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{cl}}=2.5 \mathrm{~V} \text { to } 5.5 \mathrm{~V} \end{aligned}$ $\begin{aligned} & -0.1 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{ccl}} \\ & -0.5 \mathrm{~V} \text { to } \mathrm{V}_{\mathrm{cl}}+0.5 \mathrm{~V} \end{aligned}$ $\begin{aligned} & \mathrm{V}_{\mathrm{CCI}}=2.5 \mathrm{~V}, \mathrm{~V}_{\text {CCO }}=2.5 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{CM}}=-0.2 \mathrm{~V} \text { to }+2.7 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{CCI}}=2.5 \mathrm{~V}, \mathrm{~V}_{\text {CCO }}=5.0 \mathrm{~V} \\ & R_{\text {HYS }}=\infty \end{aligned}$ | $\begin{aligned} & -0.5 \\ & -0.2 \\ & -5.0 \\ & -5.0 \\ & -2.0 \\ & 200 \\ & 100 \\ & 50 \\ & 50 \end{aligned}$ | $\begin{aligned} & \pm 2 \\ & 1 \\ & 750 \\ & 370 \\ & 62 \\ & \\ & <0.1 \end{aligned}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{ccI}}+0.2 \\ & \mathrm{~V}_{\mathrm{ccI}}+0.2 \\ & \mathrm{~V}_{\mathrm{cl}} \\ & +5.0 \\ & +5.0 \\ & +2.0 \\ & \\ & 7500 \\ & 4000 \end{aligned}$ | V <br> V <br> V <br> mV <br> $\mu \mathrm{A}$ <br> $\mu \mathrm{A}$ <br> pF <br> $\mathrm{k} \Omega$ <br> k $\Omega$ <br> dB <br> dB <br> dB <br> mV |
| LATCH ENABLE PIN CHARACTERISTICS <br> $\mathrm{V}_{\text {IH }}$ <br> VIL <br> $I_{H}$ <br> ILL |  | Hysteresis is shut off Latch mode guaranteed $\begin{aligned} \mathrm{V}_{\mathrm{IH}} & =\mathrm{V}_{\text {cco }}+0.2 \mathrm{~V} \\ \mathrm{~V}_{\mathrm{IL}} & =0.8 \mathrm{~V} \end{aligned}$ | $\begin{aligned} & 2.0 \\ & -0.2 \\ & -6 \\ & -0.1 \end{aligned}$ | $+0.4$ | $\begin{aligned} & \text { Vcco } \\ & +0.8 \\ & +6 \\ & +0.1 \end{aligned}$ | V <br> V <br> $\mu \mathrm{A}$ <br> mA |
| HYSTERESIS MODE AND TIMING <br> Hysteresis Mode Bias Voltage Minimum Resistor Value Hysteresis Current Latch Setup Time Latch Hold Time Latch-to-Output Delay Latch Minimum Pulse Width | ts <br> $\mathrm{t}_{\mathrm{H}}$ <br> tploh, tplol <br> $t_{\text {PL }}$ | $\begin{aligned} & \text { Current sink }-1 \mu \mathrm{~A} \\ & \text { Hysteresis }=120 \mathrm{mV} \\ & \text { Hysteresis }=120 \mathrm{mV} \\ & \text { V OD }=50 \mathrm{mV} \\ & \mathrm{~V}_{\mathrm{OD}}=50 \mathrm{mV} \\ & \mathrm{~V}_{\mathrm{OD}}=50 \mathrm{mV} \\ & \mathrm{~V}_{O D}=50 \mathrm{mV} \end{aligned}$ | $\begin{aligned} & 1.145 \\ & 30 \\ & -25 \end{aligned}$ | $\begin{aligned} & 1.25 \\ & \\ & -2 \\ & 2.7 \\ & 20 \\ & 24 \\ & \hline \end{aligned}$ | $\begin{aligned} & 1.40 \\ & 110 \\ & -8 \end{aligned}$ | V <br> k $\Omega$ <br> $\mu \mathrm{A}$ <br> ns <br> ns <br> ns <br> ns |
| SHUTDOWN PIN CHARACTERISTICS <br> $\mathrm{V}_{\mathrm{IH}}$ <br> VIL <br> Ін <br> IL <br> Sleep Time <br> Wake-Up Time | $\begin{aligned} & \mathrm{t}_{\mathrm{SD}} \\ & \mathrm{t}_{\mathrm{H}} \end{aligned}$ | Comparator is operating <br> Shutdown guaranteed $\begin{aligned} & \mathrm{V}_{\mathrm{HH}}=\mathrm{V}_{\mathrm{cco}} \\ & \mathrm{~V}_{\mathrm{IL}}=0 \mathrm{~V} \end{aligned}$ <br> 10\% output swing <br> $\mathrm{V}_{\mathrm{OD}}=50 \mathrm{mV}$, output valid | $\begin{aligned} & 2.0 \\ & -0.2 \\ & -6 \end{aligned}$ | $\begin{aligned} & +0.4 \\ & 1.4 \\ & 25 \end{aligned}$ | $\begin{aligned} & \text { Vcco } \\ & +0.6 \\ & +6 \\ & -0.1 \end{aligned}$ | V <br> V <br> $\mu \mathrm{A}$ <br> mA <br> ns <br> ns |
| DC OUTPUT CHARACTERISTICS <br> Differential Output Voltage Level <br> $\Delta V_{\text {OD }}$ <br> Common-Mode Voltage <br> Peak-to-Peak Common-Mode Output | Vod <br> Vocı <br> $\operatorname{Voc}(p-p)$ | $\begin{aligned} & \mathrm{V}_{\text {CCO }}=2.5 \mathrm{~V} \text { to } 5.0 \mathrm{~V} \\ & \mathrm{R}_{\text {LOAD }}=100 \Omega \\ & \mathrm{R}_{\text {LOAD }}=100 \Omega \\ & \mathrm{R}_{\text {LOAD }}=100 \Omega \\ & \mathrm{R}_{\text {LOAD }}=100 \Omega \end{aligned}$ | $\begin{aligned} & 245 \\ & 1.125 \end{aligned}$ | 350 | $\begin{aligned} & 445 \\ & 50 \\ & 1.375 \\ & 50 \end{aligned}$ | mV <br> mV <br> V <br> mV |


| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| AC PERFORMANCE ${ }^{1}$ |  |  |  |  |  |  |
| Rise Time/Fall Time | $\mathrm{t}_{\mathrm{R}}, \mathrm{t}_{\mathrm{F}}$ | 10\% to 90\% |  | 600 |  | ps |
| Propagation Delay | $\mathrm{t}_{\text {PD }}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{cco}}=2.5 \mathrm{~V} \text { to } 5.0 \mathrm{~V}, \\ & \mathrm{~V}_{\mathrm{oD}}=50 \mathrm{mV} \end{aligned}$ |  | 1.6 |  | ns |
|  |  | $\mathrm{V}_{\text {cCI }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}, \mathrm{~V}_{\text {OD }}=10 \mathrm{mV}$ |  | 3.0 |  | ns |
| Propagation Delay Skew-Rising to Falling Transition | tpInskew | $\mathrm{V}_{\text {clı }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ to 5.0 V |  | 70 |  | ps |
| Propagation Delay Skew-Q to $\overline{\mathrm{Q}}$ |  | $\mathrm{V}_{\text {clı }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ to 5.0 V |  | 70 |  | ps |
| Overdrive Dispersion |  | 10 mV < $\mathrm{V}_{\text {OD }}<125 \mathrm{mV}$ |  | 1.6 |  | ns |
| Common-Mode Dispersion |  | $\mathrm{V}_{\text {cm }}=-0.2 \mathrm{~V}$ to $\mathrm{V}_{\text {cli }}+0.2 \mathrm{~V}$ |  | 250 |  | ps |
| Input Bandwidth |  |  |  | 500 |  | MHz |
| Minimum Pulse Width | PW ${ }_{\text {MIN }}$ | $\begin{aligned} & \mathrm{V}_{\text {clI }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V} \text { to } 5.0 \mathrm{~V}, \\ & \text { PWout }=90 \% \text { of } \mathrm{PW} \text { IN } \end{aligned}$ |  | 1.3 |  | ns |
| POWER SUPPLY |  |  |  |  |  |  |
| Input Supply Voltage Range | V cıl |  | 2.5 |  | 5.5 | V |
| Output Supply Voltage Range | Vcco |  | 2.5 |  | 5.0 | V |
| Positive Supply Differential | $\mathrm{V}_{\text {cal }}$ - $\mathrm{V}_{\text {cco }}$ | Operating | -3 |  | +3 | V |
|  | $\mathrm{V}_{\text {cal }}$ - $\mathrm{V}_{\text {cco }}$ | Nonoperating | -5.0 |  | +5.0 | V |
| Input Section Supply Current | Ivca | $\mathrm{V}_{\text {cci }}=2.5 \mathrm{~V}$ to 5.5 V |  | 1.6 | 3.0 | mA |
| Output Section Supply Current | Ivcco | $\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ to 5.0 V |  | 15 | 23 | mA |
| Power Dissipation | PD | $\mathrm{V}_{\text {clı }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ |  | 37 | 55 | mW |
|  |  | $\mathrm{V}_{\text {cla }}=\mathrm{V}_{\text {cco }}=5.0 \mathrm{~V}$ |  | 95 | 120 | mW |
| Power Supply Rejection Ratio | PSRR | $\mathrm{V}_{\text {cla }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ to 5.0 V | -50 | -60 |  | dB |
| Shutdown Mode Ical |  | $\mathrm{V}_{\text {ccl }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ to 5.0 V |  | 0.92 | 1.1 | mA |
| Shutdown Mode Icco |  | $\mathrm{V}_{\text {ccl }}=\mathrm{V}_{\text {cco }}=2.5 \mathrm{~V}$ to 5.0 V | -30 |  | +30 | $\mu \mathrm{A}$ |

[^0]
## TIMING INFORMATION

Figure 2 illustrates the AD8465 latch timing relationships. Table 2 provides definitions of the terms shown in Figure 2.


Figure 2. System Timing Diagram

Table 2. Timing Descriptions

| Symbol | Timing | Description |
| :---: | :---: | :---: |
| $t_{\text {PDH }}$ | Input-to-Output High Delay | Propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the $50 \%$ point of an output low-to-high transition. |
| tPDL | Input-to-Output Low Delay | Propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the $50 \%$ point of an output high-to-low transition. |
| tploh | Latch Enable-to-Output High Delay | Propagation delay measured from the $50 \%$ point of the latch enable signal low-to-high transition to the 50\% point of an output low-to-high transition. |
| tploL | Latch Enable-to-Output Low Delay | Propagation delay measured from the $50 \%$ point of the latch enable signal high-to-low transition to the $50 \%$ point of an output high-to-low transition. |
| $\mathrm{tH}^{\text {}}$ | Minimum Hold Time | Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs. |
| $t_{\text {PL }}$ | Minimum Latch Enable Pulse Width | Minimum time that the latch enable signal must be high to acquire an input signal change. |
| ts | Minimum Setup Time | Minimum time before the negative transition of the latch enable signal occurs that an input signal change must be present to be acquired and held at the outputs. |
| $\mathrm{t}_{\mathrm{R}}$ | Output Rise Time | Amount of time required to transition from a low-to-high output as measured at the 20\% and 80\% points. |
| $\mathrm{t}_{\mathrm{F}}$ | Output Fall Time | Amount of time required to transition from a high-to-low output as measured at the $20 \%$ and $80 \%$ points. |
| Vod | Voltage Overdrive | Difference between the input voltages, $\mathrm{V}_{\mathrm{P}}$ and $\mathrm{V}_{\mathrm{N}}$. |

## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
| :---: | :---: |
| Supply Voltages |  |
| Input Supply Voltage (V $\mathrm{V}_{\text {cI }}$ to GND) | -0.5 V to +6.0 V |
| Output Supply Voltage (Vcco to GND) | -0.5 V to +6.0 V |
| Positive Supply Differential (Vccl $-\mathrm{V}_{\text {cco }}$ ) | -6.0 V to +6.0 V |
| Input Voltages |  |
| Input Voltage | -0.5 V to $\mathrm{V}_{\text {ccI }}+0.5 \mathrm{~V}$ |
| Differential Input Voltage | $\pm\left(\mathrm{V}_{\mathrm{clI}}+0.5 \mathrm{~V}\right)$ |
| Maximum Input/Output Current | $\pm 50 \mathrm{~mA}$ |
| Shutdown Control Pin |  |
| Applied Voltage ( $\mathrm{S}_{\text {DN }}$ to GND) | -0.5 V to $\mathrm{V}_{\text {cco }}+0.5 \mathrm{~V}$ |
| Maximum Input/Output Current | $\pm 50 \mathrm{~mA}$ |
| Latch/Hysteresis Control Pin |  |
| Applied Voltage (LE/HYS to GND) | -0.5 V to $\mathrm{V}_{\text {cco }}+0.5 \mathrm{~V}$ |
| Maximum Input/Output Current | $\pm 50 \mathrm{~mA}$ |
| Output Current | $\pm 50 \mathrm{~mA}$ |
| Temperature |  |
| Operating Temperature Range, Ambient | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Operating Temperature, Junction | $150^{\circ} \mathrm{C}$ |
| Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{\text {IA }}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

| Package Type | $\boldsymbol{\theta}_{\mathrm{JA}}{ }^{1}$ | Unit |
| :--- | :--- | :--- |
| 12-Lead LFCSP_WQ (CP-12-5) | 62 | ${ }^{\circ} \mathrm{C} / \mathrm{W}$ |

${ }^{1}$ Measurement in still air.

## ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
| :---: | :---: | :---: |
| 1 | $\mathrm{V}_{\text {cco }}$ | Output Section Supply. |
| 2 | $V_{\text {cII }}$ | Input Section Supply. |
| 3, 5, 9, 11 | $\mathrm{V}_{\mathrm{EE}}$ | Negative Supply Voltages. |
| 4 | $V_{\text {P }}$ | Noninverting Analog Input. |
| 6 | $\mathrm{V}_{\mathrm{N}}$ | Inverting Analog Input. |
| 7 | $\mathrm{S}_{\mathrm{DN}}$ | Shutdown. Drive this pin low to shut down the device. |
| 8 | LE/HYS | Latch/Hysteresis Control. Bias with resistor or current for hysteresis; drive low to latch. |
| 10 | $\overline{\mathrm{Q}}$ | Inverting Output. $\overline{\mathrm{Q}}$ is at logic low if the analog voltage at the noninverting input, $\mathrm{V}_{\mathrm{P}}$, is greater than the analog voltage at the inverting input, $\mathrm{V}_{\mathrm{N}}$, if the comparator is in compare mode. |
| 12 | Q | Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, $\mathrm{V}_{\mathrm{P}}$, is greater than the analog voltage at the inverting input, $\mathrm{V}_{\mathrm{N}}$, if the comparator is in compare mode. |
| 0 | EPAD | Exposed Pad. The metallic back surface of the package is electrically connected to $V_{\text {EE }}$. It can be left floating because Pin 3, Pin 5, Pin 9, and Pin 11 provide adequate electrical connection. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired. |

## AD8465

## TYPICAL PERFORMANCE CHARACTERISTICS

$\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CCO}}=2.5 \mathrm{~V}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$, unless otherwise noted.


Figure 4. LE/HYS Pin Current vs. Voltage


Figure 5. SDN Pin Current vs. Voltage


Figure 6. Input Bias Current vs. Input Common-Mode Voltage


Figure 7. LVDS Output Level vs. Vcco


Figure 8. LVDS Output Rise/Fall Time vs. Vcco


Figure 9. Hysteresis vs. Hysteresis Resistor


Figure 10. Hysteresis vs. LE/HYS Pin Current


Figure 11. Propagation Delay vs. Input Overdrive


Figure 12. Propagation Delay vs. Input Common-Mode Voltage


Figure 13. LVDS Output Swing vs. Vcco


Figure 14.50 MHz Output Voltage Waveform at $V_{c c o}=2.5 \mathrm{~V}$


Figure 15.50 MHz Output Voltage Waveform at Vcco $=5.5 \mathrm{~V}$

## APPLICATION INFORMATION POWER/GROUND LAYOUT AND BYPASSING

The AD8465 comparator is a very high speed device. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because the comparator is an uncompensated amplifier, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. The use of low impedance supply planes is of critical importance particularly with the output supply plane ( $\mathrm{V}_{\mathrm{CCO}}$ ) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.
It is also important to adequately bypass the input and output supplies. Place multiple high quality $0.01 \mu \mathrm{~F}$ bypass capacitors as close as possible to each of the $V_{\mathrm{CCI}}$ and $\mathrm{V}_{\mathrm{CCO}}$ supply pins and connect the capacitors to the GND plane with redundant vias. Place at least one capacitor to provide a physically short return path for output currents flowing back from ground to the $\mathrm{V}_{\mathrm{CCI}}$ pin and the Vcco pin. Carefully select high frequency bypass capacitors for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.
The input and output supplies have been connected separately ( $\mathrm{V}_{\mathrm{CCI}} \neq \mathrm{V}_{\mathrm{CCO}}$ ); be sure to bypass each of these supplies separately to the GND plane. Do not connect a bypass capacitor between these supplies. It is recommended that the GND plane separate the $V_{C C I}$ and $V_{C C O}$ planes when the circuit board layout is designed to minimize coupling between the two supplies to take advantage of the additional bypass capacitance from each respective supply to the ground plane. This enhances the performance when split input/output supplies are used. If the input and output supplies are connected together for single-supply operation $\left(\mathrm{V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CCO}}\right)$, coupling between the two supplies is unavoidable; however, careful board placement can help keep output return currents away from the inputs.

## LVDS-COMPATIBLE OUTPUT STAGE

Specified propagation delay dispersion performance is only achieved by keeping parasitic capacitive loads at or below the specified minimums. The outputs of the AD8465 are designed to directly drive any standard LVDS-compatible input.

## USING/DISABLING THE LATCH FEATURE

The latch input is designed for maximum versatility. It can safely be left floating or it can be driven low by any standard TTL/CMOS device as a high speed latch. In addition, the pin can be operated as a hysteresis control pin with a bias voltage of 1.25 V nominal and an input resistance of approximately $70 \mathrm{k} \Omega$. This allows the comparator hysteresis to be easily controlled by either a resistor or an inexpensive CMOS DAC. Driving this pin high or floating the pin disables all hysteresis.
Hysteresis control and latch mode can be used together if an open drain, an open collector, or a three-state driver is connected in parallel to the hysteresis control resistor or current source.
Due to the programmable hysteresis feature, the logic threshold of the latch pin is approximately 1.1 V , regardless of $\mathrm{V}_{\mathrm{cco}}$.

## OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. Large discontinuities along input and output transmission lines can also limit the specified pulse width dispersion performance. Minimize the source impedance as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, thus degrading the overall response. Thermal noise from large resistances can easily cause extra jitter with slowly slewing input signals. Higher impedances encourage undesired coupling.

## COMPARATOR PROPAGATION DELAY DISPERSION

The AD8465 comparator is designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to $\mathrm{V}_{\mathrm{CCI}}-1 \mathrm{~V}$. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (how far or how fast the input signal is driven past the switching threshold).
Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communications, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (see Figure 16 and Figure 17).

The AD8465 dispersion is typically $<1.6 \mathrm{~ns}$ as the overdrive varies from 10 mV to 125 mV . This specification applies to both positive and negative signals because the AD8465 has substantially equal delays for positive-going and negativegoing inputs and very low output skews.


Figure 16. Propagation Delay—Overdrive Dispersion


Figure 17. Propagation Delay—Slew Rate Dispersion

## COMPARATOR HYSTERESIS

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. The transfer function for a comparator with hysteresis is shown in Figure 18. As the input voltage approaches the threshold ( 0 V , in this example) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses $+\mathrm{V}_{\mathrm{H}} / 2$. The new switching threshold becomes $-\mathrm{V}_{\mathrm{H}} / 2$. The comparator remains in the high state until the $-\mathrm{V}_{\mathrm{H}} / 2$ threshold is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by $\pm \mathrm{V}_{\mathrm{H}} / 2$.


Figure 18. Comparator Hysteresis Transfer Function
The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high-speed performance and induce oscillation in some cases.

The AD8465 comparator offers a programmable hysteresis feature that significantly improves accuracy and stability. Connecting an external pull-down resistor or a current source from the LE/HYS pin to GND varies the amount of hysteresis in a predictable and stable manner. Leaving the LE/HYS pin disconnected or driving it high removes hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV . Figure 19 illustrates the amount of hysteresis applied as a function of external resistor value. Figure 10 illustrates hysteresis as a function of current.

The hysteresis control pin appears as a 1.25 V bias voltage seen through a series resistance of $70 \mathrm{k} \Omega \pm 20 \%$ throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, improved stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the LE/HYS pin because it would likely degrade the jitter performance of the device and impair the latch function. As described in the Using/Disabling the Latch Feature section, hysteresis control need not compromise the latch function.


Figure 19. Hysteresis vs. RHys Control Resistor

## CROSSOVER BIAS POINTS

Rail-to-rail inputs of this type, in both op amps and comparators, have a dual front-end design. Certain devices are active near the $\mathrm{V}_{\mathrm{CCI}}$ rail and others are active near the $\mathrm{V}_{\mathrm{EE}}$ rail. At some predetermined point in the common-mode range, a crossover occurs. At this point, normally $\mathrm{V}_{\mathrm{cc}} / 2$, the direction of the bias current reverses and there are changes in measured offset voltages and currents.

## MINIMUM INPUT SLEW RATE REQUIREMENT

With the rated load capacitance and normal good PCB design practice, as discussed in the Optimizing Performance section, these comparators should be stable at any input slew rate with no hysteresis. Broadband noise from the input stage is observed in place of the violent chattering seen with most other high speed comparators. With additional capacitive loading or poor bypassing, oscillation is observed. This oscillation is due to the high gain bandwidth of the comparator in combination with feedback parasitics in the package and PCB. In many applications, chattering is not harmful.

## TYPICAL APPLICATION CIRCUITS



Figure 20. Self-Biased, 50\% Slicer


Figure 21. LVDS to Repeater


Figure 22. Hysteresis Adjustment with Latch

Figure 23. Voltage-Controlled Oscillator



Figure 24. Oscillator and Pulse-Width Modulator


Figure 25. Hysteresis Adjustment with Latch

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.
Figure 26. 12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
$3 \mathrm{~mm} \times 3 \mathrm{~mm}$ Body, Very Very Thin Quad
(CP-12-5)
Dimensions shown in millimeters

## ORDERING GUIDE

| Model $^{\mathbf{1 , 2}}$ | Temperature Range | Package Description | Package Option | Branding |
| :--- | :--- | :--- | :--- | :--- |
| AD8465WBCPZ-WP | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 12-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-12-5 | Y24 |
| AD8465WBCPZ-R7 | $-40^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ | 12-Lead Lead Frame Chip Scale Package [LFCSP_WQ] | CP-12-5 | Y24 |

${ }^{1} \mathrm{Z}=$ RoHS Compliant Part.
${ }^{2} \mathrm{~W}=$ Qualified for Automotive Applications

## AUTOMOTIVE PRODUCTS

The AD8465W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.


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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.


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[^0]:    ${ }^{1} \mathrm{~V}_{\mathbb{I N}}=100 \mathrm{mV}$ square input at $50 \mathrm{MHz}, \mathrm{V}_{\mathrm{OD}}=50 \mathrm{mV}, \mathrm{V}_{\mathrm{CM}}=1.25 \mathrm{~V}, \mathrm{~V}_{\mathrm{CCI}}=\mathrm{V}_{\mathrm{CCO}}=2.5 \mathrm{~V}$, unless otherwise noted.

