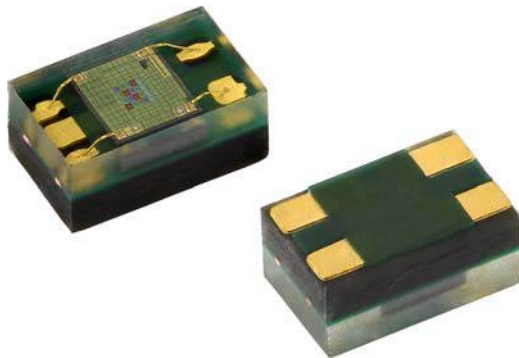


RGBW Color Sensor with I²C Interface



DESCRIPTION

VEML6040 color sensor senses red, green, blue, and white light and incorporates photodiodes, amplifiers, and analog / digital circuits into a single chip using CMOS process. With the color sensor applied, the brightness, and color temperature of backlight can be adjusted base on ambient light source that makes panel looks more comfortable for end user's eyes. VEML6040's adoption of Filtron™ technology achieves the closest ambient light spectral sensitivity to real human eye responses.

VEML6040 provides excellent temperature compensation capability for keeping the output stable under changing temperature. VEML6040's function are easily operated via the simple command format of I²C (SMBus compatible) interface protocol. VEML6040's operating voltage ranges from 2.5 V to 3.6 V. VEML6040 is packaged in a lead (Pb)-free 4 pin OPLGA package which offers the best market-proven reliability.

FEATURES

- Package type: surface mount
- Dimensions (L x W x H in mm): 2.0 x 1.25 x 1.0
- Integrated modules: color sensor (RGBW) and signal conditioning IC
- Filtron™ technology provides a spectrum matching real human eye responses
- Supports low transmittance (dark) lens design
- Fluorescent light flicker immunity
- Provides 16-bit resolution for each channel (R, G, B, W)
- Selectable maximum detection range (360, 721, 1442, 2883, 5767, or 11 796) lux with highest sensitivity 0.0056 lux/step
- Package: OPLGA
- Temperature compensation: -40 °C to +85 °C
- Low power consumption I²C (SMBus compatible) interface
- Floor life: 168 h, MSL 3, according to J-STD-020
- Output type: I²C bus
- Operation voltage: 2.5 V to 3.6 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



APPLICATIONS

- Handheld device
- Notebook
- Consumer device
- Industrial and mechanical application

PRODUCT SUMMARY

| PART NUMBER | OPERATING VOLTAGE RANGE (V) | I ² C BUS VOLTAGE RANGE (V) | PEAK SENSITIVITY (nm) | RANGE OF SPECTRAL BANDWIDTH λ _{0.5} (nm) | OUTPUT CODE |
|-------------|-----------------------------|--|-------------------------|---|--------------------------|
| VEML6040 | 2.5 to 3.6 | 1.7 to 3.6 | 650, 550, 450 (R, G, B) | ± 35, ± 35, ± 40 (R, G, B) | 16 bit, I ² C |

Note

(1) Adjustable through I²C interface

ORDERING INFORMATION

| ORDERING CODE | PACKAGING | VOLUME (1) | REMARKS |
|---------------|---------------|---------------|---------------------------|
| VEML6040A30G | Tape and reel | MOQ: 2500 pcs | 2.0 mm x 1.25 mm x 1.0 mm |

Note

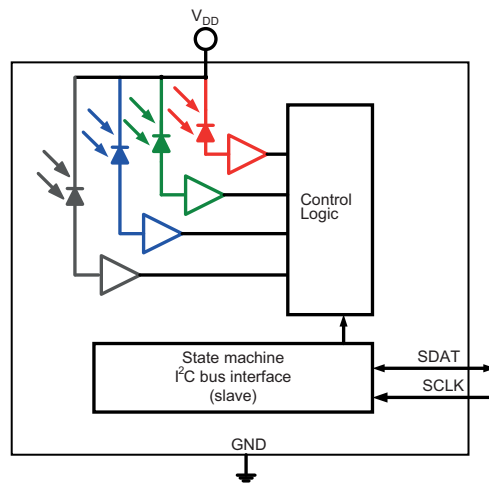
(1) MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

| PARAMETER | TEST CONDITION | SYMBOL | MIN. | MAX. | UNIT |
|-----------------------------|----------------|------------------|------|------|------|
| Supply voltage | | V _{DD} | 0 | 3.6 | V |
| Operation temperature range | | T _{amb} | -40 | +85 | °C |
| Storage temperature range | | T _{stg} | -40 | +85 | °C |

| RECOMMENDED OPERATING CONDITIONS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified) | | | | | |
|--|----------------|----------------|------|------|--------------------|
| PARAMETER | TEST CONDITION | SYMBOL | MIN. | MAX. | UNIT |
| Supply voltage | | V_{DD} | 2.5 | 3.6 | V |
| Operation temperature range | | T_{amb} | -40 | +85 | $^{\circ}\text{C}$ |
| I ² C bus operating frequency | | $f_{(I2CCLK)}$ | 10 | 400 | kHz |

| PIN DESCRIPTIONS | | | |
|-------------------------|----------|--------------------|---|
| PIN ASSIGNMENT | SYMBOL | TYPE | FUNCTION |
| 1 | GND | I | Ground |
| 2 | SDAT | I / O (open drain) | I ² C data bus data input / output |
| 3 | SCLK | I | I ² C digital bus clock input |
| 4 | V_{DD} | I | Power supply input |

BLOCK DIAGRAM


| BASIC CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified) | | | | | | |
|---|---|---|----------|--------|------|----------------------------------|
| PARAMETER | TEST CONDITION | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Supply voltage | | V_{DD} | 2.5 | | 3.6 | V |
| Supply current | | I_{DD} | | 200 | | μA |
| I ² C signal input | Logic high | $V_{DD} = 3.3\text{ V}$ | V_{IH} | 1.5 | | V |
| | Logic low | | V_{IL} | | 0.8 | |
| | Logic high | $V_{DD} = 2.6\text{ V}$ | V_{IH} | 1.4 | | V |
| | Logic low | | V_{IL} | | 0.6 | |
| Peak sensitivity wavelength | | λ_{PR} | | 650 | | nm |
| | | λ_{PG} | | 550 | | nm |
| | | λ_{PB} | | 450 | | nm |
| Irradiance responsivity | $\lambda_{PR} = 630\text{ nm}$ | | | 180 | | LSB/ $(\mu\text{W}/\text{cm}^2)$ |
| | $\lambda_{PG} = 530\text{ nm}$ | | | 144 | | |
| | $\lambda_{PB} = 467\text{ nm}$ | | | 52 | | |
| Detectable intensity | Minimum | G channel, $t_T = 1280\text{ ms}$ ⁽¹⁾⁽²⁾ | | 0.0056 | | lx |
| | Maximum | G channel, $t_T = 40\text{ ms}$ ⁽¹⁾⁽²⁾ | | 11 796 | | |
| Dark offset | | G channel, $t_T = 80\text{ ms}$ ⁽¹⁾ | | 0 | 3 | |
| Operating temperature range | | T_{amb} | -40 | | +85 | $^{\circ}\text{C}$ |
| Shutdown current | Light condition = dark, $V_{DD} = 3.6\text{ V}$ | I_{DD} | | 800 | | nA |

Notes

- (1) Test condition: $V_{DD} = 3.3\text{ V}$, temperature: $25\text{ }^{\circ}\text{C}$
 (2) Light source: white LED

| I²C BUS TIMING CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified) | | | | | | |
|---|-----------------|---------------|------|-----------|------|---------------|
| PARAMETER | SYMBOL | STANDARD MODE | | FAST MODE | | UNIT |
| | | MIN. | MAX. | MIN. | MAX. | |
| Clock frequency | $f_{(SMBCLK)}$ | 10 | 100 | 10 | 400 | kHz |
| Bus free time between start and stop condition | $t_{(BUF)}$ | 4.7 | | 1.3 | | μs |
| Hold time after (repeated) start condition; after this period, the first clock is generated | $t_{(HDSTA)}$ | 4.0 | | 0.6 | | μs |
| Repeated start condition setup time | $t_{(SUSTA)}$ | 4.7 | | 0.6 | | μs |
| Stop condition setup time | $t_{(SUSTO)}$ | 4.0 | | 0.6 | | μs |
| Data hold time | $t_{(HDDAT)}$ | 200 | | 90 | | ns |
| Data setup time | $t_{(SUDAT)}$ | 250 | | 100 | | ns |
| I ² C clock (SCK) low period | $t_{(LOW)}$ | 4.7 | | 1.3 | | μs |
| I ² C clock (SCK) high period | $t_{(HIGH)}$ | 4.0 | | 0.6 | | μs |
| Detect clock / data low timeout | $t_{(TIMEOUT)}$ | 25 | 35 | | | ms |
| Clock / data fall time | $t_{(F)}$ | | 300 | | 300 | ns |
| Clock / data rise time | $t_{(R)}$ | | 1000 | | 300 | ns |

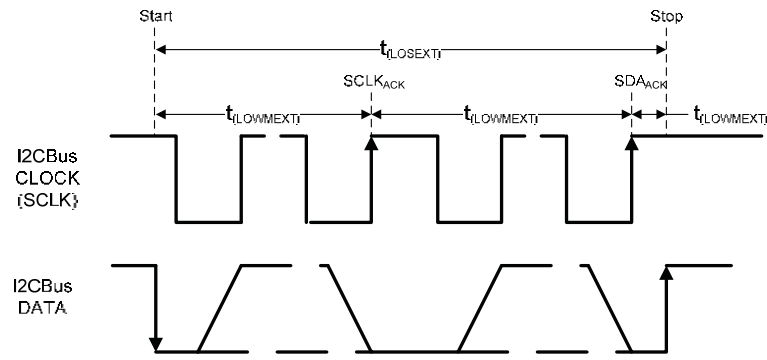
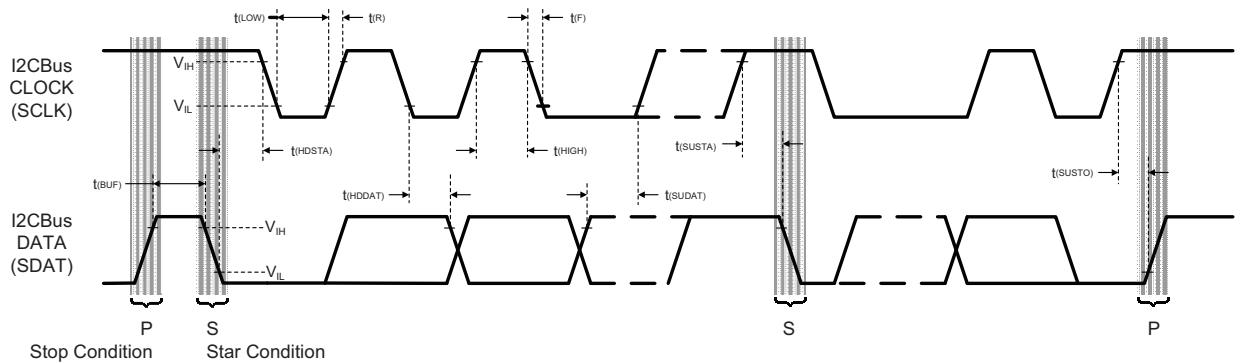


Fig. 1 - I²C Bus Timing Diagram

PARAMETER TIMING INFORMATION

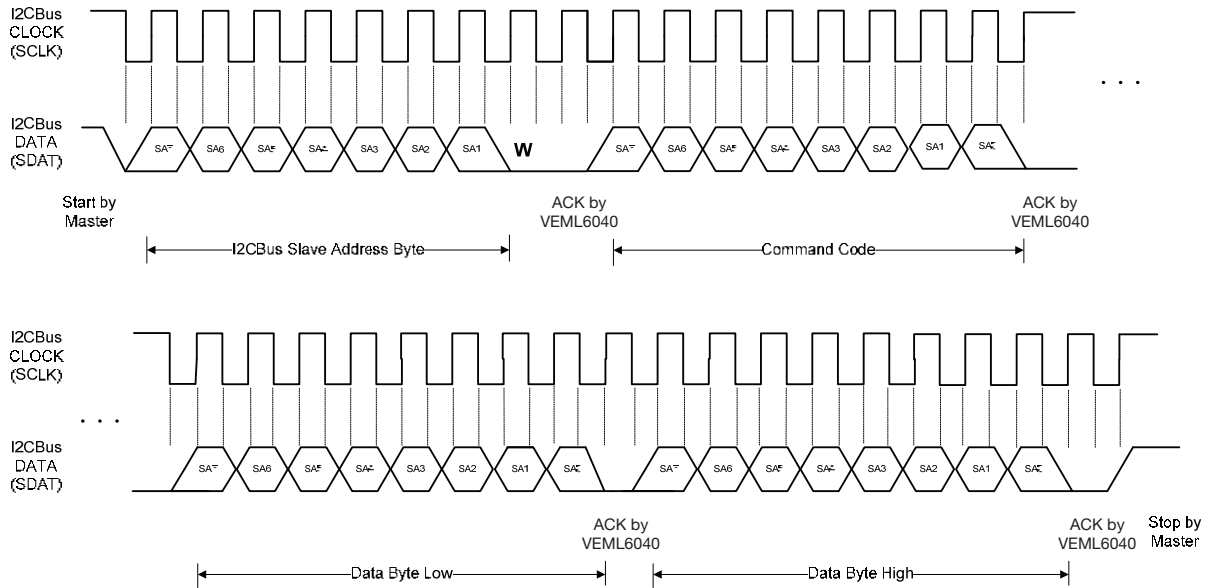


Fig. 2 - I²C Bus Timing for Sending Word Command Format

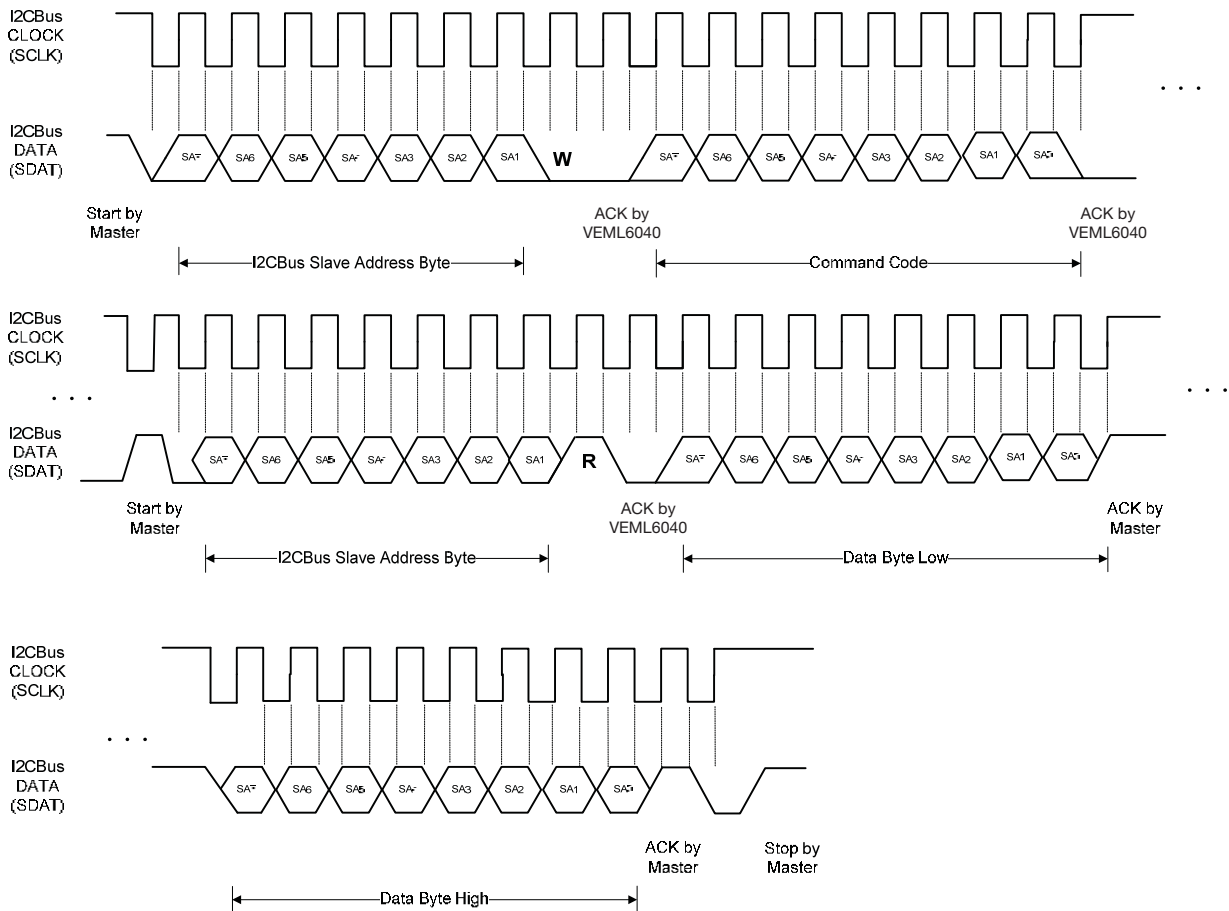


Fig. 3 - I²C Bus Timing for Receiving Word Command Format

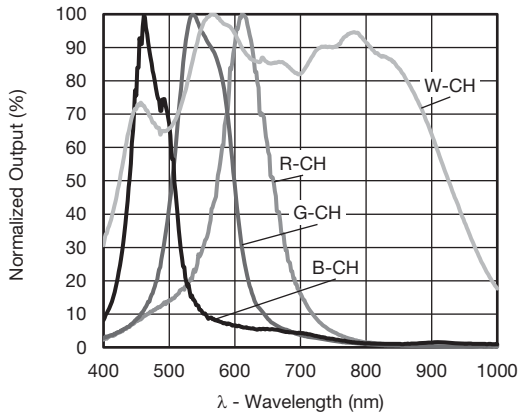
TYPICAL PERFORMANCE CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 4 - Normalized Spectral Response

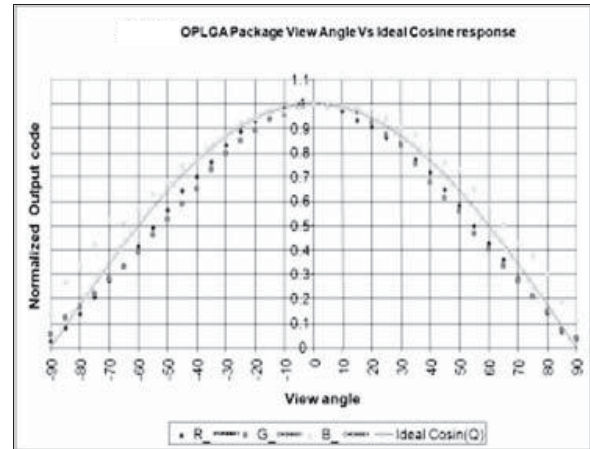


Fig. 5 - Normalized Output vs. View Angle

APPLICATION INFORMATION
Pin Connection with the Host

VEML6040 integrates R, G, B, and W sensor together with I²C interface. It is very easy for the baseband (CPU) to access VEML6040 output data via I²C interface without extra software algorithms. The hardware schematic is shown in the following diagram.

The 0.1 μF capacitor near the V_{DD} pin is used for power supply noise rejection. The 2.2 k Ω s are suitable for the pull-up resistors of I²C.

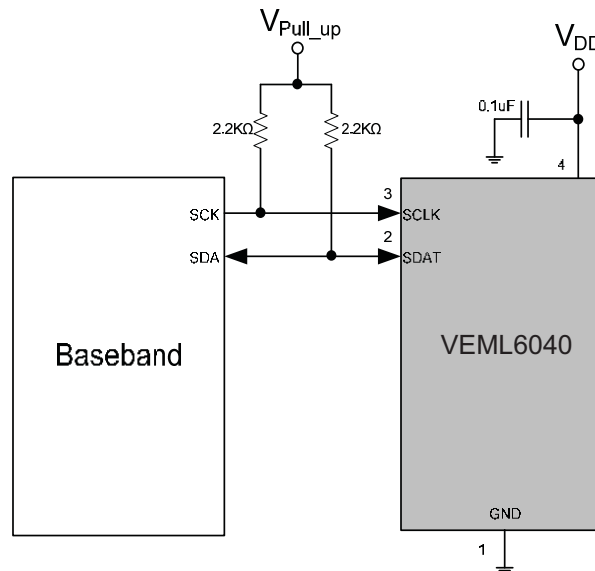


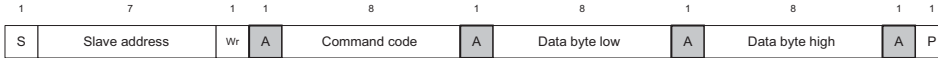
Fig. 6 - Hardware Pin Connection Diagram



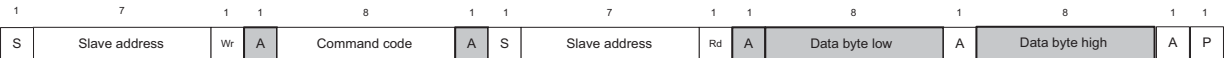
Digital Interface

VEML6040 apply slave address 0x10 of 7 bit addressing protocol for I2C. VEML6040 contains an 8-bit command register following each of slave address as shown in figure 7. All operations can be controlled by the command register. The simple command structure helps users easily program the operation setting and latch the light data from VEML6040. Following I2C command format is simple for read and write operations between VEML6040 and the host as shown in figure 7. The white sections indicate host activity and the gray sections indicate VEML6040's acknowledgement of the host access activity. Based on write word protocol, 8-bit command codes can be written by the host under the same slave address. For data reading, VEML6040 apply read word protocol.

Send Byte → Write Command to VEML6040



Receive Byte → Read Data from VEML6040



S = start condition
P = stop condition
A = acknowledge
Shaded area = VEML6040 acknowledge

Fig. 7 - Command Protocol Format

Slave Address and Function Description

VEML6040 uses 0x10 slave address for 7-bit I2C addressing protocol. VEML6040 has 16-bit resolution for each channel (R, G, B, and W) that provides sensitivity up to 0.0056 lux/step for G, which is advantageous under a low transmittance lens design (dark lens).

TABLE 1 - SLAVE ADDRESS AND COMMAND CODE DESCRIPTION. Table with columns: COMMAND CODE, REGISTER NAME, R / W, BIT (7, 6, 5, 4, 3, 2, 1, 0). Rows include CONF, Reserved, R_DATA_L, R_DATA_M, G_DATA_L, G_DATA_M, B_DATA_L, B_DATA_M, W_DATA_L, W_DATA_M.

Note

- Slave address is 7-bit addressing protocol



Command Register Format

VEML6040 provides an 8-bit command register for controlling. The description of each command format is shown in the following tables. Color sensor is function compatible with ambient light sensor when apply color sensor at green channel.

Color Sensor Command

| TABLE 2-1 - COMMAND CODE 00H BITS DESCRIPTION | | | | | | | |
|---|-------|--|-------|-------|-------|-------|-------|
| SLAVE ADDRESS: 0x10; REGISTER NAME: CONF; COMMAND CODE: 00H / DATA BYTE LOW | | | | | | | |
| X | IT | | | X | TRIG | AF | SD |
| BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
| 0 | IT2 | IT1 | IT0 | 0 | TRIG | AF | SD |
| DESCRIPTION | | | | | | | |
| IT | | Integration time setting | | | | | |
| TRIG | | Proceed one detecting cycle at manual force mode | | | | | |
| AF | | Auto / manual force mode | | | | | |
| SD | | Chip shutdown setting | | | | | |

| TABLE 2-2 - COMMAND CODE 00H REGISTER SETTING | | | | | |
|--|--|-----------------------|---------------|--|-----------------------------------|
| BITS SETTING | | DESCRIPTION | BITS SETTING | | DESCRIPTION |
| BIT 7 | | Default = 0 | BIT 3 | | Default = 0 |
| BIT 6, 5, 4 IT (2 : 0) | | (0 : 0 : 0) = 40 ms | BIT 2 TRIG | | 0 = no trigger |
| | | (0 : 0 : 1) = 80 ms | | | 1 = trigger one time detect cycle |
| | | (0 : 1 : 0) = 160 ms | BIT 1 AF | | 0 = auto mode |
| | | (0 : 1 : 1) = 320 ms | | | 1 = force mode |
| | | (1 : 0 : 0) = 640 ms | BIT 0 SD | | 0 = enable color sensor |
| | | (1 : 0 : 1) = 1280 ms | | | 1 = disable color sensor |

| TABLE 3-1 - RESERVE COMMAND CODE DESCRIPTION | | |
|---|-------|------------------------------------|
| RESERVED | | COMMAND CODE: 00H / DATA BYTE HIGH |
| Command | Bit | Description |
| Reserved | 7 : 0 | Default = 00H |

| TABLE 3-2 - RESERVE COMMAND CODE DESCRIPTION | | |
|---|-------|--------------------------|
| RESERVED | | COMMAND CODE: 01H TO 07H |
| Command | Bit | Description |
| Reserved | 7 : 0 | Default = 00H |

| TABLE 4 - READ OUT COMMAND CODE DESCRIPTION | | | |
|--|----------|-------|---------------------------------------|
| COMMAND CODE | REGISTER | BIT | DESCRIPTION |
| 08H_L (08H data byte low) | R_DATA_L | 7 : 0 | 00H to FFH, R channel LSB output data |
| 08H_H (08H data byte high) | R_DATA_M | 7 : 0 | 00H to FFH, R channel MSB output data |
| 09H_L (09H data byte low) | G_DATA_L | 7 : 0 | 00H to FFH, G channel LSB output data |
| 09H_H (09H data byte high) | G_DATA_M | 7 : 0 | 00H to FFH, G channel MSB output data |
| 0AH_L (0AH data byte low) | B_DATA_L | 7 : 0 | 00H to FFH, B channel LSB output data |
| 0AH_H (0AH data byte high) | B_DATA_M | 7 : 0 | 00H to FFH, B channel MSB output data |
| 0BH_L (0BH data byte low) | W_DATA_L | 7 : 0 | 00H to FFH, W channel LSB output data |
| 0BH_H (0BH data byte high) | W_DATA_M | 7 : 0 | 00H to FFH, W channel MSB output data |

PACKAGE INFORMATION in millimeters

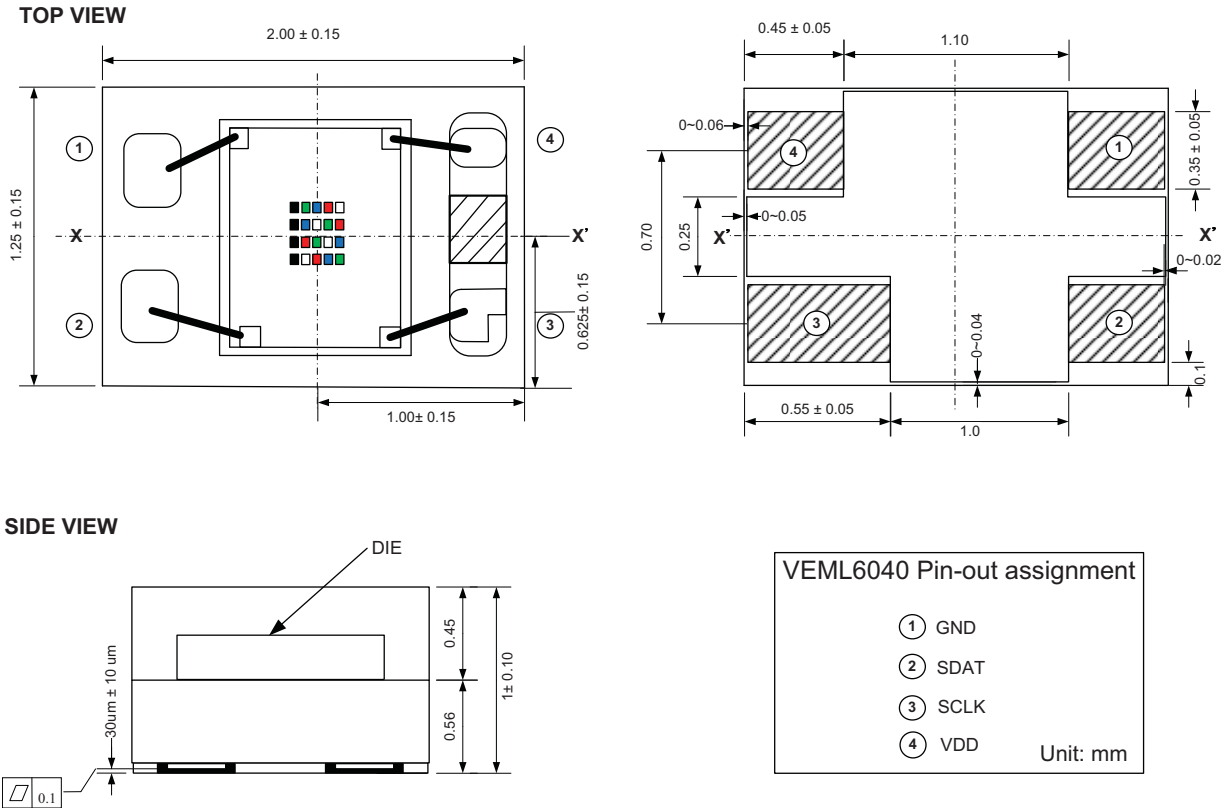


Fig. 8 - VEML6040 A3OG Package Dimensions

LAYOUT NOTICE AND REFERENCE CIRCUIT in millimeters

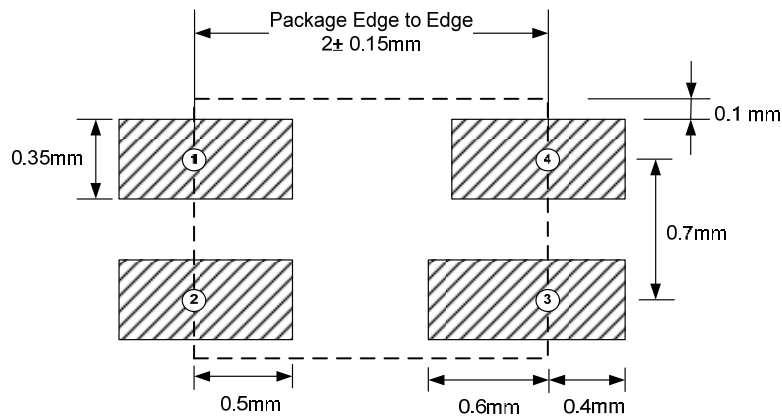


Fig. 9 - VEML6040 PCB Layout Footprint

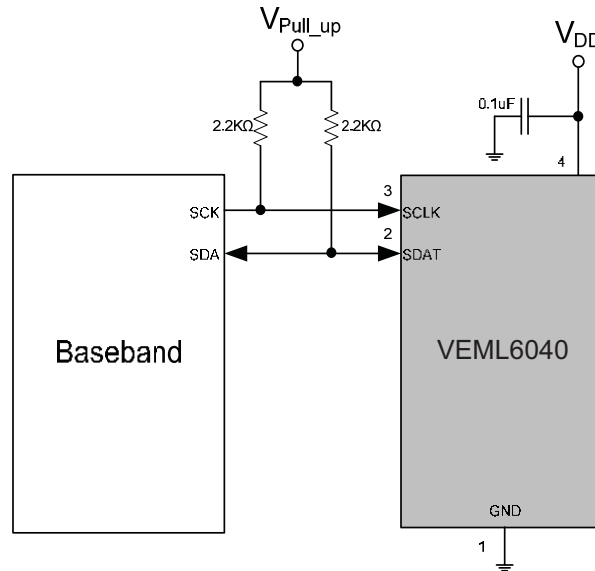
APPLICATION CIRCUIT BLOCK REFERENCE


Fig. 10 - VEML6040 Application Circuit

| RECOMMENDED STORAGE AND REBAKING CONDITIONS | | | | |
|---|--|------|------|--------|
| PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
| Storage temperature | | 5 | 50 | °C |
| Relative humidity | | | 60 | % |
| Open time | | | 168 | h |
| Total time | From the date code on the aluminized envelope (unopened) | | 12 | months |
| Rebaking | Tape and reel: 60 °C | | 22 | h |
| | Tube: 60 °C | | 22 | h |

RECOMMENDED INFRARED REFLOW

Soldering conditions which are based on J-STD-020 C

| IR REFLOW PROFILE CONDITION | | | |
|--|------------|---------------------------------------|---------------|
| PARAMETER | CONDITIONS | TEMPERATURE | TIME |
| Peak temperature | | 255 °C + 0 °C / - 5 °C (max.: 260 °C) | 10 s |
| Preheat temperature range and timing | | 150 °C to 200 °C | 60 s to 180 s |
| Timing within 5 °C to peak temperature | | | 10 s to 30 s |
| Timing maintained above temperature / time | | 217 °C | 60 s to 150 s |
| Timing from 25 °C to peak temperature | | | 8 min (max.) |
| Ramp-up rate | | 3 °C/s (max.) | |
| Ramp-down rate | | 6 °C/s (max.) | |

Recommend Normal Solder Reflow is 235 °C to 255 °C

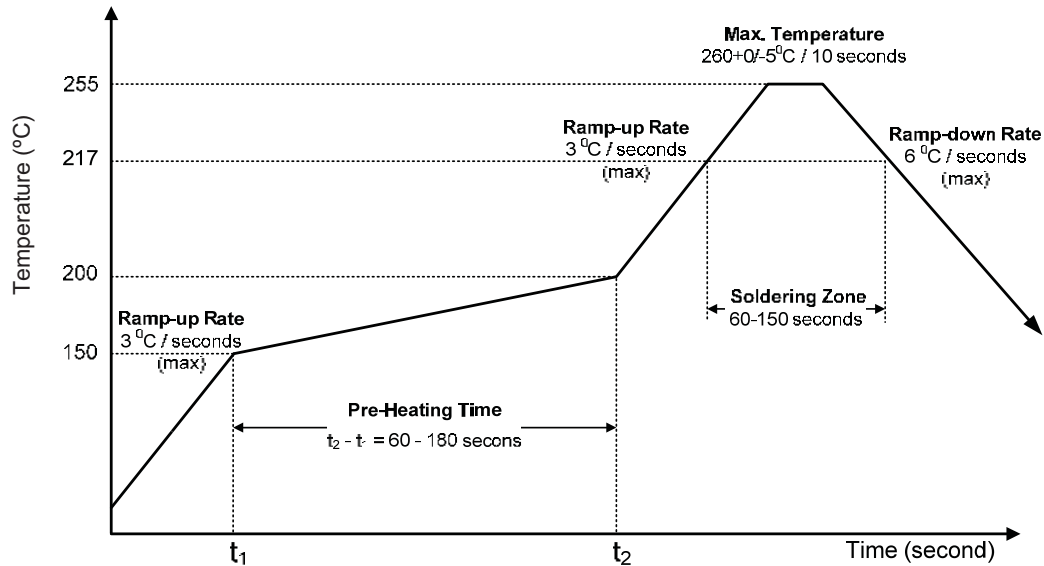


Fig. 11 - VEML6040 OPLGA Solder Reflow Profile Chart

RECOMMENDED IRON TIP SOLDERING CONDITION AND WARNING HANDLING

1. Solder the device with the following conditions:
 - 1.1. Soldering temperature: 400 °C (max.)
 - 1.2. Soldering time: 3 s (max.)
2. If the temperature of the method portion rises in addition to the residual stress between the leads, the possibility that an open or short circuit occurs due to the deformation or destruction of the resin increases.
3. The following methods: VPS and wave soldering, have not been suggested for the component assembly.
4. Cleaning method conditions:
 - 4.1. Solvent: methyl alcohol, ethyl alcohol, isopropyl alcohol
 - 4.2. Solvent temperature < 45 °C (max.)
 - 4.3. Time: 3 min (min.)

TAPE PACKAGING INFORMATION in millimeters

DIMENSION OF CARRIER TAPE

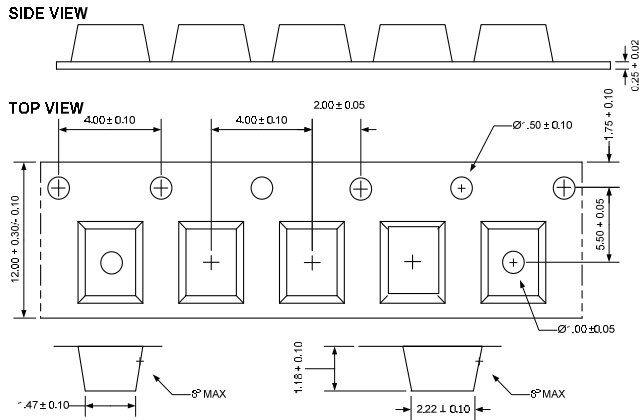


Fig. 12 - VEML6040 A3OG Package Carrier Tape

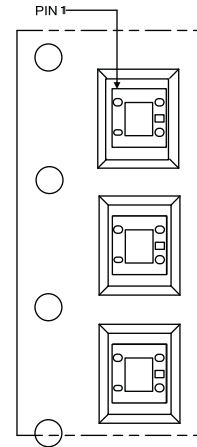


Fig. 13 - Taping Direction

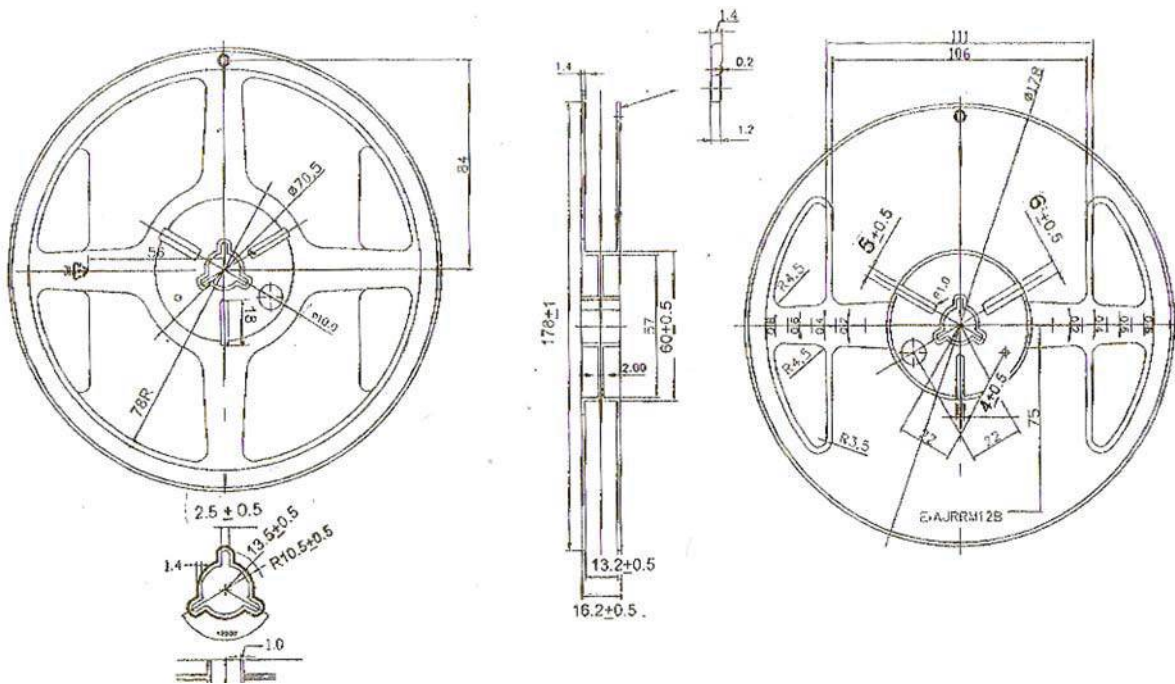


Fig. 14 - Reel Dimensions



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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