

Description

The 5PB12xx is a high-performance TCXO/LVCMOS clock fanout buffer family with individual OE pin for each output. The CLKIN pin can accept either a square wave (LVCMOS) or clipped sine wave (such as TCXO clipped sine wave output) as input.

There are 3 different fan-out versions available: 1:3, 1:4 and 1:6.

The 5PB12xx has industry-leading low jitter and extremely low current consumption, making it ideal for smart mobile devices.

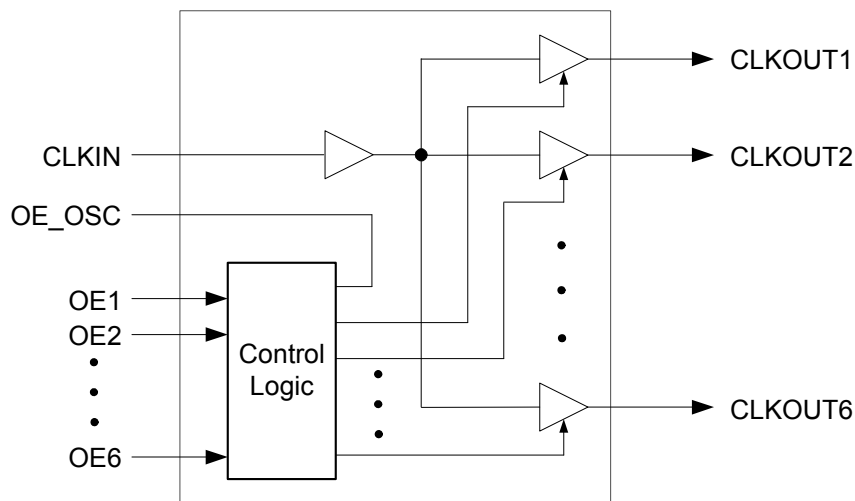
Typical Applications

- Smart Mobile Handsets
- RF and baseband peripheral clock distribution
- Automotive

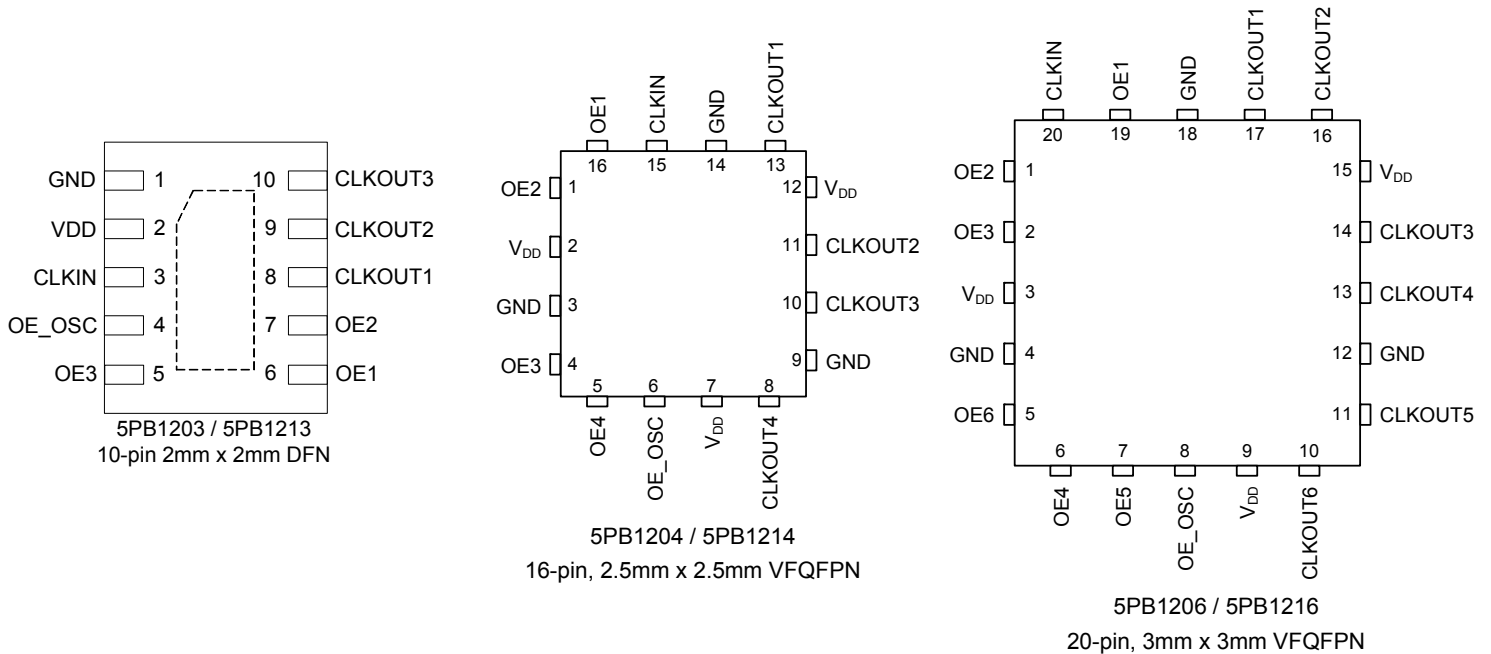
Features

- Extremely low operating and standby current consumption
- Low RMS additive phase jitter
- Family supports 1.8V to 3.3V power supply voltage:
 - For 1.8V supply: 5PB1203, 5PB1204, 5PB1206
 - For 2.5V / 3.3V supply: 5PB1213, 5PB1214, 5PB1216
- Three, four, and six outputs with individual Output Enable pin
- One input
- OE_OSC control pin to enable/disable reference TCXO/XO
- Small 10-pin, 16-pin and 20-pin packages available
- Industrial -40° to +105°C temperature range

Block Diagram



Pin Assignments



Pin Descriptions

| Pin Name | Pin Number | | | Pin Type | Pin Description |
|----------|--------------------|--------------------|--------------------|----------|--|
| | 5PB1203 5PB1213 | 5PB1204 5PB1214 | 5PB1206 5PB1216 | | |
| VDD | 2 | 2, 7, 12 | 3, 9, 15 | Power | Connect 1.8V to 5PB1203/5PB1204/5PB1206. Connect 2.5V or 3.3V to 5PB1213/5PB1214/5PB1216. |
| GND | 1 | 3, 9, 14 | 4, 12, 18 | Power | Power supply ground. |
| CLKIN | 3 | 15 | 20 | Input | Reference input pin. Connect to LVCMOS input or TCXO. |
| OE_osc | 4 | 6 | 8 | Output | Input Crystal Oscillator enable pin. Follow Enable Function Truth Table. If all OE pins are low then OE_osc is low. Otherwise OE_osc is high, enabling reference crystal oscillator. |
| OE1 | 6 | 16 | 19 | Input | Output Enable pin for CLKOUT1. Active High. Internal 120kΩ pull-down. |
| OE2 | 7 | 1 | 1 | Input | Output Enable pin for CLKOUT2. Active High. Internal 120kΩ pull-down. |
| OE3 | 5 | 4 | 2 | Input | Output Enable pin for CLKOUT3. Active High. Internal 120kΩ pull-down. |
| OE4 | — | 5 | 6 | Input | Output Enable pin for CLKOUT4. Active High. Internal 120kΩ pull-down. |
| OE5 | — | — | 7 | Input | Output Enable pin for CLKOUT5. Active High. Internal 120kΩ pull-down. |
| OE6 | — | — | 5 | Input | Output Enable pin for CLKOUT6. Active High. Internal 120kΩ pull-down. |
| CLKOUT1 | 8 | 13 | 17 | Output | Clock Output 1. Same frequency as CLKIN. |
| CLKOUT2 | 9 | 11 | 16 | Output | Clock Output 2. Same frequency as CLKIN. |
| CLKOUT3 | 10 | 10 | 14 | Output | Clock Output 3. Same frequency as CLKIN. |
| CLKOUT4 | — | 8 | 13 | Output | Clock Output 4. Same frequency as CLKIN. |
| CLKOUT5 | — | — | 11 | Output | Clock Output 5. Same frequency as CLKIN. |
| CLKOUT6 | — | — | 10 | Output | Clock Output 6. Same frequency as CLKIN. |

Enable Function Truth Table

| Input | | | | | | Output | | | | | | |
|-------|-----|-----|-----|-----|-----|--------|---------|---------|---------|---------|---------|---------|
| OE1 | OE2 | OE3 | OE4 | OE5 | OE6 | OE_OSC | CLKOUT1 | CLKOUT2 | CLKOUT3 | CLKOUT4 | CLKOUT5 | CLKOUT6 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 | CLOCK | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | CLOCK | CLOCK | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... | ... |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | CLOCK | CLOCK | CLOCK | CLOCK | CLOCK | CLOCK |

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD on pin 1 and GND on pin 4, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

To achieve the low output skew that the 5PB12xx is capable of, careful attention must be paid to board layout. Essentially, all four outputs must have identical terminations, identical loads and identical trace geometries. If they do not, the output skew will be degraded. For example, using a 30 Ω series termination on one output (with 33 Ω on the others) will cause at least 15ps of skew.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 5PB12xx. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|--|-----------------------|
| Supply Voltage, VDD | 3.8V |
| Output Enable and All Inputs/Outputs | -0.5 V to VDD + 0.5 V |
| Ambient Operating Temperature (extended) | -40 to +105°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

DC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%, for 5PB1203 / 1204 / 1206, ambient temperature -40° to +105°C, unless stated otherwise.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|---|-------------|-------|-------------|-------|
| Operating Voltage | VDD | | 1.71 | | 1.89 | V |
| Input High Voltage, CLKIN | V _{IH} | LVC MOS input. Note 1 | VDD/2 + 200 | | VDD | mV |
| Input Low Voltage, CLKIN | V _{IL} | LVC MOS input. Note 1 | | | VDD/2 - 200 | mV |
| Input High Voltage, OE | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -4mA | 0.8xVDD | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 4mA | | | 0.2xVDD | V |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | | | 5 | | pF |
| Operating Supply Current | | | | | | |
| 5PB1203 | IDD | CLKIN = 26MHz, all outputs enabled | | 5.10 | | mA |
| | | CLKIN = Low or High, all outputs disabled | | 0.02 | 0.03 | |
| 5PB1204 | | CLKIN = 26MHz, all outputs enabled | | 9.30 | | |
| | | CLKIN = Low or High, all outputs disabled | | 2.51 | 4 | |
| 5PB1206 | | CLKIN = 26MHz, all outputs enabled | | 11.90 | | |
| | | CLKIN = Low or High, all outputs disabled | | 2.5 | 4 | |

VDD = 2.5V ±5%, for 5PB1213 / 1214 / 1216, ambient temperature -40° to +105°C, unless stated otherwise.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|---|-------------|------|-------------|-------|
| Operating Voltage | VDD | | 2.375 | | 2.625 | V |
| Input High Voltage, CLKIN | V _{IH} | LVC MOS input. Note 1 | VDD/2 + 200 | | VDD | mV |
| Input Low Voltage, CLKIN | V _{IL} | LVC MOS input. Note 1 | | | VDD/2 - 200 | mV |
| Input High Voltage, OE | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -4mA | 0.8xVDD | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 4mA | | | 0.2xVDD | V |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | ICLK, OE pin | | 5 | | pF |
| Operating Supply Current | | | | | | |
| 5PB1213 | IDD | CLKIN = 26MHz, all outputs enabled | | 6.68 | | mA |
| | | CLKIN = Low or High, all outputs disabled | | 0.05 | 0.5 | |
| 5PB1214 | | CLKIN = 26MHz, all outputs enabled | | 10.2 | | |
| | | CLKIN = Low or High, all outputs disabled | | 3.47 | 5 | |
| 5PB1216 | | CLKIN = 26MHz, all outputs enabled | | 16.5 | | |
| | | CLKIN = Low or High, all outputs disabled | | 3.50 | 5 | |

VDD = 3.3V ±5%, for 5PB1213 / 1214 / 1216, ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---------------------------------|-----------------|---|-------------|------|-------------|-------|
| Operating Voltage | VDD | | 3.135 | | 3.465 | V |
| Input High Voltage, CLKIN | V _{IH} | LVC MOS input. Note 1 | VDD/2 + 200 | | VDD | mV |
| Input Low Voltage, CLKIN | V _{IL} | LVC MOS input. Note 1 | | | VDD/2 - 200 | mV |
| Input High Voltage, OE | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -4mA | 0.8xVDD | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 4mA | | | 0.2xVDD | V |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | ICLK, OE pin | | 5 | | pF |
| Operating Supply Current | | | | | | |
| 5PB1213 | IDD | CLKIN = 26MHz, all outputs enabled | | 9.10 | | mA |
| | | CLKIN = Low or High, all outputs disabled | | 0.22 | 0.5 | |
| 5PB1214 | | CLKIN = 26MHz, all outputs enabled | | 13.4 | | |
| | | CLKIN = Low or High, all outputs disabled | | 4.28 | 7 | |
| 5PB1216 | | CLKIN = 26MHz, all outputs enabled | | 21.4 | | |
| | | CLKIN = Low or High, all outputs disabled | | 4.60 | 7 | |

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

(VDD = 1.8V, 2.5V, 3.3V)

VDD = 1.8V ±5%; for 5PB1203 / 1204 / 1206, ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------------------------|---|------|------|------|--------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.36 to 1.44V, C _L = 5pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 1.44 to 0.36V, C _L = 5pF | | 0.6 | 1.0 | ns |
| Propagation Delay | Note 1 | Note 1 | 1.5 | 2.0 | 2.5 | ns |
| Buffer Additive Phase Jitter, RMS | | 26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz | | 420 | | fs |
| | | 125MHz LVCMOS input, Integration Range: 12kHz to 20MHz | | 42 | | fs |
| Output to Output Skew | t _{SKEWO-O} | Note 2, Rising edges at VDD/2 | | 20 | 50 | ps |
| Device to Device Skew | t _{SKEWD-D} | Rising edges at VDD/2 | | | 200 | ps |
| Delay for Output Enable / Disable Time ENABLEx to BCLKn | t _{EN} /t _{DIS} | CL < 5pF | | | 3 | cycles |
| Start-up Time | t _{START-UP} | | | | 2 | ms |
| TCXO Clock Clipped Sine Wave Input Voltage Swing Level | V _{INpp} | VDD = 1.8V, should connect to CLKIN through AC coupling and bias circuit | | 0.8 | | V |

VDD = 2.5V ±5%; for 5PB1213 / 1214 / 1216, ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|-----------------------------------|---|------|------|------|--------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.5 to 2.0V, C _L = 5pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.0 to 0.5V, C _L = 5pF | | 0.6 | 1.0 | ns |
| Propagation Delay | Note 1 | Note 1 | 1.7 | 2.2 | 2.7 | ns |
| Buffer Additive Phase Jitter, RMS | | 26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz | | 280 | | fs |
| | | 125MHz LVCMOS input, Integration Range: 12kHz to 20MHz | | 30 | | fs |
| Output to Output Skew | t _{SKEWO-O} | Note 2, Rising edges at VDD/2 | | 20 | 50 | ps |
| Device to Device Skew | t _{SKEWD-D} | Rising edges at VDD/2 | | | 200 | ps |
| Delay for Output Enable / Disable Time ENABLEx to BCLKn | t _{EN} /t _{DIS} | CL < 5pF | | | 3 | cycles |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| TCXO Clock Clipped Sine Wave Input Voltage Swing Level | V _{INpp} | VDD = 2.5V, should connect to CLKIN through AC coupling and bias circuit | | 0.8 | | V |

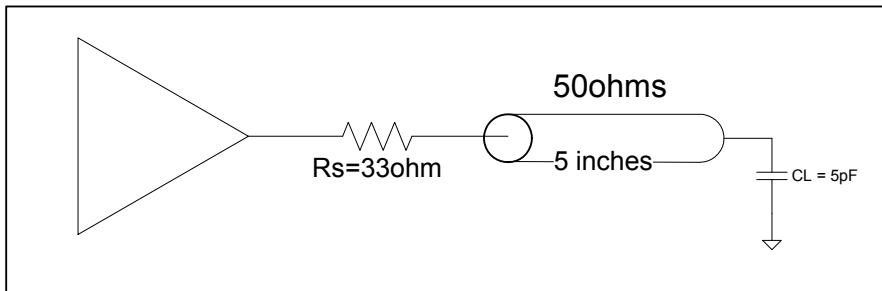
VDD = 3.3V ±5%; for 5PB1213 / 1214 / 1216, ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|-----------------------------------|--|------|------|------|--------|
| Input Frequency | | | 0 | | 200 | MHz |
| Output Rise Time | t _{OR} | 0.66 to 2.64V, C _L = 5pF | | 0.6 | 1.0 | ns |
| Output Fall Time | t _{OF} | 2.64 to 0.66V, C _L = 5pF | | 0.6 | 1.0 | ns |
| Propagation Delay | Note 1 | Note 1 | 1.4 | 1.9 | 2.4 | ns |
| Buffer Additive Phase Jitter, RMS | | 26MHz TCXO clipped sine wave input, Integration Range: 12kHz to 20MHz | | 377 | | fs |
| | | 125MHz LVCMOS input, Integration Range: 12kHz to 20MHz | | 18 | | fs |
| Output to Output Skew | t _{SKEWO-O} | Note 2, Rising edges at VDD/2 | | 20 | 50 | ps |
| Device to Device Skew | t _{SKEWD-D} | Rising edges at VDD/2 | | | 200 | ps |
| Delay for Output Enable / Disable Time ENABLEx to BCLKn | t _{EN} /t _{DIS} | CL < 5pF | | | 3 | cycles |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| TCXO Clock Clipped Sine Wave Input Voltage Swing Level | V _{INpp} | VDD = 3.3V, should connect to CLKIN through AC coupling and bias circuit | | 0.5 | | V |

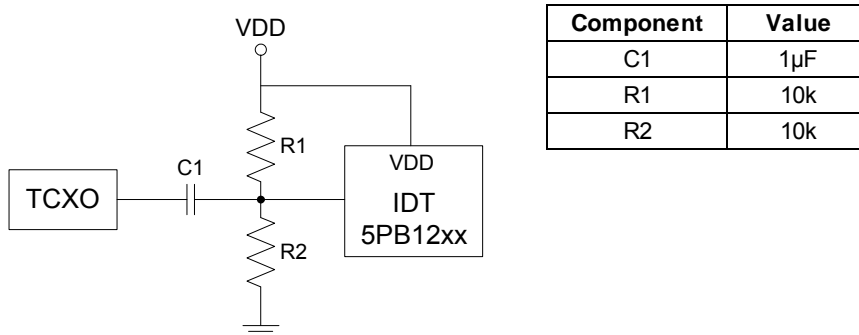
Notes:

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.

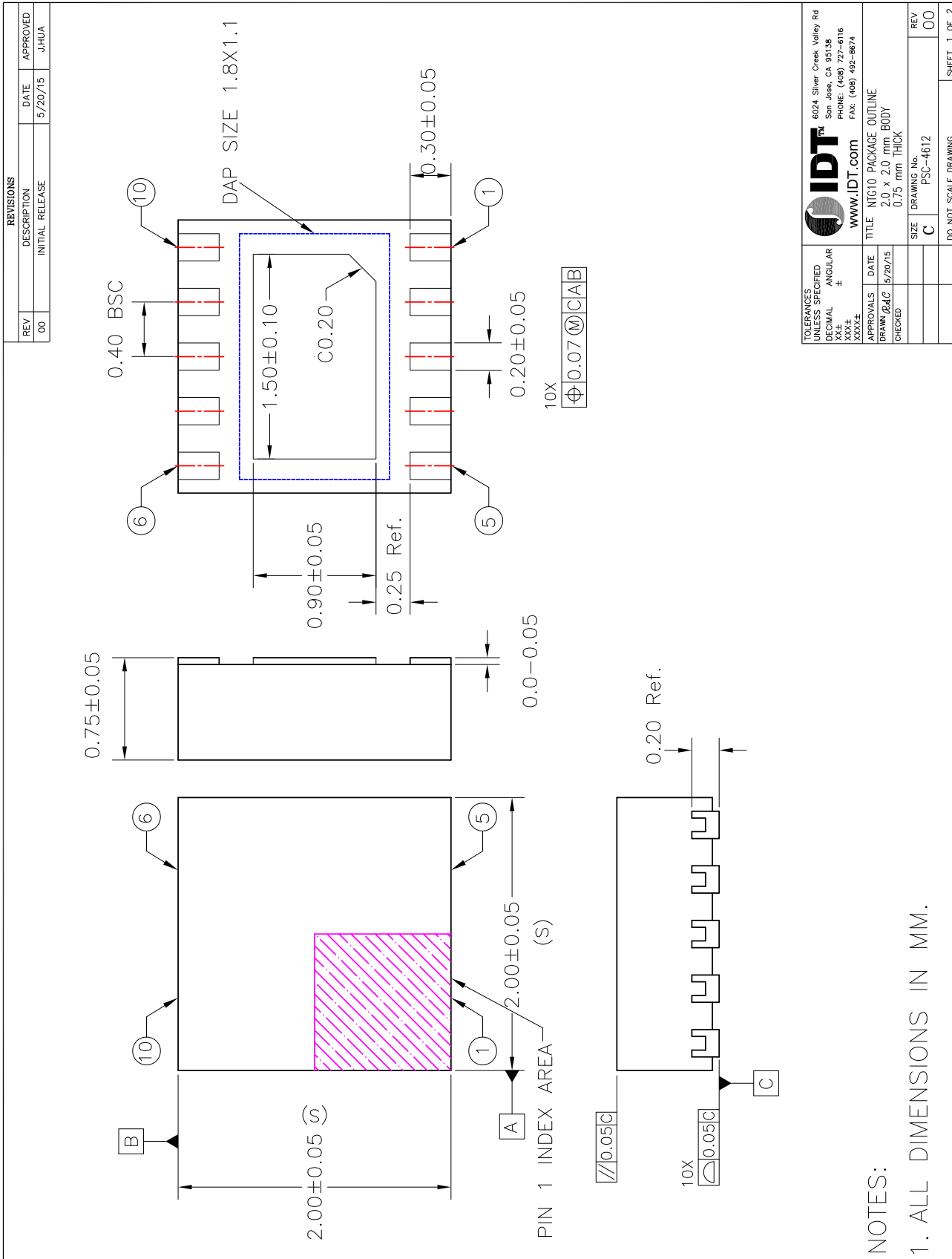
Test Load and Circuit



AC Coupling and Bias Circuit



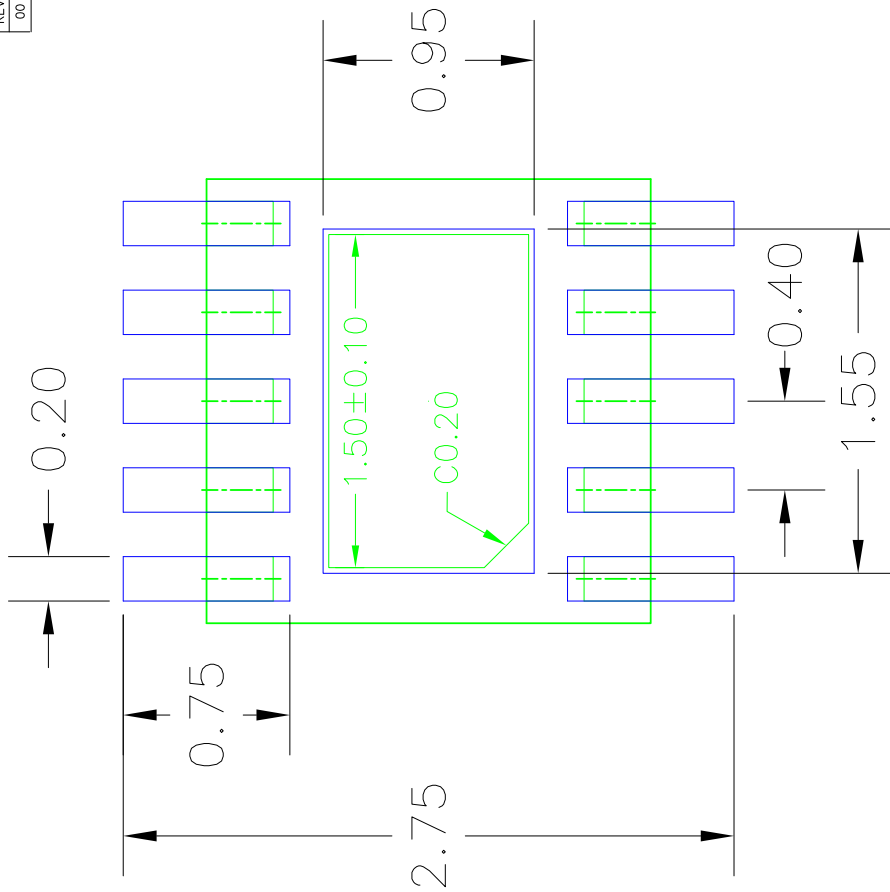
Package Outline Drawings (5PB1203 / 5PB1213 10-pin DFN)



| | | | |
|--|--|-------------|------------------------------------|
| TOLERANCES UNLESS SPECIFIED DECIMAL ± XXX ± XXX ± | IDT™ 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 WWW.IDT.COM FAX: (408) 492-8674 | | |
| | APPROVALS | DATE | TITLE |
| | DRAWN: QAC | 5/20/15 | 10G10 PACKAGE OUTLINE |
| | CHECKED | | 2.0 x 2.0 mm BODY 0.75 mm THICK |
| | SIZE | DRAWING No. | REV |
| | C | PSC-4612 | 00 |
| | DO NOT SCALE DRAWING | | SHEET 1 OF 2 |

Package Outline Drawings (5PB1203 / 5PB1213 10-pin DFN), cont.

| REVISIONS | | |
|-----------|-----------------|---------|
| REV | DESCRIPTION | DATE |
| 00 | INITIAL RELEASE | 5/20/15 |
| | APPROVED | J.HUA |



RECOMMENDED LAND PATTERN DIMENSION

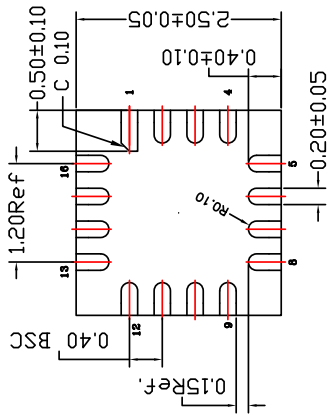
NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

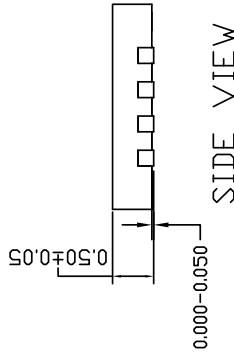
| | | |
|--|-------------|--------------|
| TOLERANCES UNLESS SPECIFIED | DECIMAL | ANGULAR |
| XXX± | | ± |
| XXXX± | | |
| APPROVALS | DATE | |
| DRAWN/BJC | 5/20/15 | |
| CHECKED | | |
| | | |
| 6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 WWW.IDT.COM | | |
| TITLE: 1010 PACKAGE OUTLINE SIZE: 2.0 x 2.0 mm BODY THICK: 0.75 mm THICK | | |
| SIZE | DRAWING No. | REV |
| C | PSC-4612 | 00 |
| DO NOT SCALE DRAWING | | SHEET 2 OF 2 |

Package Outline Drawings (5PB1204 / 5PB1214 16-pin VFQFPN)

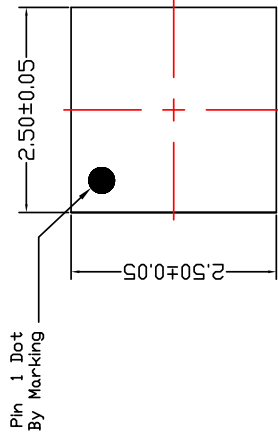
| REVISIONS | | | |
|-----------|------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/03/14 | JH |
| 01 | ADD PIN1 CHAMFER | 12/11/14 | JH |



BOTTOM VIEW



SIDE VIEW



TOP VIEW

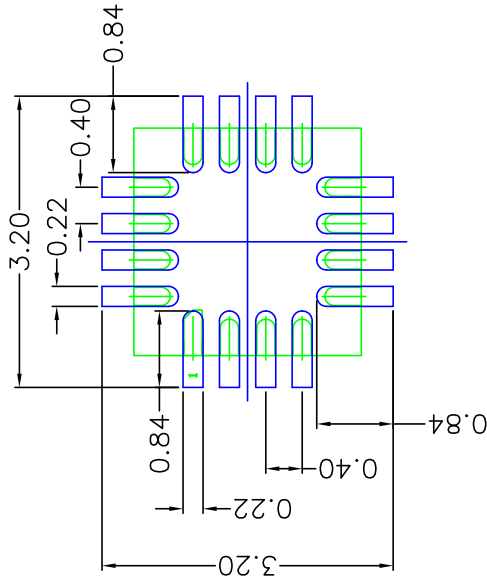
NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

| | | | |
|-----------------------------|---|----------|----------------------|
| TOLERANCES UNLESS SPECIFIED | 6024 Silver Creek Valley Road San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 | | |
| DECIMAL | WWW.IDT.COM | | |
| ANGULAR | TITLE CMG 16 PACKAGE OUTLINE | | |
| ±1° | 2.5 x 2.5 mm BODY | | |
| X± | 0.40 mm PITCH VFQFN | | |
| XX± | APPROVALS | DATE | REV |
| XXX± | | 04/03/14 | 01 |
| XXXX± | DRAWN BY | CHECKED | SIZE |
| | | | C |
| | | | DRAWING No. PSC-4478 |
| | | | DO NOT SCALE DRAWING |
| | | | SHEET 1 OF 2 |

Package Outline Drawings (5PB1204 / 5PB1214 16-pin VFQFPN), cont.

| REVISIONS | | | |
|-----------|------------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/03/14 | JH |
| 01 | ADD PIN1 CHAMFER | 12/11/14 | JH |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE IS SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | | |
|--|----------------|---|------------------------------|--|
| TOLERANCES UNLESS SPECIFIED DECIMAL XX. XXX± | ANGULAR ±1° | IDT™ 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 WWW.IDT.COM | TITLE CMG 16 PACKAGE OUTLINE | |
| | APPROVALS | | DATE 04/03/14 | 2.5 x 2.5 mm BODY 0.40 mm PITCH VFQFN |
| DRAWN JSC | CHECKED | SIZE C | DRAWING No. PSC-4478 | REV 01 |
| DO NOT SCALE DRAWING | | | SHEET 2 OF 2 | |

Package Outline Drawings (5PB1206 / 5PB1216 20-pin VFQFPN)

| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 3/30/16 | JH |

TOP VIEW

SIDE VIEW

BOTTOM VIEW

| DIMENSION | | | |
|-----------|------------|------|------|
| Symbol | Min | Nom | Max |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.20 Ref | | |
| b | 0.17 | 0.20 | 0.25 |
| e | 0.40 BASIC | | |
| N | 20 | | |
| ND | 5 | | |
| NE | 5 | | |
| D | 3.00 BASIC | | |
| E | 3.00 BASIC | | |
| D2 | 1.55 | 1.65 | 1.75 |
| E2 | 1.55 | 1.65 | 1.75 |
| L | 0.30 | 0.40 | 0.50 |

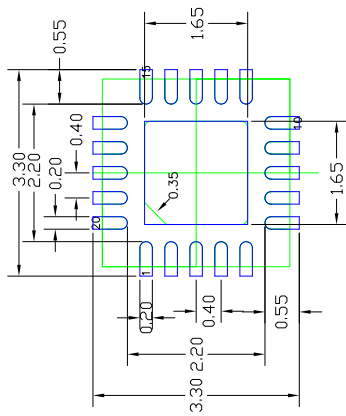
NOTE :

1. ALL DIMENSIONS ARE IN mm; ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05 mm.
3. WARPAGE SHALL NOT EXCEED 0.05 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. REFER JEDEC MO-220.

| | |
|---|-------------------------------|
| TOLERANCES UNLESS SPECIFIED | 6024 Silver Creek Valley Road |
| DECIMAL | San Jose CA 95138 |
| ANGULAR | PHONE: (408) 284-8200 |
| ± | WWW.IDT.COM |
| XXX± | FAX: (408) 284-8591 |
| APPROVALS | DATE |
| DRAWN ØAG | 3/30/16 |
| CHECKED | |
| | |
| TITLE ND/NDG 20 PACKAGE OUTLINE 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ 0.40 PITCH QFN | |
| SIZE | DRAWING No. |
| C | PSC-4179-02 |
| REV | 00 |
| DO NOT SCALE DRAWING | |
| SHEET 1 OF 2 | |

Package Outline Drawings (5PB1206 / 5PB1216 20-pin VFQFPN), cont.

| REVISIONS | | |
|-----------|-----------------|----------|
| REV | DESCRIPTION | DATE |
| 00 | INITIAL RELEASE | 3/30/16 |
| | | APPROVED |
| | | JH |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

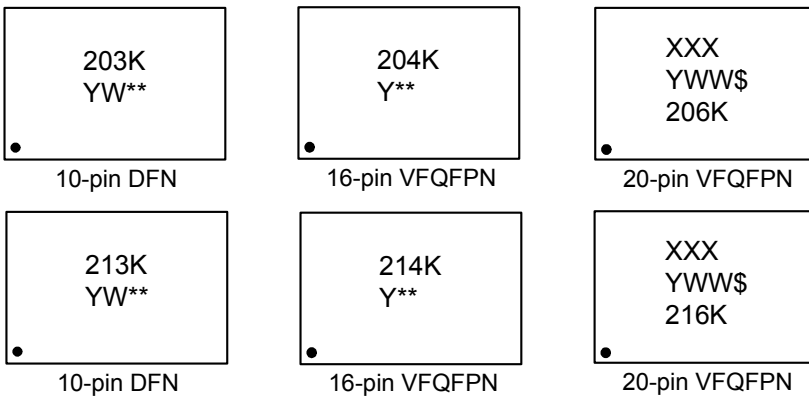
| | | |
|---|-------------|---|
| TOLERANCES UNLESS SPECIFIED DECIMAL X± XXX± XXX± | ANGULAR | ±1° |
| | APPROVALS | DATE |
| | DRAWN | 04G |
| | CHECKED | 3/30/16 |
| 6024 Silver Creek Valley Road San Jose CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-8591 www.IDT.com | | TITLE ND/NDG 20 PACKAGE OUTLINE 3.0 x 3.0 mm BODY, EPAD 1.65 mm SQ 0.40 PITCH QFN |
| SIZE | DRAWING No. | REV |
| C | PSC-4179-02 | 00 |
| DO NOT SCALE DRAWING | | SHEET 2 OF 2 |

Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|---------------|---------------|
| 5PB1203NTGK | Cut Tape | 10-pin DFN | -40 to +105°C |
| 5PB1203NTGK8 | Tape and Reel | 10-pin DFN | -40 to +105°C |
| 5PB1213NTGK | Cut Tape | 10-pin DFN | -40 to +105°C |
| 5PB1213NTGK8 | Tape and Reel | 10-pin DFN | -40 to +105°C |
| 5PB1204CMGK | Cut Tape | 16-pin VFQFPN | -40 to +105°C |
| 5PB1204CMGK8 | Tape and Reel | 16-pin VFQFPN | -40 to +105°C |
| 5PB1214CMGK | Cut Tape | 16-pin VFQFPN | -40 to +105°C |
| 5PB1214CMGK8 | Tape and Reel | 16-pin VFQFPN | -40 to +105°C |
| 5PB1206NDGK | Tube | 20-pin VFQFPN | -40 to +105°C |
| 5PB1206NDGK8 | Tape and Reel | 20-pin VFQFPN | -40 to +105°C |
| 5PB1216NDGK | Tube | 20-pin VFQFPN | -40 to +105°C |
| 5PB1216NDGK8 | Tape and Reel | 20-pin VFQFPN | -40 to +105°C |

“G” after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Marking Diagrams



Notes:

1. “**” is the lot number.
2. “YWW”, “YW”, or “Y” are the last digit(s) of the year and week that the part was assembled.
3. “\$” denotes mark code.
4. “K” denotes extended temperature range device.
5. “XXX” denotes last three characters of Asm lot.

Revision History

| Date | Description of Change |
|-------------------|---|
| February 28, 2018 | 1. Updated CLKIN input high and low voltage ratings in DC characterization tables. 2. Updated Absolute Maximum supply voltage (VDD) from 3.465V to 3.8V. |
| April 10, 2017 | 1. Updated Operating Supply Current and Operating Voltage values in DC electrical characteristics tables. 2. Updated Propagation Delay and Output skew values in AC electrical characteristics tables. 3. Updated package outline drawings. 4. Updated legal disclaimer. |
| July 11, 2016 | Initial release. |



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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