Document Number: A2V09H525-04N
Rev. 0, 03/2017

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 120 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 720 to 960 MHz.

900 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 1.1 Vdc, P_{out} = 120 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	18.9	57.8	7.5	–28.9
940 MHz	18.9	56.7	7.3	–32.4
960 MHz	18.7	54.8	6.9	–34.8

780 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 48 Vdc, I_{DQA} = 700 mA, V_{GSB} = 0.9 Vdc, P_{out} = 120 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

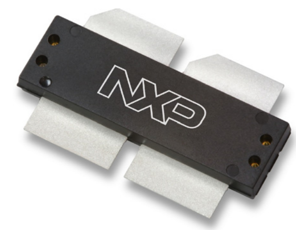
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
758 MHz	18.1	56.2	7.5	–28.2
780 MHz	18.1	54.7	7.5	–29.3
803 MHz	17.7	52.5	7.2	–32.5

Features

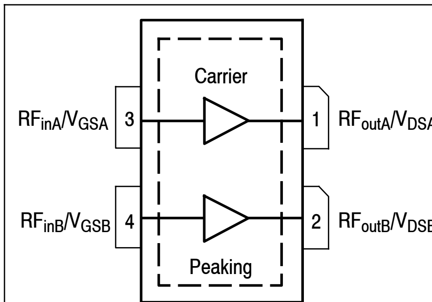
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2V09H525-04NR6

720–960 MHz, 120 W AVG., 48 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-1230-4L PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +105	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	55, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range [1,2]	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value [2,3]	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 120 W Avg., W-CDMA, 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 1.1 Vdc, 940 MHz	$R_{\theta JC}$	0.23	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics [4]					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 105 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 55 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 140 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Gate Quiescent Voltage (V_{DD} = 48 Vdc, I_{DA} = 688 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.1	2.5	2.9	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.4 Adc)	$V_{DS(on)}$	0.1	0.3	0.5	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 280 μAdc)	$V_{GS(th)}$	1.3	1.8	2.3	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.8 Adc)	$V_{DS(on)}$	0.1	0.3	0.5	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1,2] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 1.1 Vdc, P_{out} = 120 W Avg., f = 940 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	18.1	18.9	21.1	dB
Drain Efficiency	η_D	51.0	56.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.6	7.3	—	dB
Adjacent Channel Power Ratio	ACPR	—	–32.4	–28.0	dBc
Load Mismatch [2] (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 688 mA, V_{GSB} = 1.1 Vdc, f = 940 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 55 Vdc, 245 W Pulsed CW Output Power (3dB Backed Off from 492 W Pulsed CW Rated Power)			No Device Degradation		
Typical Performance [2] (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 48 Vdc, I_{DQA} = 688 mA, V_{GSB} = 1.1 Vdc, 920–960 MHz Bandwidth					
P_{out} @ 3 dB Compression Point [3]	P3dB	—	759	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 920–960 MHz frequency range)	Φ	—	–22	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	70	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 120 W Avg.	G_F	—	0.29	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.004	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	$\Delta P1dB$	—	0.014	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2V09H525-04NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L

1. Part internally input matched.
2. Measurement made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

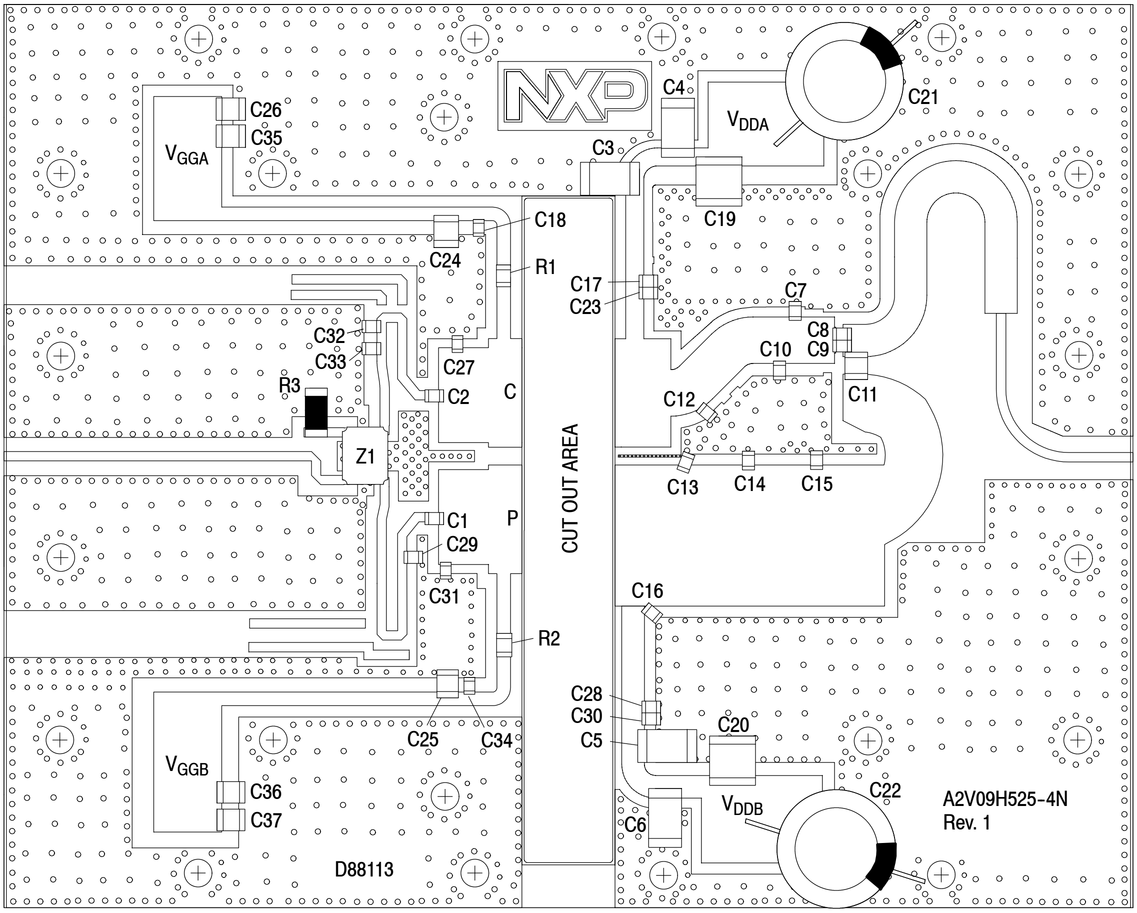


Figure 2. A2V09H525-04NR6 Test Circuit Component Layout

Table 7. A2V09H525-04NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C17, C18, C23, C28, C30, C34	56 pF Chip Capacitor	ATC600F560JT250XT	ATC
C3, C4, C5, C6	4.7 μF Chip Capacitor	C4532X7S2A475M230KB	TDK
C7	3.3 pF Chip Capacitor	ATC600F3R3BT250XT	ATC
C8, C9	5.6 pF Chip Capacitor	ATC600F5R6BT250XT	ATC
C10, C14, C29	6.8 pF Chip Capacitor	ATC600F6R8BT250XT	ATC
C11	56 pF Chip Capacitor	ATC100B560JT500XT	ATC
C12, C16	7.5 pF Chip Capacitor	GQM1875C2E7R5BB12D	Murata
C13	12 pF Chip Capacitor	ATC600F120JT250XT	ATC
C15	10 pF Chip Capacitor	ATC600F100JT250XT	ATC
C19, C20	15 μF Chip Capacitor	C5750X7S2A156M230KB	TDK
C21, C22	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C24, C25	1000 pF Chip Capacitor	ATC800B102JT50XT	ATC
C26, C35, C36, C37	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
C27, C31	8.2 pF Chip Capacitor	ATC600F8R2BT250XT	ATC
C32	1.8 pF Chip Capacitor	ATC600F1R8BT250XT	ATC
C33	1.5 pF Chip Capacitor	ATC600F1R5BT250XT	ATC
R1, R2	3.3 Ω, 1/4 W Chip Resistor	CRCW08053R30JNEA	Vishay
R3	50 Ω, 10 W Termination Chip Resistor	81A7031-50-5F	Florida RF Labs
Z1	800–1000 MHz Band, 90°, 2 dB Asymmetric Coupler	CMX09Q02	Cemax
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D88113	MTL

TYPICAL CHARACTERISTICS — 920–960 MHz

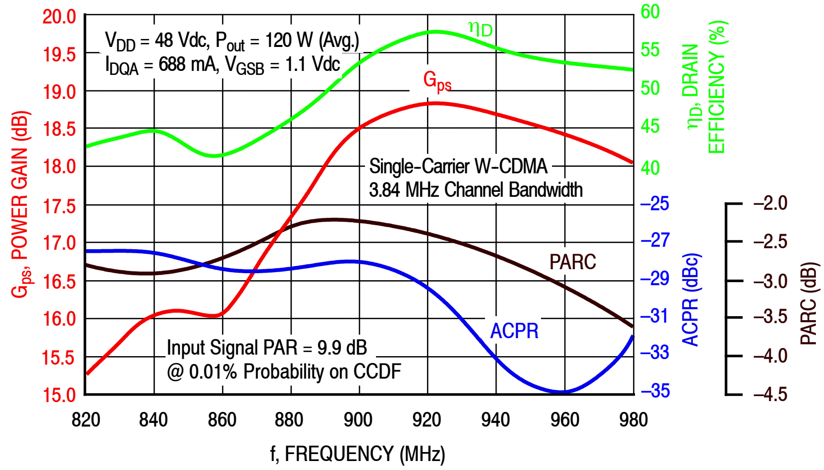


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 120 Watts Avg.

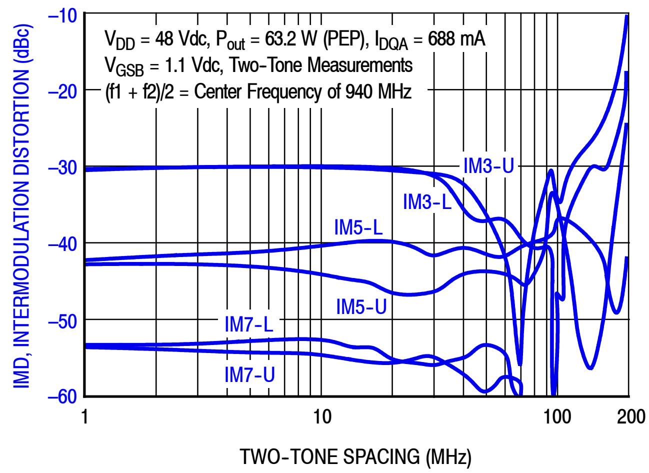


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

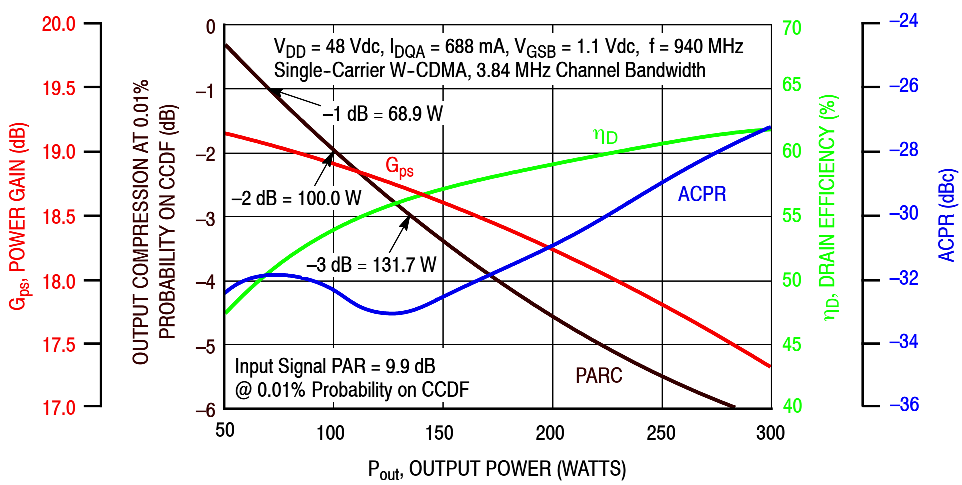


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 920–960 MHz

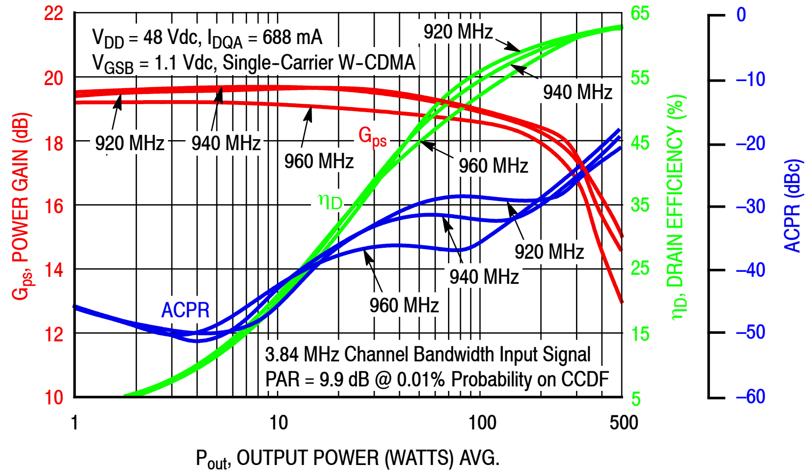


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

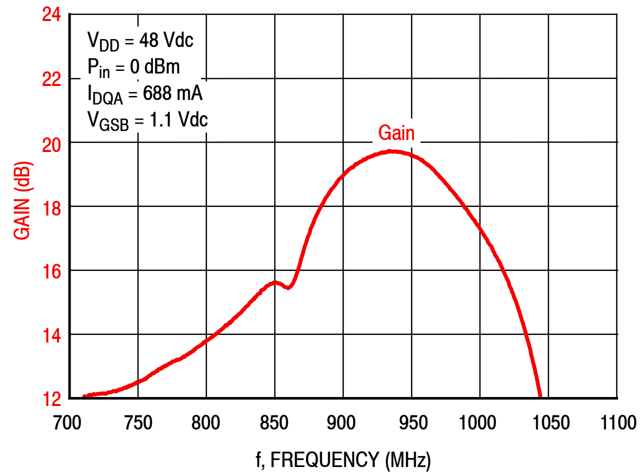


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 691 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	5.02 – j5.30	5.03 + j6.04	2.26 + j0.05	20.3	54.2	261	59.6	–14
940	5.83 – j5.60	6.06 + j6.45	2.31 – j0.06	20.2	54.1	256	58.2	–14
960	7.20 – j6.14	7.45 + j6.86	2.36 – j0.17	20.2	54.0	252	57.5	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	5.02 – j5.30	5.02 + j6.91	2.44 – j0.08	18.2	54.8	304	60.3	–19
940	5.83 – j5.60	6.25 + j7.50	2.49 – j0.22	18.1	54.8	299	58.6	–19
960	7.20 – j6.14	7.94 + j8.07	2.55 – j0.34	18.0	54.7	295	57.8	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 9. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 691 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	5.02 – j5.30	4.33 + j6.18	1.69 + j1.66	22.6	52.6	181	73.3	–21
940	5.83 – j5.60	5.21 + j6.71	1.75 + j2.12	23.3	51.5	142	70.4	–20
960	7.20 – j6.14	6.77 + j7.07	1.97 + j1.45	22.4	52.6	181	70.1	–18

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	5.02 – j5.30	4.34 + j6.97	1.69 + j1.66	20.6	53.1	206	73.6	–30
940	5.83 – j5.60	5.37 + j7.66	1.55 + j1.48	20.4	53.0	202	73.1	–31
960	7.20 – j6.14	7.26 + j8.27	1.97 + j1.45	20.4	53.2	209	70.1	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

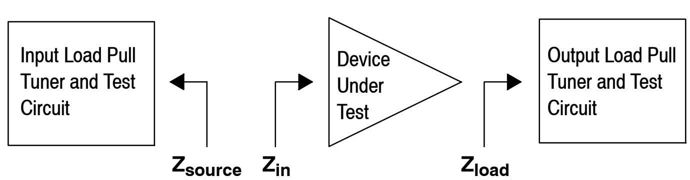


Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.49 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.08 – j2.73	2.20 + j3.85	0.91 – j0.38	15.6	57.3	540	61.5	–22
940	2.49 – j2.81	2.66 + j4.18	0.92 – j0.47	15.7	57.2	529	60.2	–21
960	2.70 – j3.04	3.34 + j4.59	0.97 – j0.57	15.7	57.2	520	59.4	–21

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.08 – j2.73	2.20 + j4.24	1.00 – j0.52	13.4	57.9	622	61.4	–28
940	2.49 – j2.81	2.71 + j4.66	1.02 – j0.60	13.5	57.9	610	60.3	–27
960	2.70 – j3.04	3.51 + j5.17	1.05 – j0.69	13.4	57.8	602	59.4	–27

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

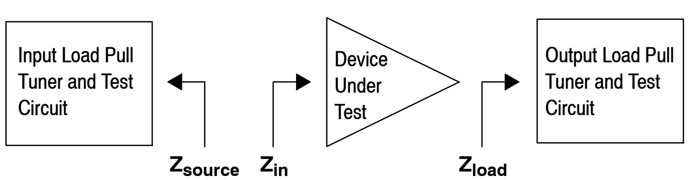
Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 0.49 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.08 – j2.73	1.84 + j3.75	1.01 + j0.55	16.9	55.4	348	74.8	–26
940	2.49 – j2.81	2.37 + j4.18	1.40 + j0.30	16.6	55.8	383	73.2	–21
960	2.70 – j3.04	2.76 + j4.48	0.94 + j0.38	17.0	55.2	332	71.9	–26

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	2.08 – j2.73	1.92 + j4.16	1.13 + j0.42	14.8	56.4	439	72.6	–33
940	2.49 – j2.81	2.46 + j4.65	1.40 + j0.27	14.6	56.5	450	72.9	–28
960	2.70 – j3.04	3.02 + j5.07	0.99 + j0.30	14.9	56.1	407	71.3	–35

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 940 MHz

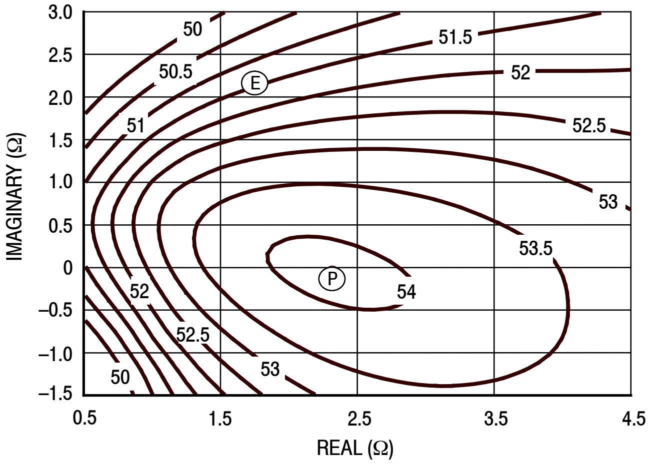


Figure 8. P1dB Load Pull Output Power Contours (dBm)

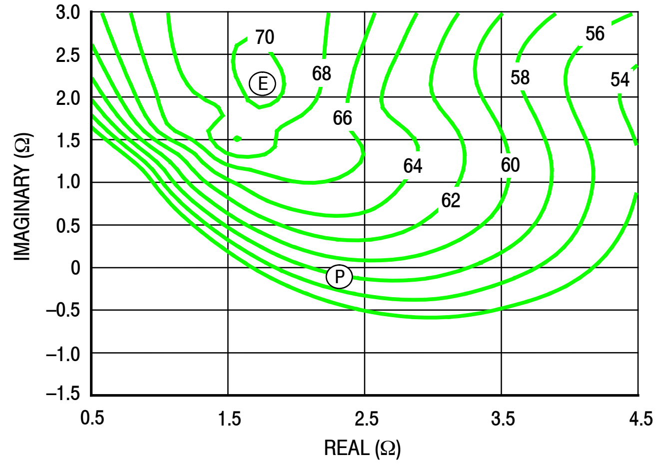


Figure 9. P1dB Load Pull Efficiency Contours (%)

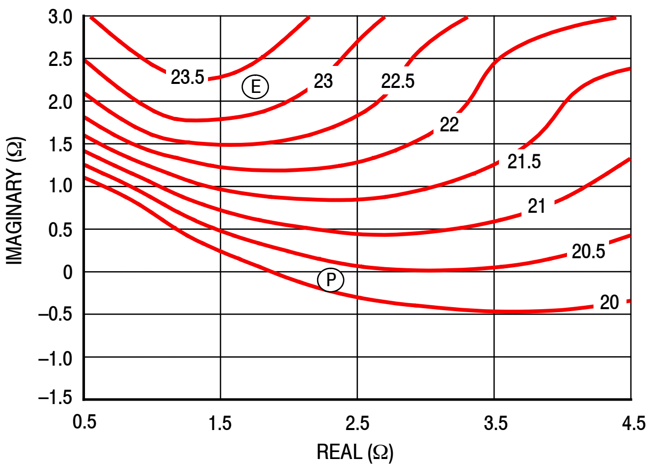


Figure 10. P1dB Load Pull Gain Contours (dB)

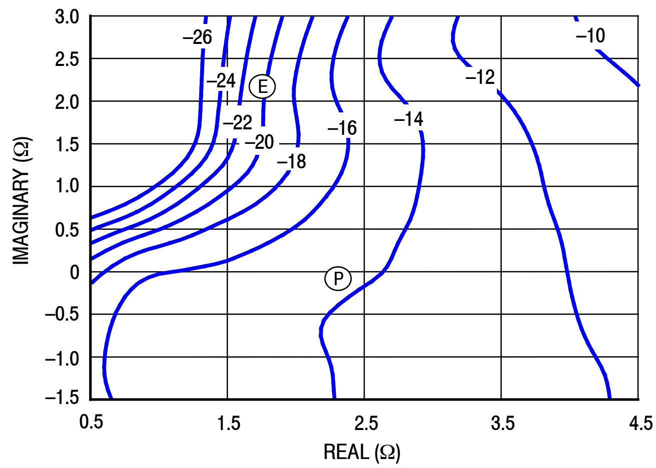


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 940 MHz

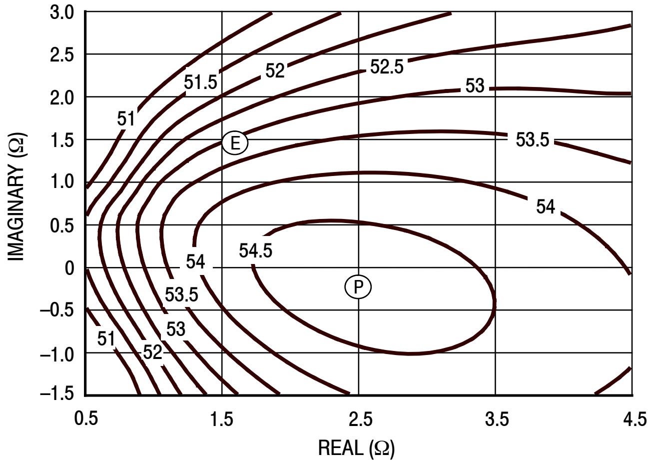


Figure 12. P3dB Load Pull Output Power Contours (dBm)

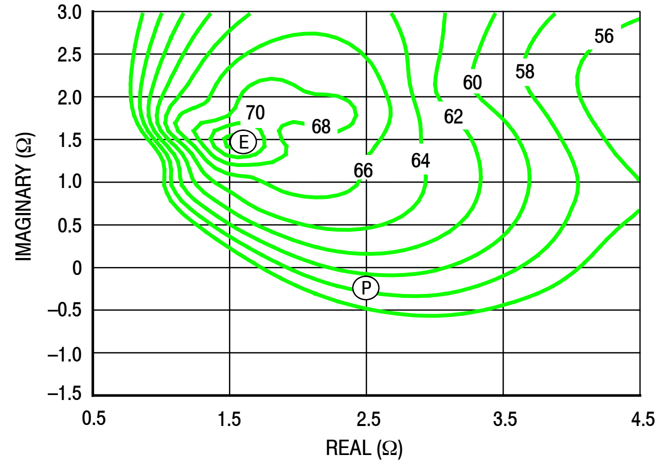


Figure 13. P3dB Load Pull Efficiency Contours (%)

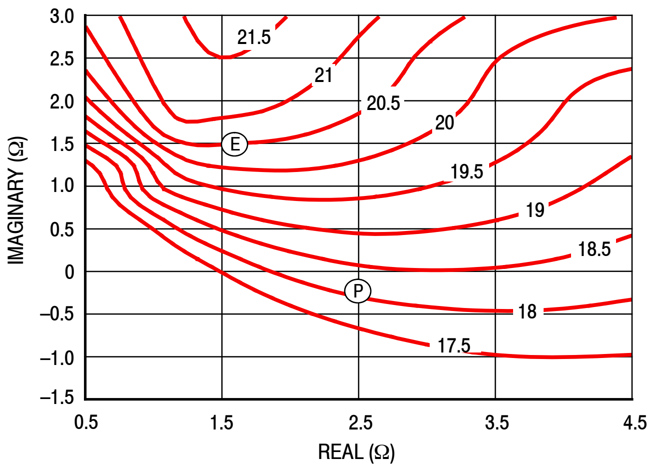


Figure 14. P3dB Load Pull Gain Contours (dB)

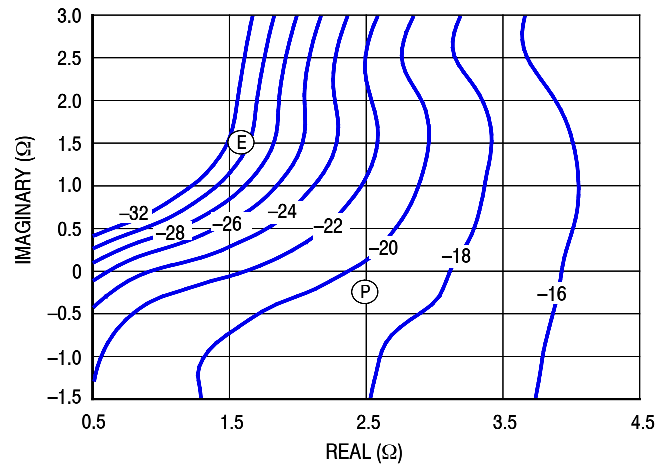


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 940 MHz

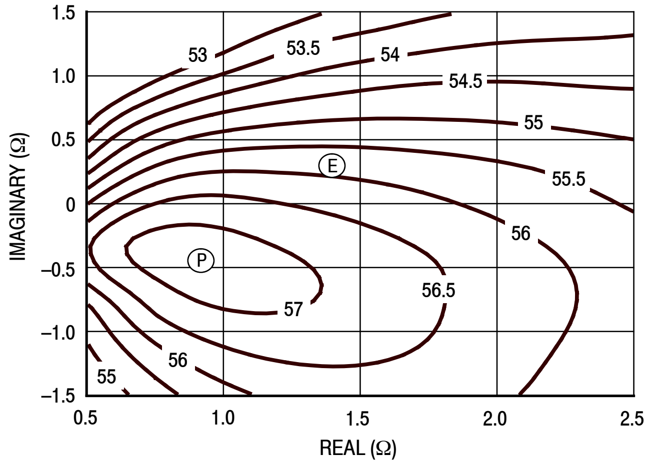


Figure 16. P1dB Load Pull Output Power Contours (dBm)

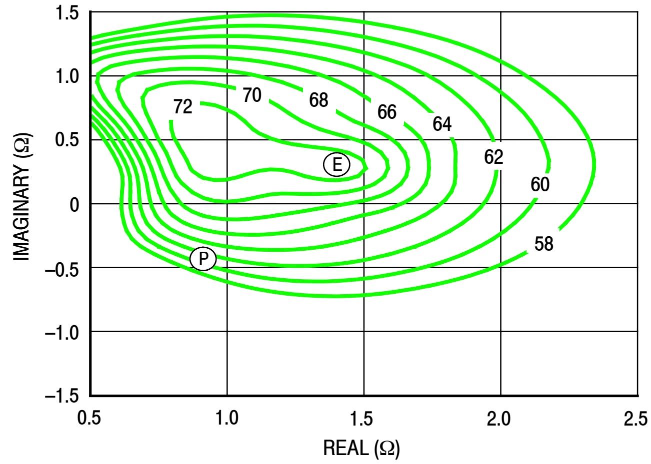


Figure 17. P1dB Load Pull Efficiency Contours (%)

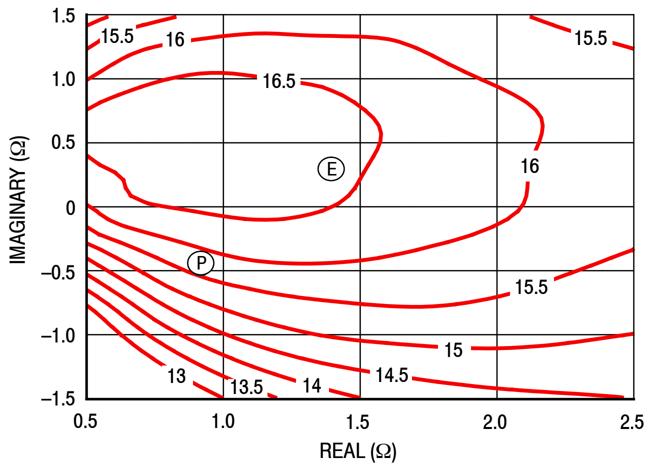


Figure 18. P1dB Load Pull Gain Contours (dB)

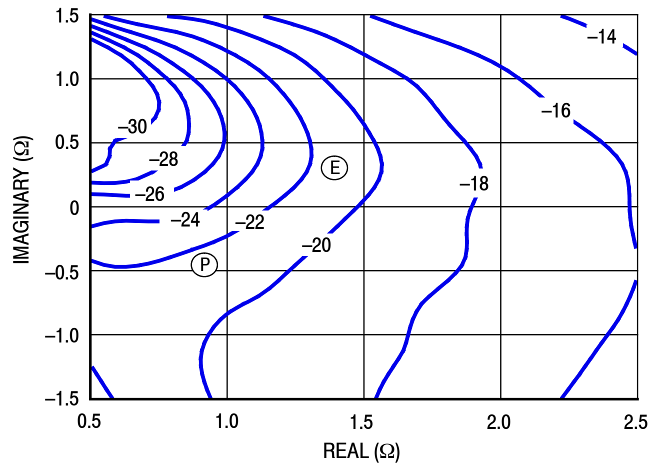


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 940 MHz

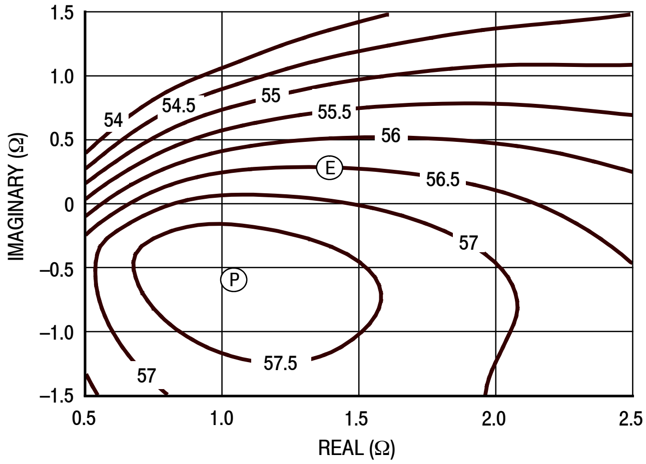


Figure 20. P3dB Load Pull Output Power Contours (dBm)

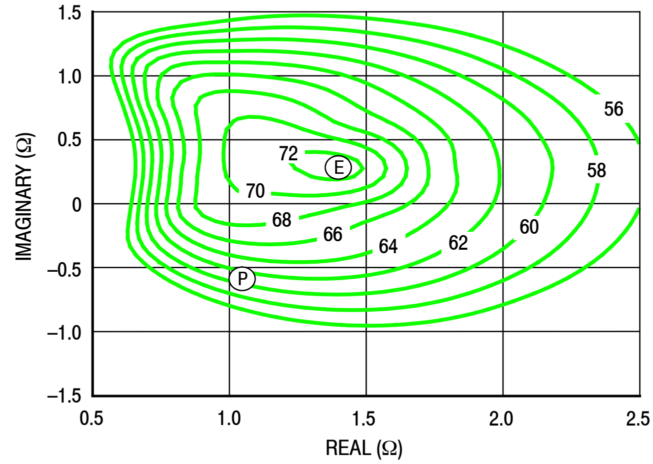


Figure 21. P3dB Load Pull Efficiency Contours (%)

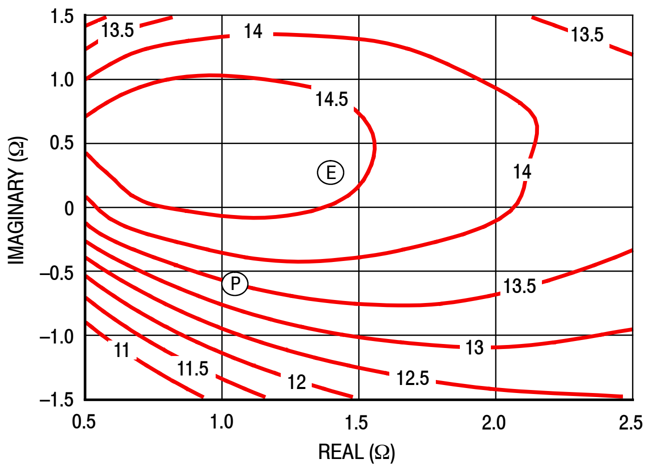


Figure 22. P3dB Load Pull Gain Contours (dB)

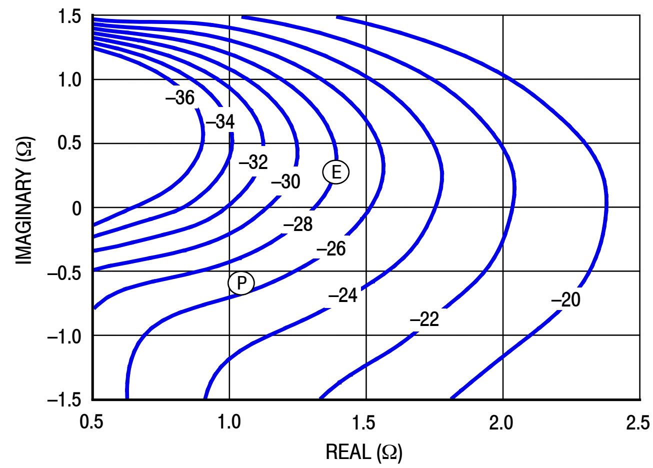


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

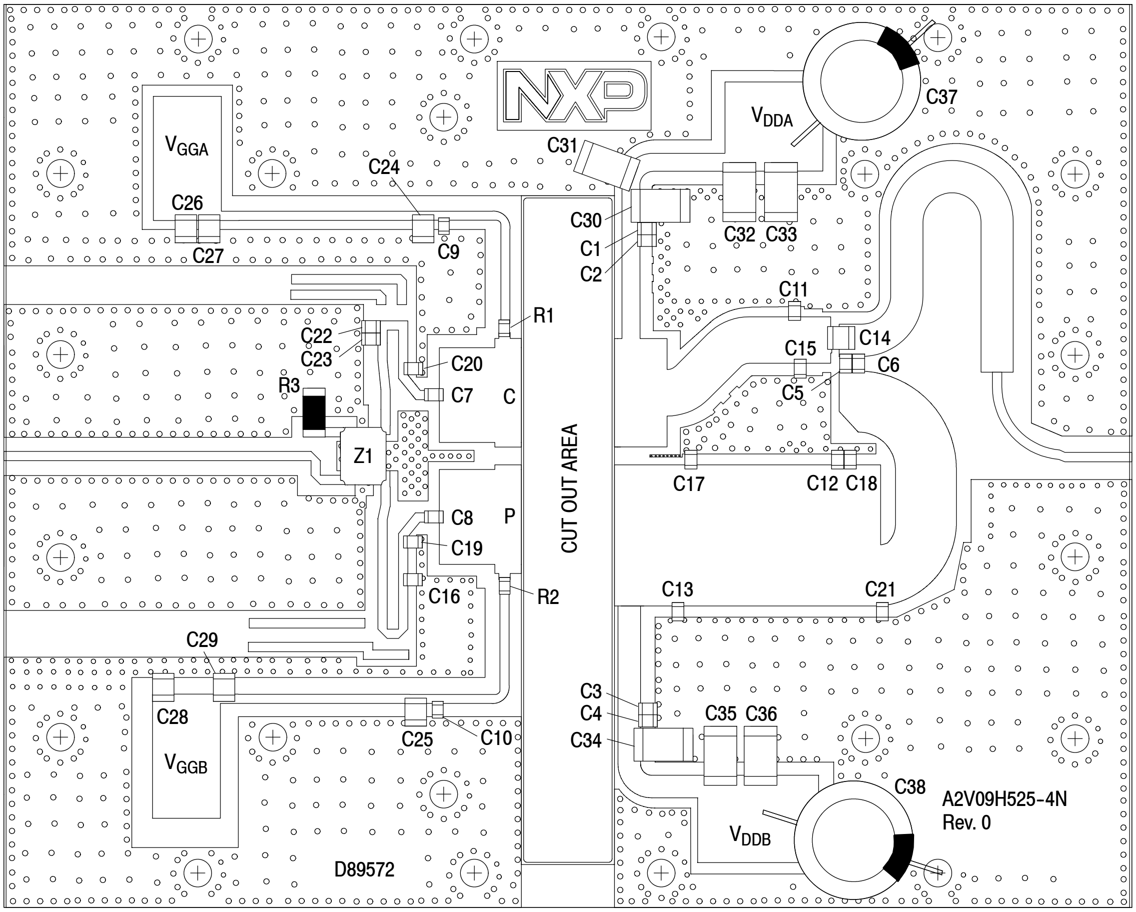


Figure 24. A2V09H525-04NR6 Test Circuit Component Layout — 758–803 MHz

Table 12. A2V09H525-04NR6 Test Circuit Component Designations and Values — 758–803 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7, C8, C9, C10	56 pF Chip Capacitor	ATC600F560JT250XT	ATC
C11, C12, C13	6.8 pF Chip Capacitor	ATC600F6R8BT250XT	ATC
C14	22 pF Chip Capacitor	ATC800B220JT500XT	ATC
C15, C16	7.5 pF Chip Capacitor	GQM1875C2E7R5BB12D	Murata
C17, C18	12 pF Chip Capacitor	ATC600F120JT250XT	ATC
C19, C20	10 pF Chip Capacitor	ATC600F100JT250XT	ATC
C21	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
C22	2.0 pF Chip Capacitor	ATC600F2R0BT250XT	ATC
C23	2.4 pF Chip Capacitor	ATC600F2R4BT250XT	ATC
C24, C25	1000 pF Chip Capacitor	ATC800B102JT50XT	ATC
C26, C27, C28, C29	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
C30, C31, C32, C33, C34, C35, C36	15 μF Chip Capacitor	C5750X7S2A156M230KB	TDK
C37, C38	220 μF, 100 V Electrolytic Capacitor	MCGPR100V227M16X26-RH	Multicomp
R1, R2	4.75 Ω, 1/4 W Chip Resistor	CRCW12064R75FNEA	Vishay
R3	50 Ω, 10 W Termination Chip Resistor	81A7031-50-5F	Florida RF Labs
Z1	800–1000 MHz Band, 90°, 2 dB Asymmetric Coupler	CMX09Q02	Cemax
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D89572	MTL

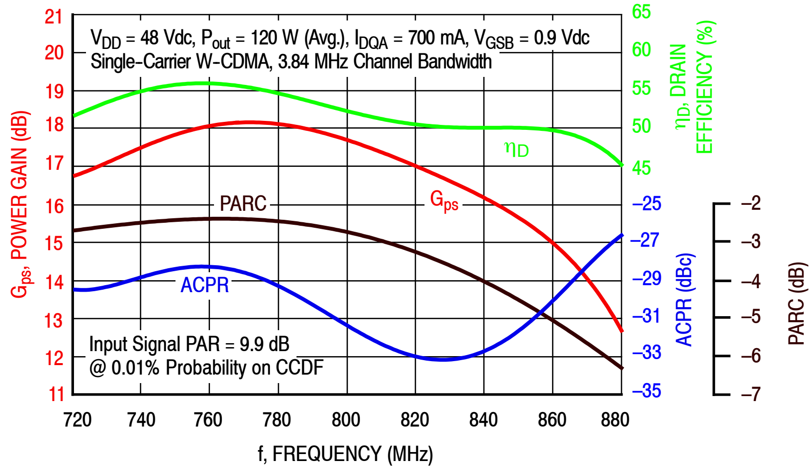


Figure 25. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 120 Watts Avg.

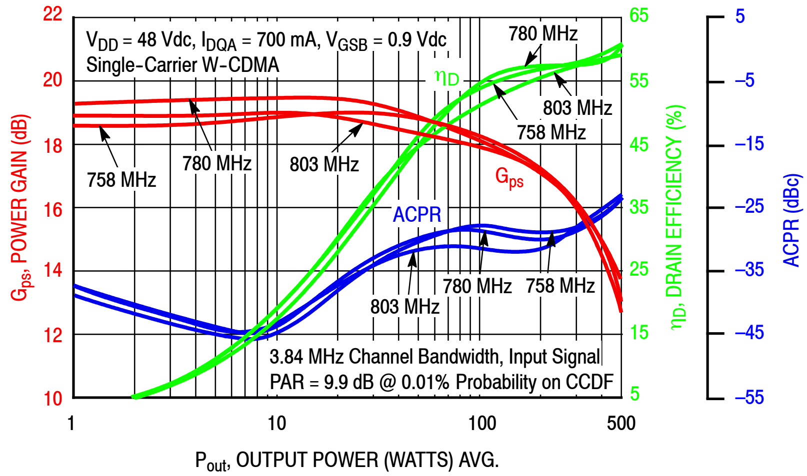


Figure 26. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

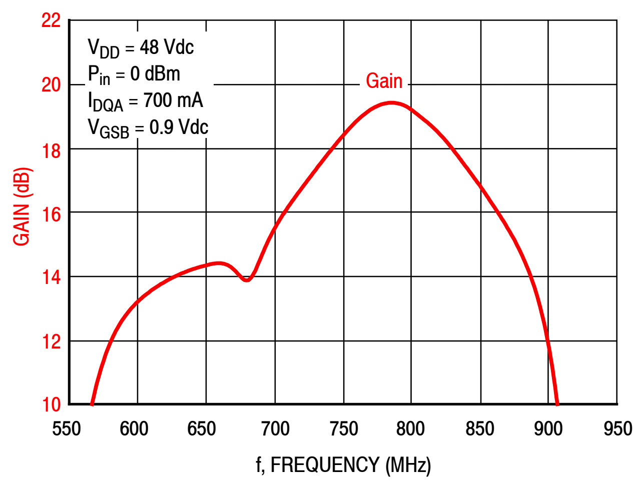


Figure 27. Broadband Frequency Response

Table 13. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, I_{DQA} = 712 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.26 – j2.42	3.95 + j2.45	2.65 + j0.05	19.3	54.4	277	59.8	–10
780	3.25 – j3.06	3.37 + j2.82	2.09 + j0.53	19.9	54.4	273	60.3	–10
822	3.49 – j3.60	3.40 + j3.55	2.03 + j0.38	20.3	54.4	277	61.9	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.26 – j2.42	3.66 + j2.68	2.70 – j0.04	17.2	55.0	315	60.4	–12
780	3.25 – j3.06	3.15 + j3.17	2.28 + j0.45	17.9	55.1	324	64.1	–14
822	3.49 – j3.60	3.19 + j3.98	2.25 + j0.24	18.2	55.0	318	63.4	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 14. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, I_{DQA} = 712 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.26 – j2.42	3.39 + j2.32	2.35 + j1.99	21.3	52.9	196	67.8	–16
780	3.25 – j3.06	2.89 + j3.10	2.34 + j2.64	22.5	52.5	176	71.9	–15
822	3.49 – j3.60	2.90 + j3.71	2.01 + j2.03	22.6	52.8	189	72.2	–19

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	4.26 – j2.42	3.31 + j2.52	2.36 + j1.67	19.0	53.9	243	67.8	–19
780	3.25 – j3.06	2.93 + j3.40	2.95 + j2.28	19.8	53.8	238	71.6	–17
822	3.49 – j3.60	2.93 + j4.04	2.37 + j1.64	20.1	54.0	251	72.1	–22

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

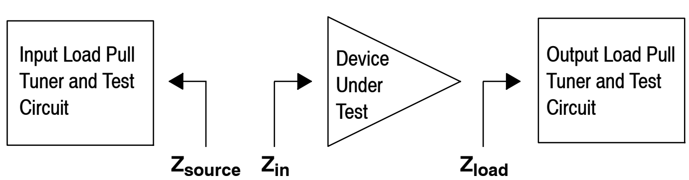


Table 15. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 48 Vdc, V_{GSB} = 1.4 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	1.87 – j1.72	1.99 + j1.63	1.12 – j0.24	15.9	57.6	576	63.1	–21
780	1.68 – j1.75	1.67 + j1.81	1.04 – j0.36	16.6	57.7	585	63.2	–22
822	1.64 – j2.13	1.57 + j2.10	0.99 – j0.54	17.0	57.6	576	62.9	–23

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	1.87 – j1.72	1.79 + j1.78	1.21 – j0.35	13.9	58.1	653	64.5	–24
780	1.68 – j1.75	1.50 + j1.99	1.08 – j0.40	14.6	58.2	666	65.5	–27
822	1.64 – j2.13	1.42 + j2.35	1.10 – j0.65	14.9	58.2	654	63.9	–28

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

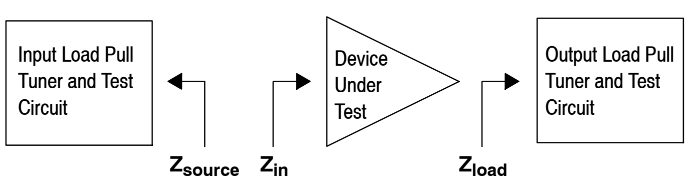
Table 16. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 48 Vdc, V_{GSB} = 1.4 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	1.87 – j1.72	1.75 + j1.52	1.33 + j0.89	17.0	55.7	374	75.2	–26
780	1.68 – j1.75	1.38 + j1.72	1.24 + j0.88	18.1	55.3	341	76.8	–27
822	1.64 – j2.13	1.21 + j2.00	1.02 + j0.71	18.6	54.8	300	75.7	–31

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
733	1.87 – j1.72	1.63 + j1.67	1.38 + j0.87	15.0	56.2	421	73.9	–30
780	1.68 – j1.75	1.34 + j1.95	1.47 + j0.56	15.9	56.7	466	74.9	–30
822	1.64 – j2.13	1.23 + j2.26	1.24 + j0.39	16.4	56.4	435	74.2	–34

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 780 MHz

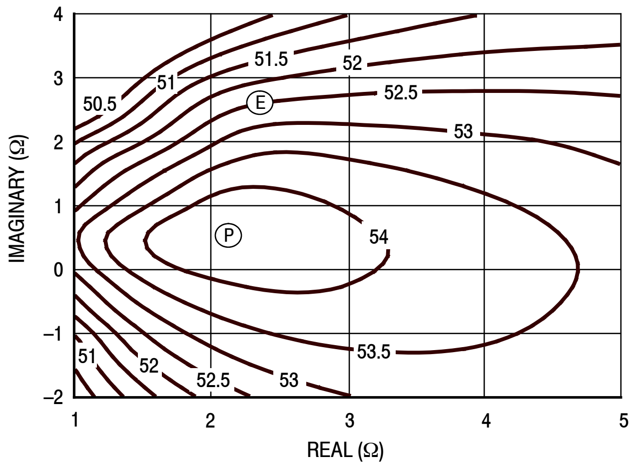


Figure 28. P1dB Load Pull Output Power Contours (dBm)

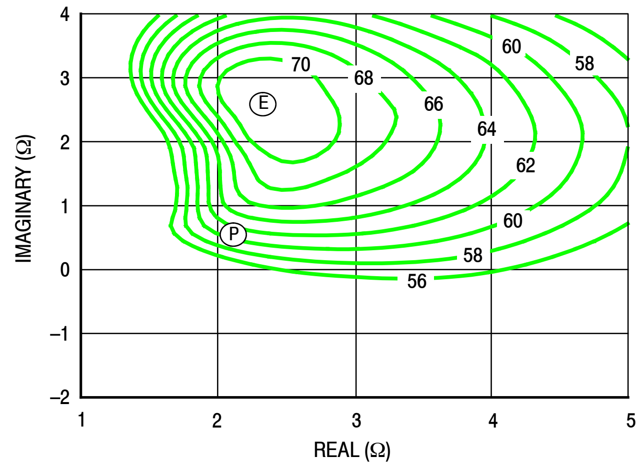


Figure 29. P1dB Load Pull Efficiency Contours (%)

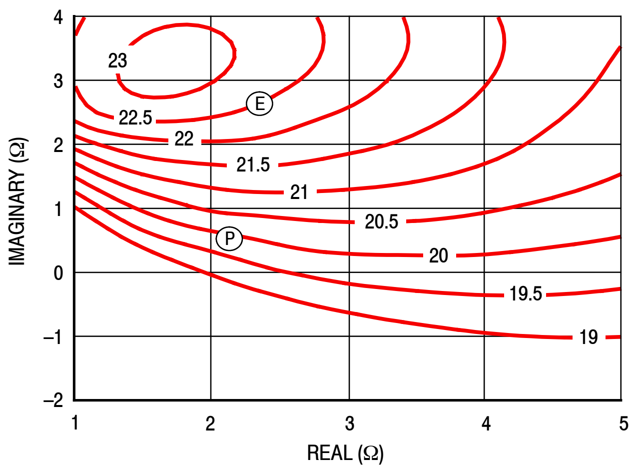


Figure 30. P1dB Load Pull Gain Contours (dB)

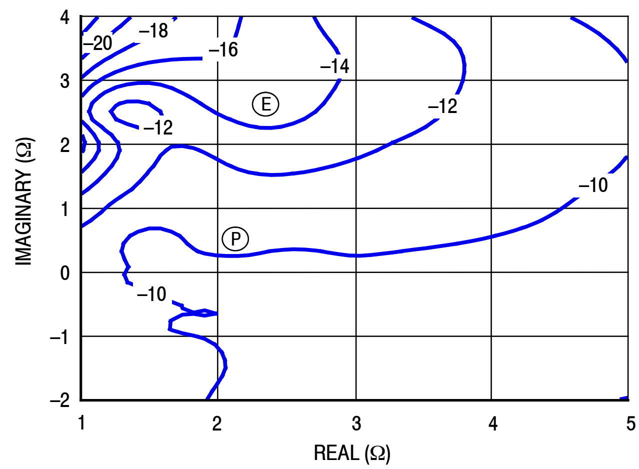


Figure 31. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 780 MHz

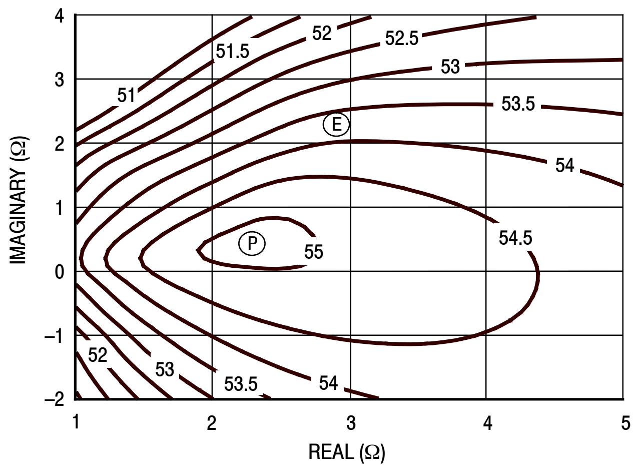


Figure 32. P3dB Load Pull Output Power Contours (dBm)

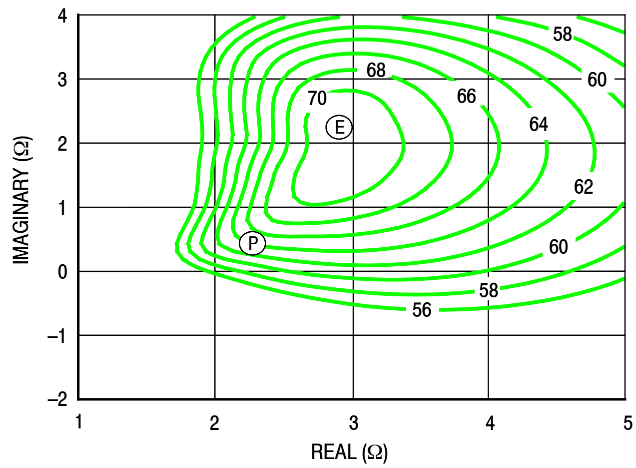


Figure 33. P3dB Load Pull Efficiency Contours (%)

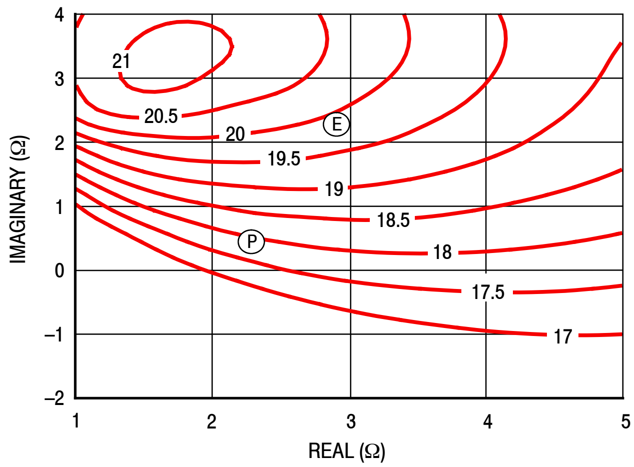


Figure 34. P3dB Load Pull Gain Contours (dB)

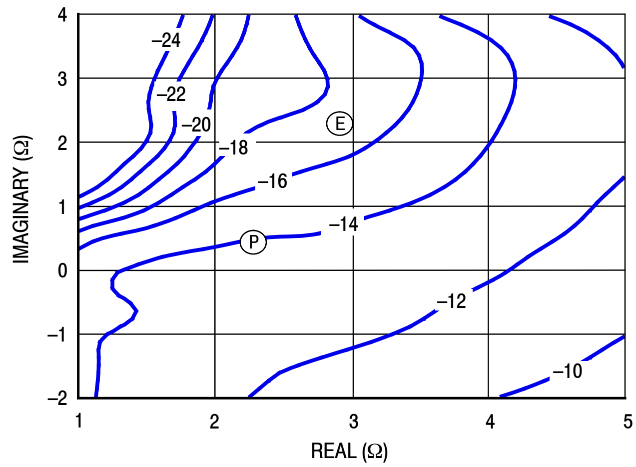


Figure 35. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 780 MHz

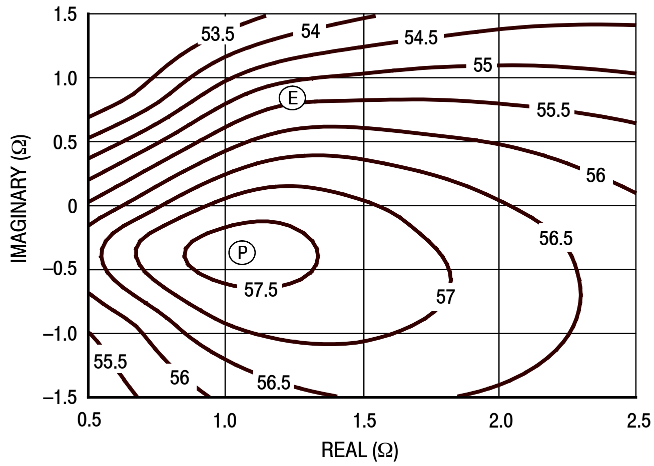


Figure 36. P1dB Load Pull Output Power Contours (dBm)

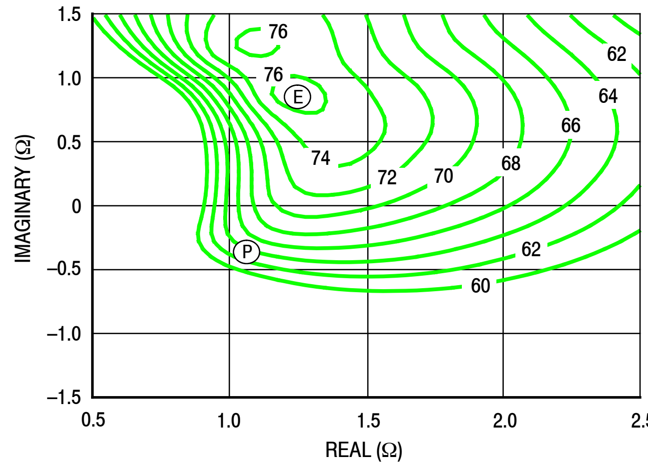


Figure 37. P1dB Load Pull Efficiency Contours (%)

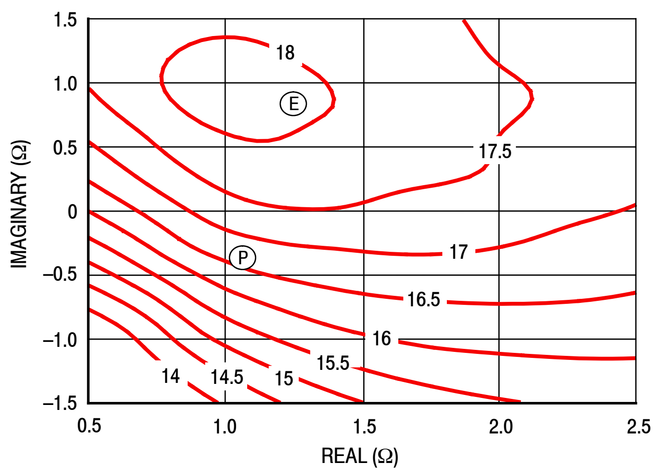


Figure 38. P1dB Load Pull Gain Contours (dB)

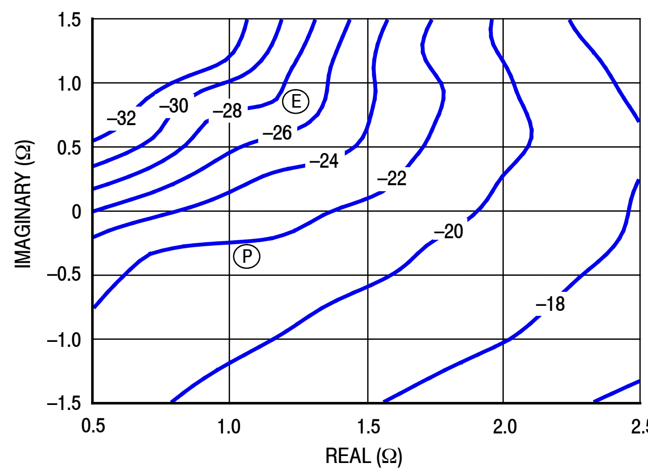


Figure 39. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power

(E) = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 780 MHz

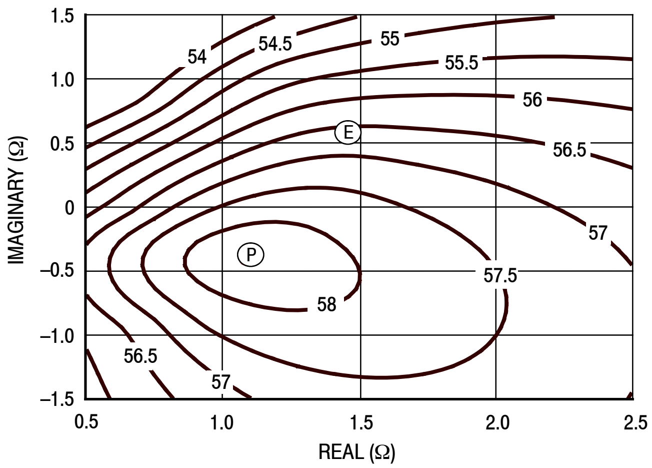


Figure 40. P3dB Load Pull Output Power Contours (dBm)

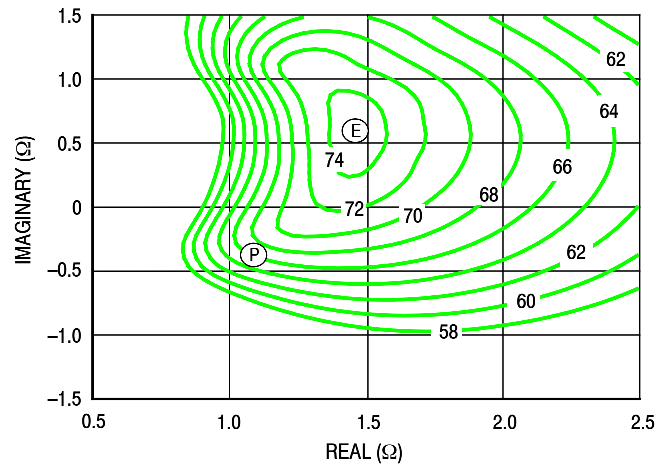


Figure 41. P3dB Load Pull Efficiency Contours (%)

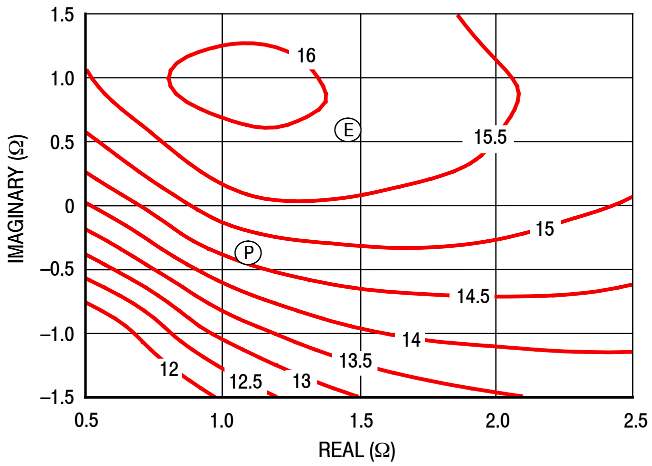


Figure 42. P3dB Load Pull Gain Contours (dB)

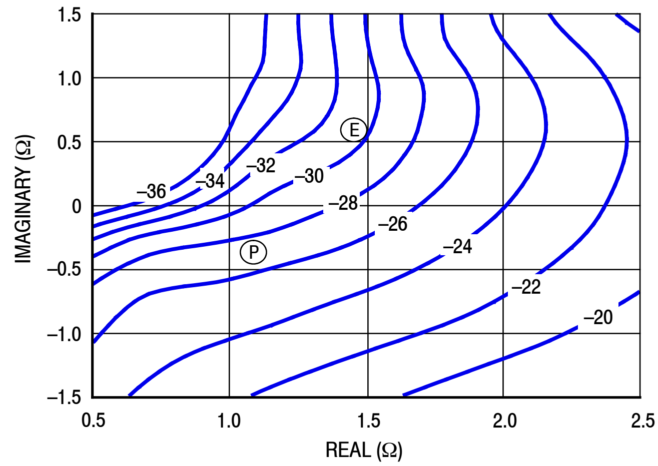
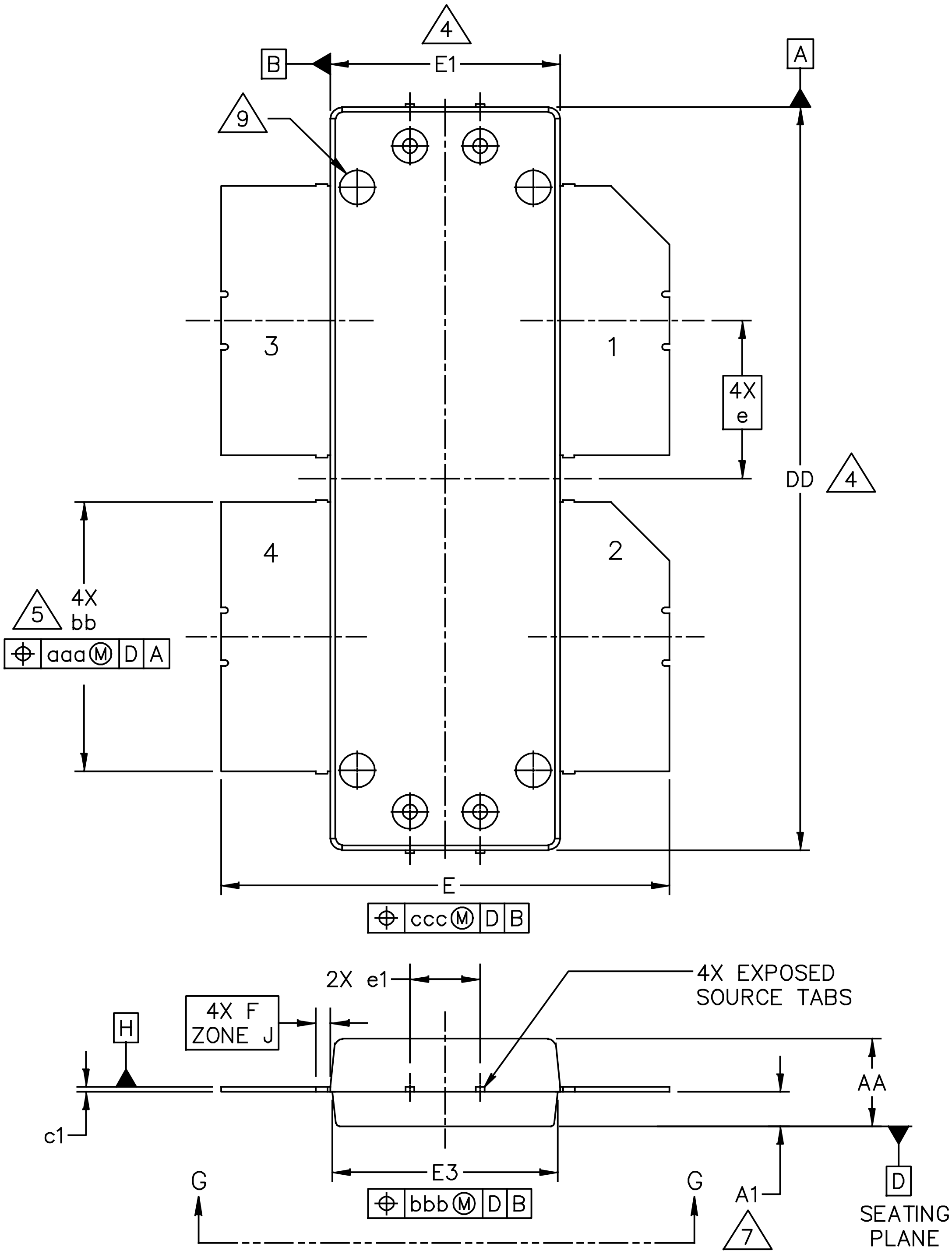


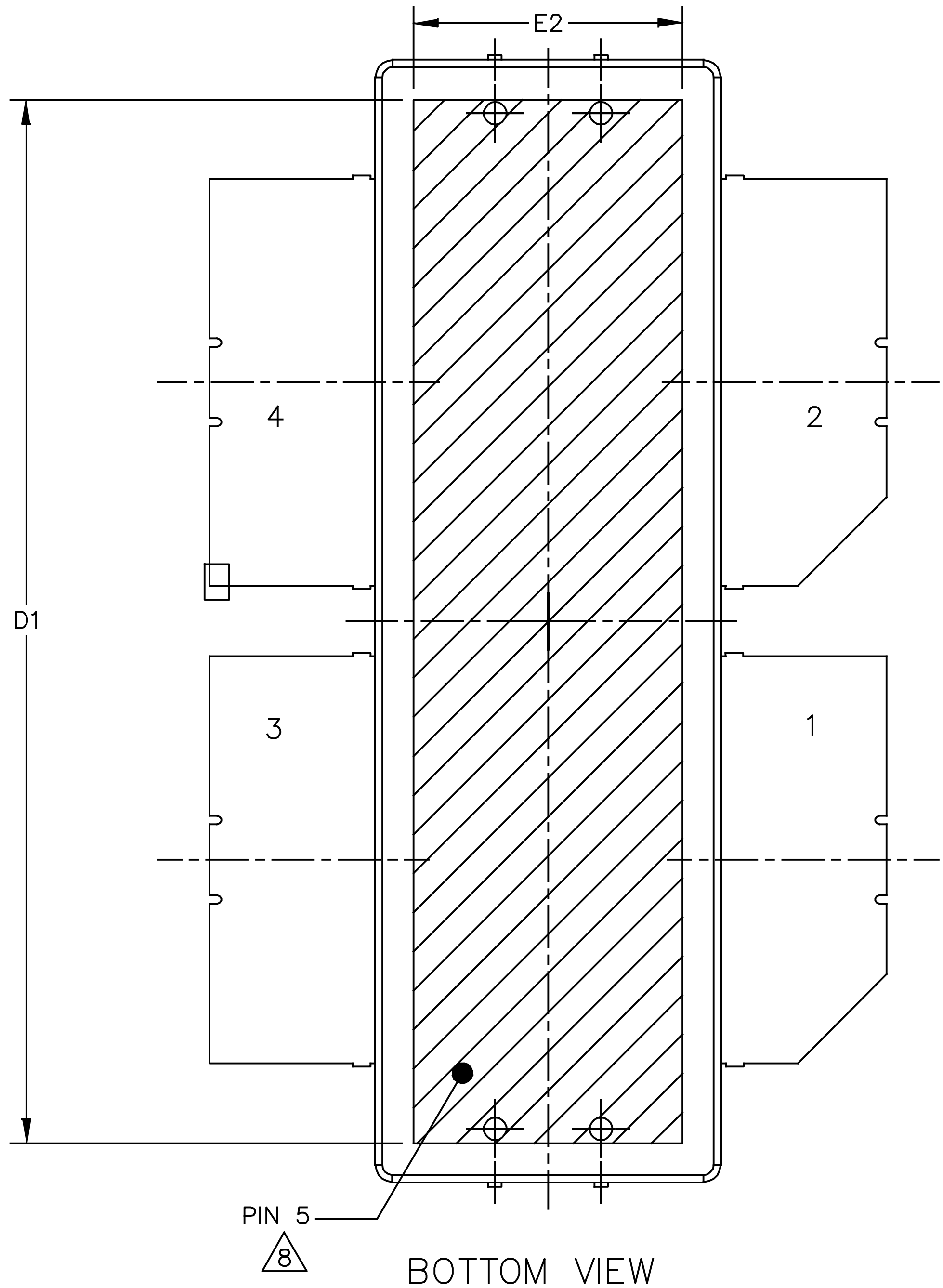
Figure 43. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power



© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM–1230–4L	DOCUMENT NO: 98ASA00506D	REV: C
	STANDARD: NON–JEDEC	
	SOT1816–1	08 FEB 2016



BOTTOM VIEW
VIEW G–G

© NXP SEMICONDUCTORS N.V. ALL RIGHTS RESERVED	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM–1230–4L	DOCUMENT NO: 98ASA00506D REV: C	
	STANDARD: NON–JEDEC	
	SOT1816–1	08 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

△4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

△5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

△7. DIMENSION A1 APPLIES WITHIN ZONE J ONLY.

△8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

△9. DIMPLED HOLE REPRESENTS INPUT SIDE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	bb	.457	.463	11.61	11.76
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
DD	1.267	1.273	32.18	32.33	e	.270 BSC		6.86 BSC	
D1	1.180	----	29.97	----	e1	.116	.124	2.95	3.15
E	.762	.770	19.35	19.56					
E1	.390	.394	9.91	10.01	aaa	.004		0.10	
E2	.306	----	7.77	----	bbb	.006		0.15	
E3	.383	.387	9.73	9.83	ccc	.010		0.25	
F	.025 BSC		0.635 BSC						

MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE

TITLE: OM—1230—4L

DOCUMENT NO: 98ASA00506D REV: C

STANDARD: NON—JEDEC

SOT1816—1 08 FEB 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2017	• Initial release of data sheet

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number: A2V09H525-04N
Rev. 0, 03/2017

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.