FEATURES

- **Member of the Texas Instruments Widebus+™ Family**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DESCRIPTION/ORDERING INFORMATION

This device contains eight independent noninverting buffers and a 16-bit noninverting bus transceiver and D-type latch designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74ALVCH32973 is particularly suitable for demultiplexing an address/data bus into a dedicated address bus and dedicated data bus. The device is used where there is asynchronous bidirectional communication between the A and B data bus, and the address signals are latched and buffered on the Q bus. The control-function implementation minimizes external timing requirements.

This device can be used as one 8-bit buffer, two 8-bit transceivers, and two 8-bit latches or one 8-bit buffer, one 16-bit transceiver, and one 16-bit latch. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The transceiver output-enable ($\overline{\text{TOE}}$) input can be used to disable the transceivers so that the A and B buses effectively are isolated.

When the latch-enable (LE) input is high, the Q outputs follow the data (A) inputs. When LE is taken low, the Q outputs are latched at the levels set up at the A inputs. The latch output-enable ($\overline{\text{LOE}}$) input can be used to place the nine Q outputs in either a normal logic state (high or low logic level) or the high-impedance state. In the high-impedance state, the Q outputs neither drive nor load the bus lines significantly. $\overline{\text{LOE}}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the Q outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{LOE}}$ and $\overline{\text{TOE}}$ should be tied to V_{CC} through pullup resistors; the minimum values of the resistors are determined by the current-sinking capability of the drivers.

The eight independent noninverting buffers perform the Boolean function Y = D and are independent of the state of DIR, $\overline{\text{TOE}}$, LE, and $\overline{\text{LOE}}$.

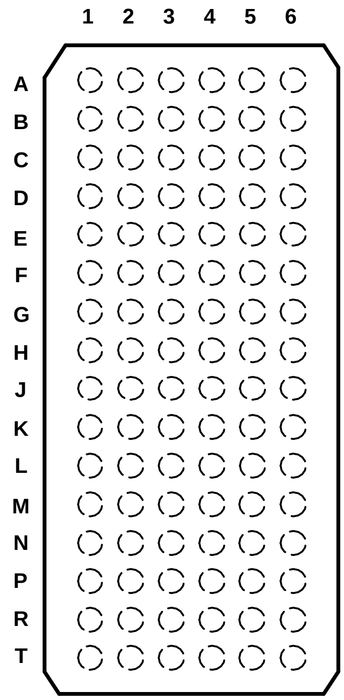
The A and B I/Os and D inputs have bus-hold circuitry. Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA - GKE	Tape and reel	SN74ALVCH32973KR	ACH973
	LFBGA - ZKE (Pb-free)		74ALVCH32973ZKER	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

GKE OR ZKE PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS

	1	2	3	4	5	6
A	1A1	D1	$1\overline{TOE}$	1DIR	1B1	1Q1
B	1A2	Y1	GND	GND	1B2	1Q2
C	1A3	D2	V_{CC}	V_{CC}	1B3	1Q3
D	1A4	Y2	GND	GND	1B4	1Q4
E	1A5	D3	GND	GND	1B5	1Q5
F	1A6	Y3	V_{CC}	V_{CC}	1B6	1Q6
G	1A7	D4	GND	GND	1B7	1Q7
H	1A8	Y4	1LE	$1\overline{LOE}$	1B8	1Q8
J	2A1	D5	$2\overline{TOE}$	2DIR	2B1	2Q1
K	2A2	Y5	GND	GND	2B2	2Q2
L	2A3	D6	V_{CC}	V_{CC}	2B3	2Q3
M	2A4	Y6	GND	GND	2B4	2Q4
N	2A5	D7	GND	GND	2B5	2Q5
P	2A6	Y7	V_{CC}	V_{CC}	2B6	2Q6
R	2A7	D8	GND	GND	2B7	2Q7
T	2A8	Y8	2LE	$2\overline{LOE}$	2B8	2Q8

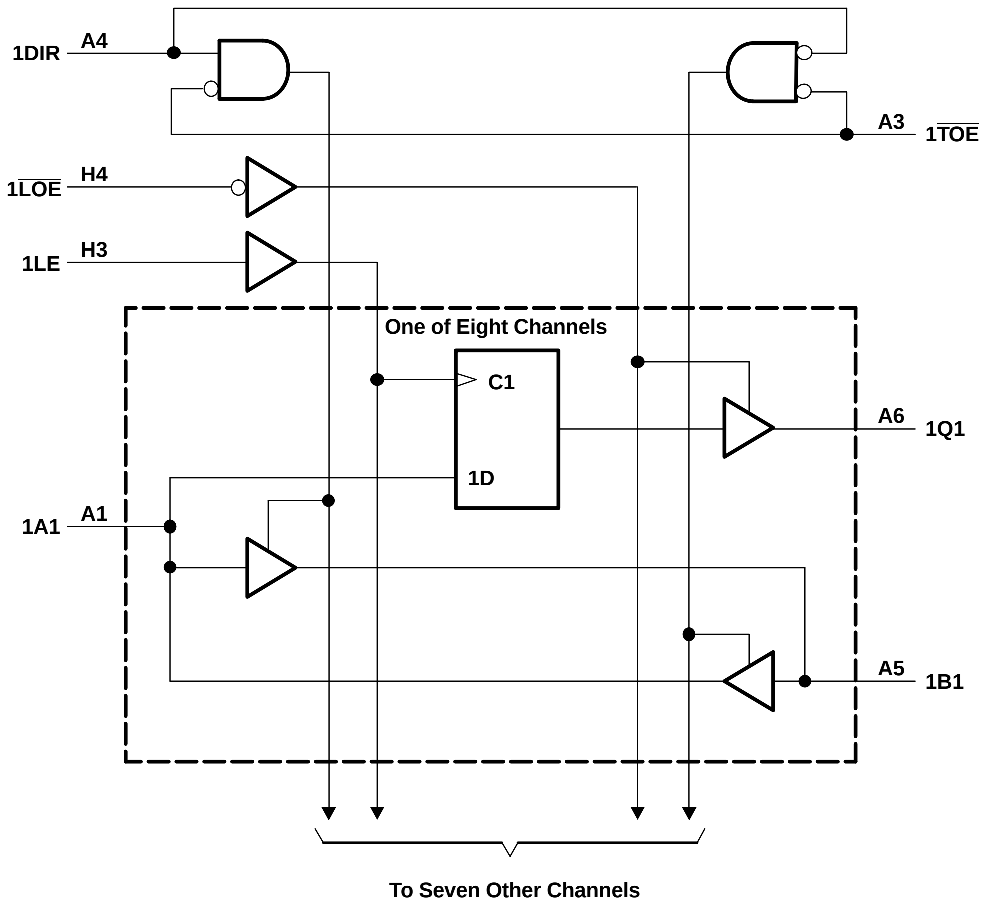
FUNCTION TABLES

INPUTS		OPERATION
$\overline{TOE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus and B bus isolation

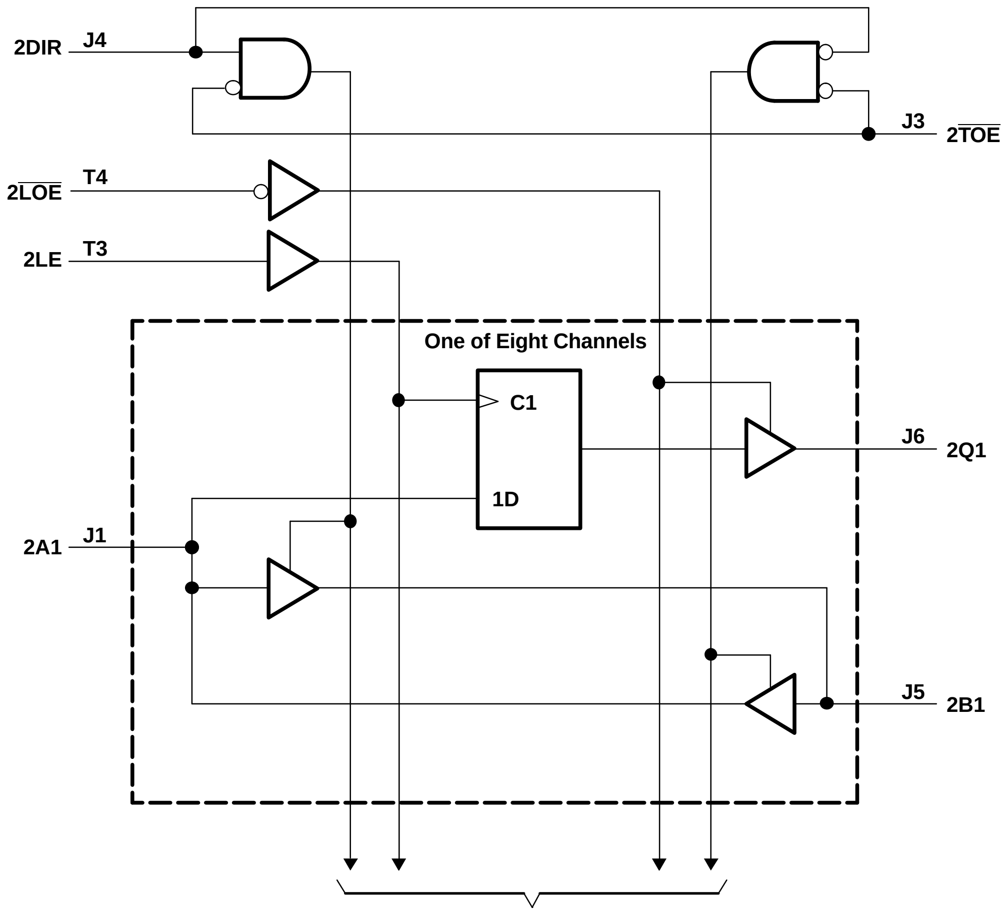
INPUTS			OUTPUT Q
$\overline{LOE}$	LE	A	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

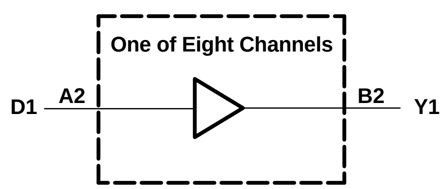
INPUT D	OUTPUT Y
L	L
H	H

LOGIC DIAGRAM (POSITIVE LOGIC)



LOGIC DIAGRAM (POSITIVE LOGIC)





ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range	Except I/O and D input ports[2]	-0.5	4.6	V
		I/O and D input ports[2][3]	-0.5	V_{CC} + 0.5	
V_O	Output voltage range[2][3]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance[4]	GKE/ZKE package		40	°C/W
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		-4	mA
		V_{CC} = 2.3 V		-12	
		V_{CC} = 2.7 V		-12	
		V_{CC} = 3 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		12	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	85	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

TEXAS INSTRUMENTS
www.ti.com

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{OH}		I_{OH} = -100 µA	1.65 V to 3.6 V	V_{CC} - 0.2			V
		I_{OH} = -4 mA	1.65 V	1.2			
		I_{OH} = -6 mA	2.3 V	2			
		I_{OH} = -12 mA	2.3 V	1.7			
			2.7 V	2.2			
			3 V	2.4			
		I_{OH} = -24 mA	3 V	2			
V_{OL}		I_{OL} = 100 µA	1.65 V to 3.6 V			0.2	V
		I_{OL} = 4 mA	1.65 V			0.45	
		I_{OL} = 6 mA	2.3 V			0.4	
		I_{OL} = 12 mA	2.3 V			0.7	
			2.7 V			0.4	
		I_{OL} = 24 mA	3 V			0.55	
I_I		$V_I = V_{CC}$ or GND	3.6 V			±5	µA
I_{BHL}(2)		V_I = 0.57 V	1.65 V	25			µA
		V_I = 0.7 V	2.3 V	45			
		V_I = 0.8 V	3 V	75			
I_{BHH}(3)		V_I = 1.07 V	1.65 V	-25			µA
		V_I = 1.7 V	2.3 V	-45			
		V_I = 2 V	3 V	-75			
I_{BHLO}(4)		V_I = 0 to V_{CC}	1.95 V	200			µA
			2.7 V	300			
			3.6 V	500			
I_{BHHO}(5)		V_I = 0 to V_{CC}	1.95 V	-200			µA
			2.7 V	-300			
			3.6 V	-500			
I_{OZ}(6)		$V_O = V_{CC}$ or GND	3.6 V			±10	µA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	3.6 V			60	µA
ΔI_{CC}		One input at V_{CC} - 0.6 V, Other inputs at V_{CC} or GND	3 V to 3.6 V			750	µA
C_i	Control inputs	$V_I = V_{CC}$ or GND	3.3 V		3		pF
	D				4		
C_{io}	A ports	$V_O = V_{CC}$ or GND	3.3 V		4.5		pF
	B ports				4.5		
C_o	Q	$V_O = V_{CC}$ or GND	3.3 V		3		pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(3) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(4) An external driver must source at least I_{BHLO} to switch this node from low to high.
(5) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(6) For I/O ports, the parameter I_{OZ} includes the input leakage current.

TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V_{CC} = 1.8 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	2		2		2		ns
t_{su}	Setup time, data before LE↓	0.9		0.9		0.9		ns
t_h	Hold time, data after LE↓	0.9		0.9		0.9		ns

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	
t_{pd}	D	Y	2.2	0.5	3.2	0.5	3	ns
	A	Q	2.2	0.5	3.2	0.5	3	
	LE		2.8	0.5	3.3	0.5	3	
	A or B	B or A	2.2	0.5	3.2	0.5	3	
t_{en}	$\overline{\text{LOE}}$	Q	2.9	0.7	4.9	0.7	4.7	ns
	$\overline{\text{TOE}}$	A or B	3	0.7	4.6	0.7	4.4	
	DIR		3.4	0.7	4.9	0.7	4.7	
t_{dis}	$\overline{\text{LOE}}$	Q	2.8	0.5	4.3	0.5	4.1	ns
	$\overline{\text{TOE}}$	A or B	3.2	0.5	4.3	0.5	4.1	
	DIR		3.4	0.5	4.9	0.5	4.7	

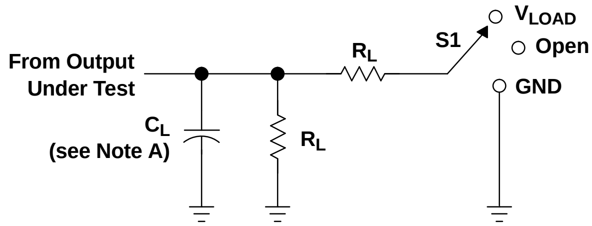
OPERATING CHARACTERISTICS(1)

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	UNIT
				TYP	TYP	TYP	
C_{pd} (2) (each output)	Power dissipation capacitance	A outputs enabled, Q outputs disabled, one A output switching	One f_A = 10 MHz, One f_B = 10 MHz, $\overline{TOE}$ = GND, $\overline{LOE}$ = V_{CC}, DIR = GND, C_L = 0 pF	12	14	19	pF
		B outputs enabled, Q outputs disabled, one B output switching	One f_A = 10 MHz, One f_B = 10 MHz, $\overline{TOE}$ = GND, $\overline{LOE}$ = V_{CC}, DIR = GND, C_L = 0 pF	12	14	21	
		Q outputs enabled, A and B I/Os isolated, one Q output switching	One f_A = 10 MHz, One f_{LE} = 20 MHz, One f_Q = 10 MHz, $\overline{TOE}$ = V_{CC}, $\overline{LOE}$ = GND, C_L = 0 pF	11	13	19	
		One Y output switching, A and B I/Os isolated, Q outputs disabled	One f_D = 10 MHz, One f_Y = 10 MHz, $\overline{TOE}$ = V_{CC}, $\overline{LOE}$ = V_{CC}, C_L = 0 pF	7	8	12	
C_{pd} (Z)	Power dissipation capacitance	A and B I/Os isolated, Q outputs disabled, one LE and one A data input switching	One f_A = 10 MHz, One f_{LE} = 20 MHz, f_Q not switching, $\overline{TOE}$ = V_{CC}, $\overline{LOE}$ = V_{CC}, C_L = 0 pF	4	5	11	pF
C_{pd} (3) (each LE)	Power dissipation capacitance	A and B I/Os isolated, Q outputs disabled, one LE input switching	f_A not switching, One f_{LE} = 20 MHz, f_Q not switching, $\overline{TOE}$ = V_{CC}, $\overline{LOE}$ = V_{CC}, C_L = 0 pF	6	7	9	pF

(1) Total device C_{pd} for multiple (m) outputs switching and (n) LE inputs switching = [m * C_{pd} (each output)] + [n * C_{pd} (each LE)]
(2) C_{pd} (each output) is the C_{pd} for each data bit (input and output circuitry) when it operates at 10 MHz (Note: The LE is operating at 20 MHz in this test, but its I_{CC} component has been subtracted).
(3) C_{pd} (each LE) is the C_{pd} for the clock circuitry only when it operates at 20 MHz.

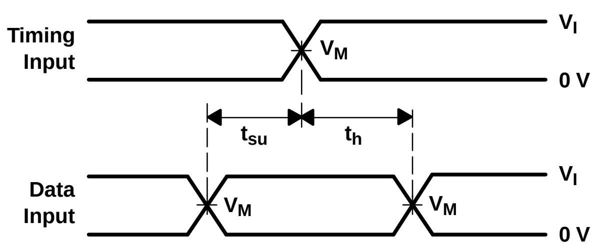
PARAMETER MEASUREMENT INFORMATION



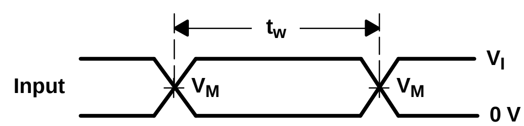
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

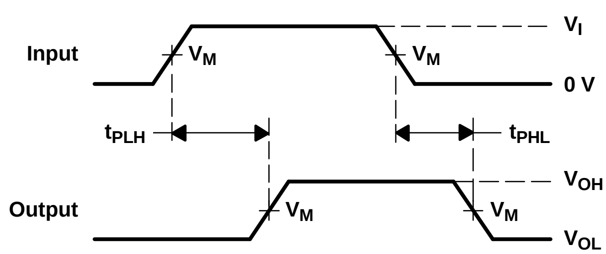
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



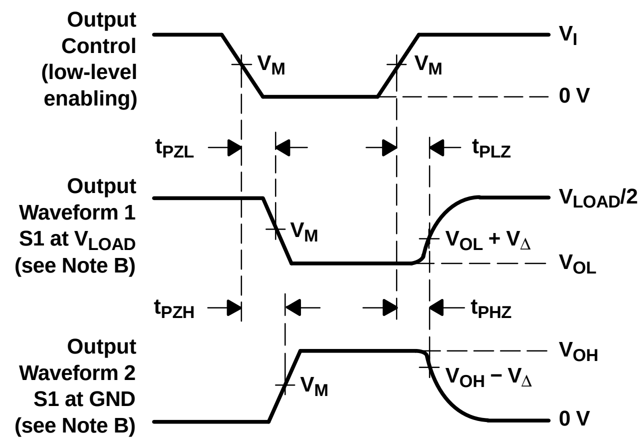
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
74ALVCH32973ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-250C-168 HR
SN74ALVCH32973KR	ACTIVE	LFBGA	GKE	96	1000	TBD	SNPB	Level-3-220C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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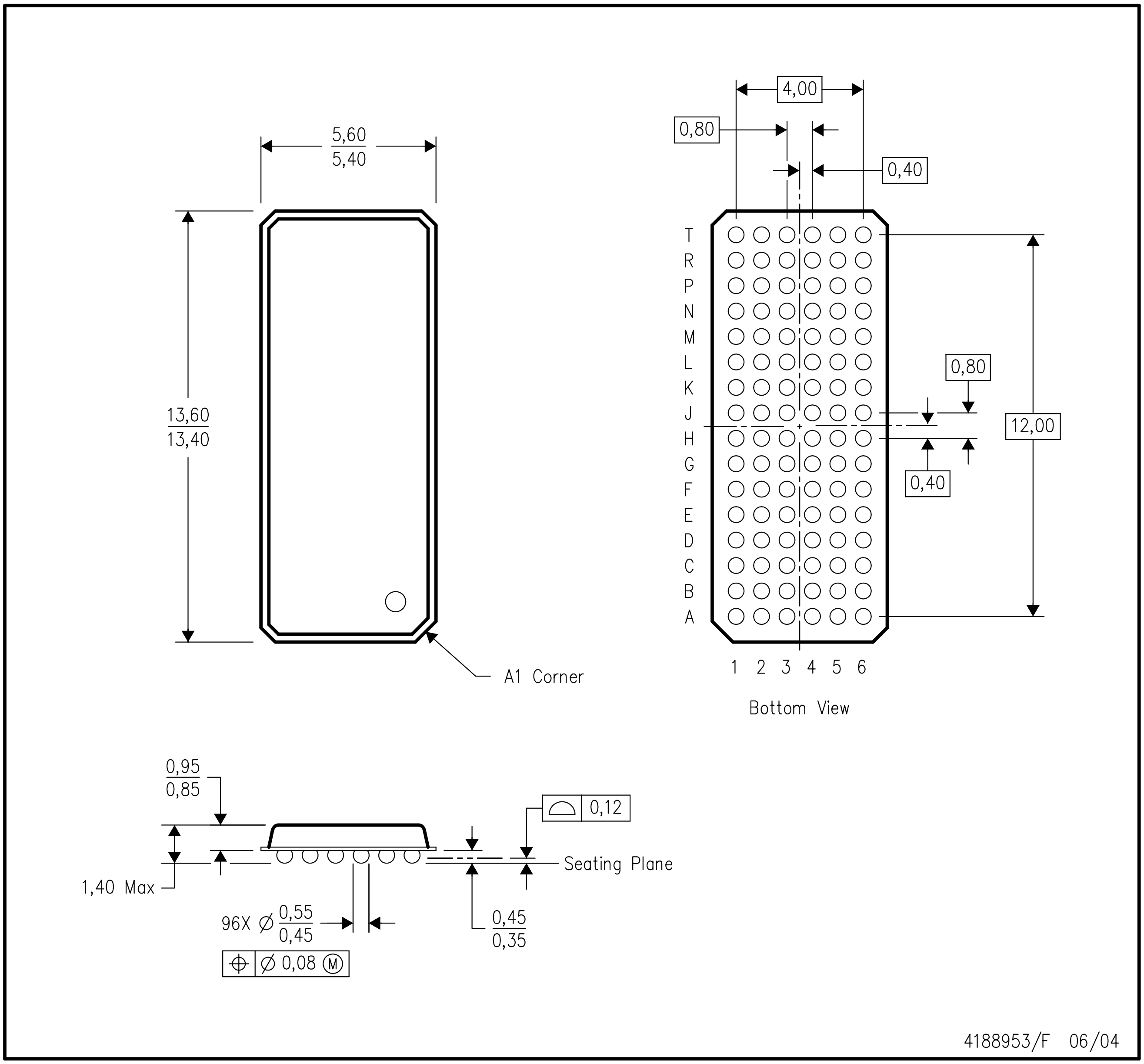
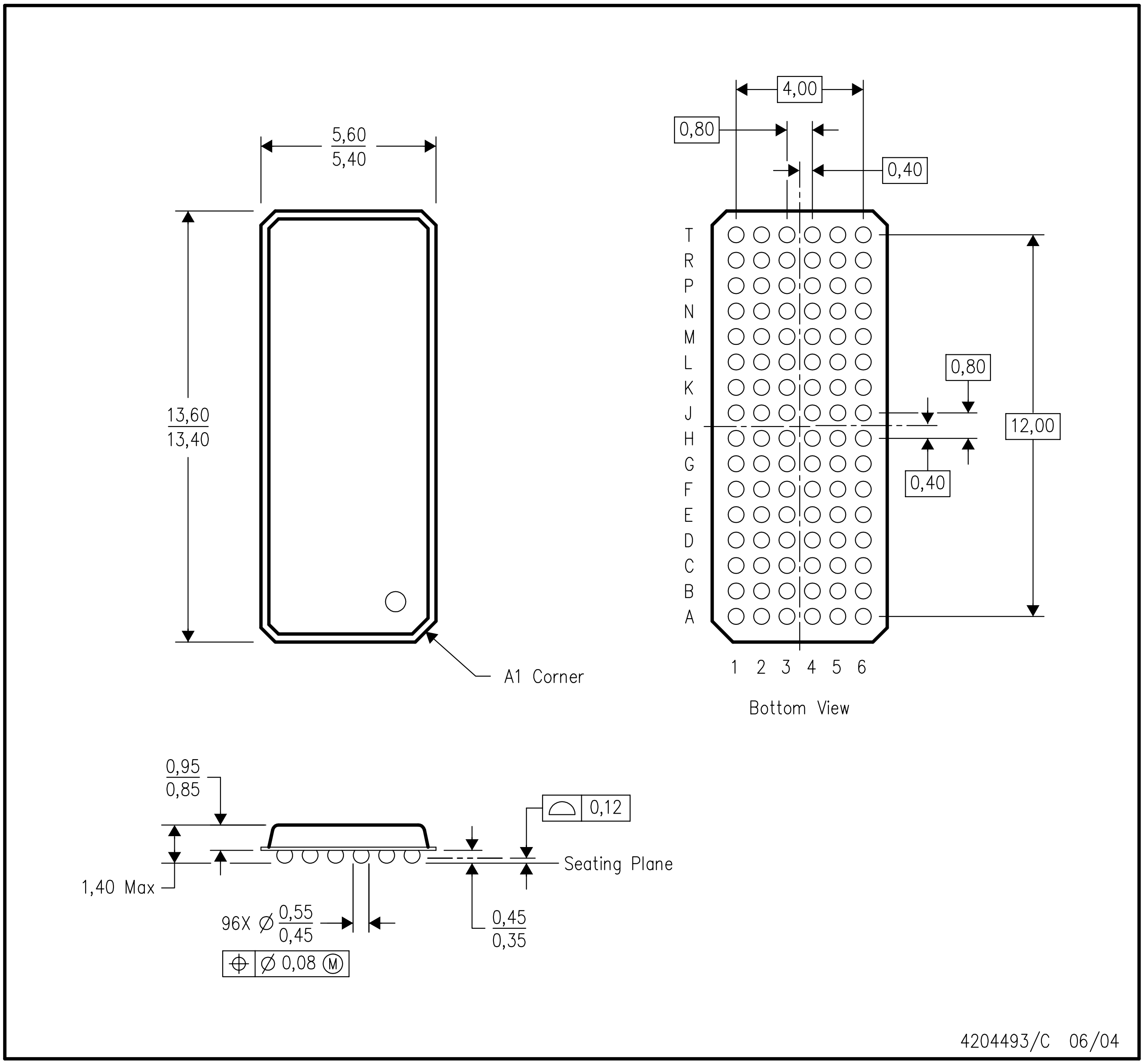
GKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–205 variation CC.
D. This package is tin–lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead–free.

ZKE (R–PBGA–N96) PLASTIC BALL GRID ARRAY



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO–205 variation CC.
- D. This package is lead–free. Refer to the 96 GKE package (drawing 4188953) for tin–lead (SnPb).

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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Как с нами связаться

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