

FFSPF1065A

Silicon Carbide Schottky Diode

650 V, 10 A

Description

Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

Features

- Max Junction Temperature 175°C
- Avalanche Rated 64 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery / No Forward Recovery
- This Device is Pb-Free and is RoHS Compliant

Applications

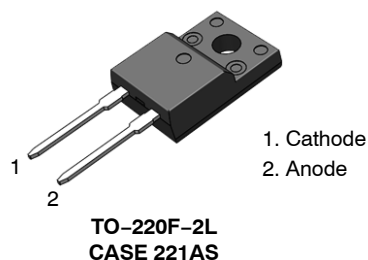
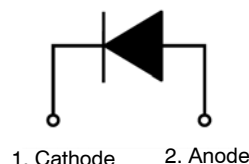
- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits



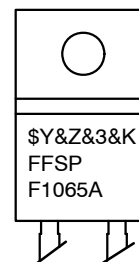
ON Semiconductor®

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V_{RRM}	I_F
650 V	10 A



MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FFSPF1065A	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FFSPF1065A

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	FFSPF1065A	Unit
V _{RRM}	Peak Repetitive Reverse Voltage	650	V
E _{AS}	Single Pulse Avalanche Energy (Note 1)	64	mJ
I _F	Continuous Rectified Forward Current	@T _C < 110°C	10
		@ T _C < 135°C	7.2
I _{F, Max}	Non-Repetitive Peak Forward Surge Current	T _C = 25°C, 10 μs	720
		T _C = 150°C, 10 μs	680
I _{F, SM}	Non-Repetitive Forward Surge Current	Half-Sine Pulse, t _p = 8.3 ms	56
I _{F, RM}	Repetitive Forward Surge Current	Half-Sine Pulse, t _p = 8.3 ms	28
P _{tot}	Power Dissipation	T _C = 25°C	38
		T _C = 150°C	6.4
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. E_{AS} of 64 mJ is based on starting T_J = 25°C, L = 0.5 mH, I_{AS} = 16 A, V = 50 V.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	3.9	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FFSPF1065A	FFSPF1065A	TO-220F-2L	Tube	N/A	N/A	50 Units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _F	Forward Voltage	I _F = 10 A, T _C = 25°C	–	1.50	1.75	V
		I _F = 10 A, T _C = 125°C	–	1.60	2.0	
		I _F = 10 A, T _C = 175°C	–	1.72	2.4	
I _R	Reverse Current	V _R = 650 V, T _C = 25°C	–	–	200	μA
		V _R = 650 V, T _C = 125°C	–	–	400	
		V _R = 650 V, T _C = 175°C	–	–	600	
Q _C	Total Capacitance Charge	V = 400 V	–	34	–	nC
C	Total Capacitance	V _R = 1 V, f = 100 kHz	–	575	–	pF
		V _R = 200 V, f = 100 kHz	–	62	–	
		V _R = 400 V, f = 100 kHz	–	47	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

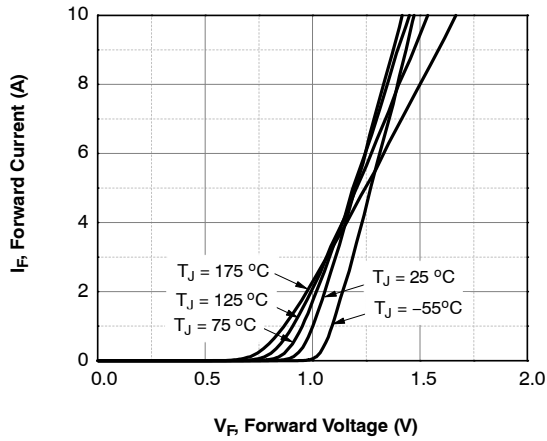


Figure 1. Forward Characteristics

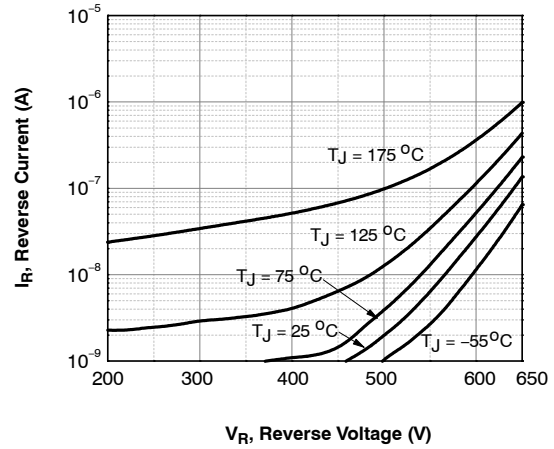


Figure 2. Reverse Characteristics

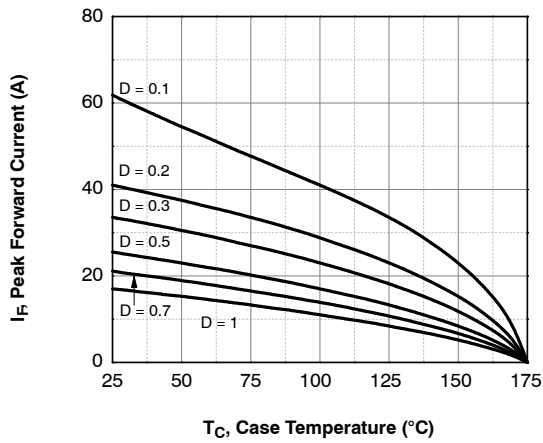


Figure 3. Current Derating

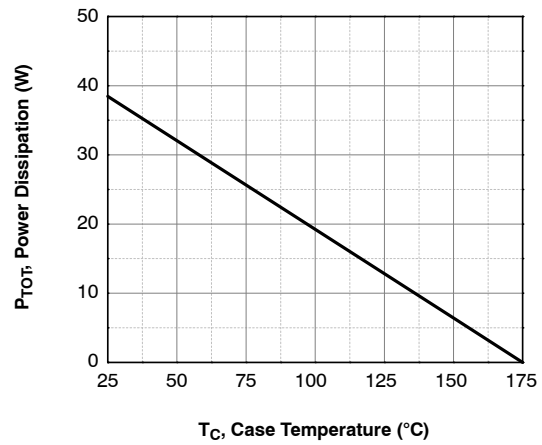


Figure 4. Power Derating

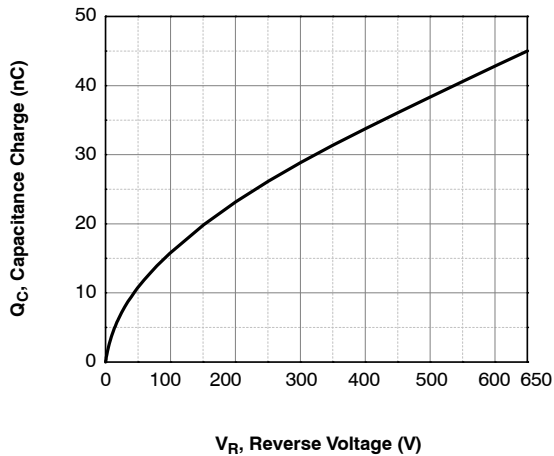


Figure 5. Capacitive Charge vs. Reverse Voltage

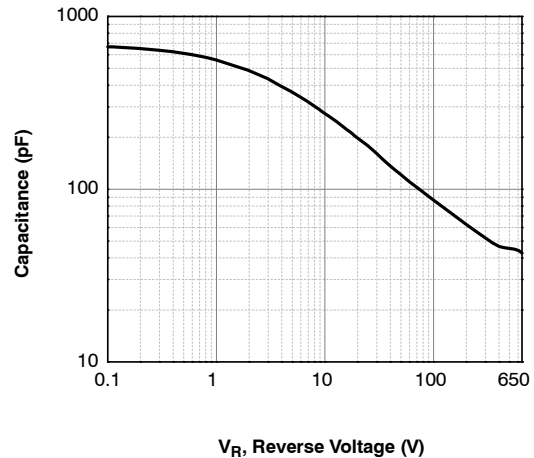


Figure 6. Capacitance vs. Reverse Voltage

TYPICAL CHARACTERISTICS (Continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

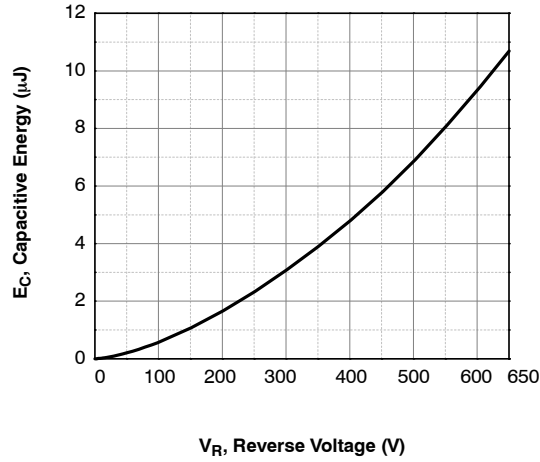


Figure 7. Capacitance Stored Energy

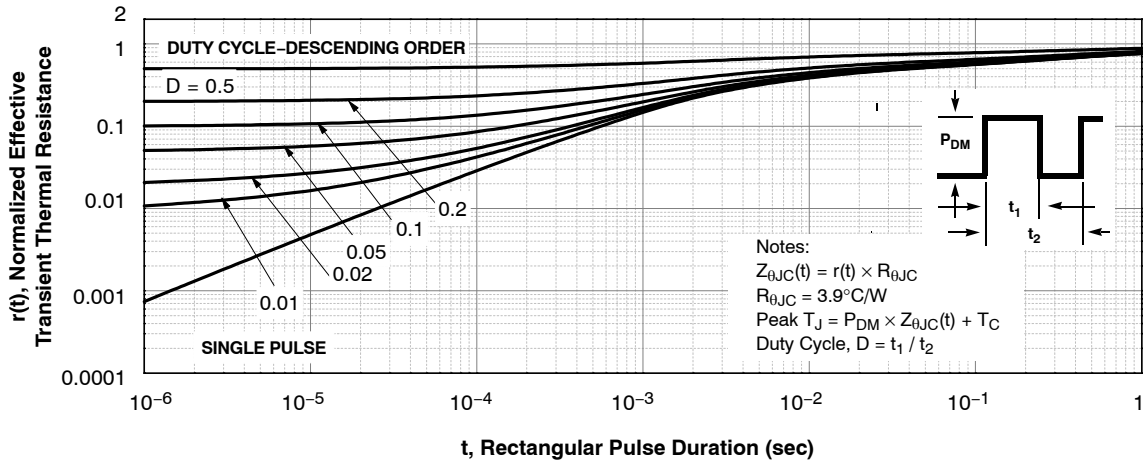


Figure 8. Junction-to-Case Transient Thermal Response Curve

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TEST CIRCUIT AND WAVEFORMS

$L = 0.5 \text{ mH}$
 $R < 0.1 \Omega$
 $V_{DD} = 50 \text{ V}$
 $E_{AVL} = 1/2 L I_L^2 [V_{R(AVL)} / (V_{R(AVL)} - V_{DD})]$
 $Q1 = \text{IGBT } (BV_{CES} > DUT \ V_{R(AVL)})$

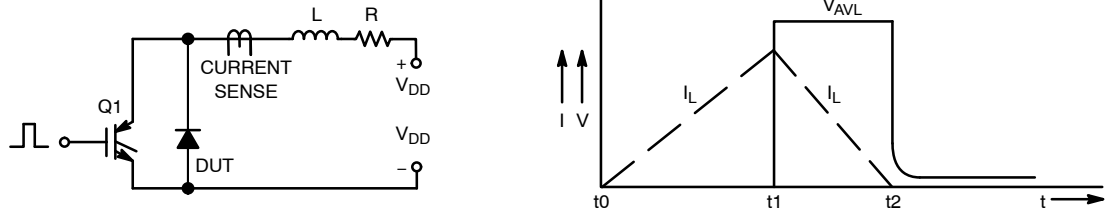


Figure 9. Unclamped Inductive Switching Test Circuit & Waveform

PACKAGE DIMENSIONS

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