

TOSHIBA Diode Silicon Epitaxial Planar Type

# 1SS181

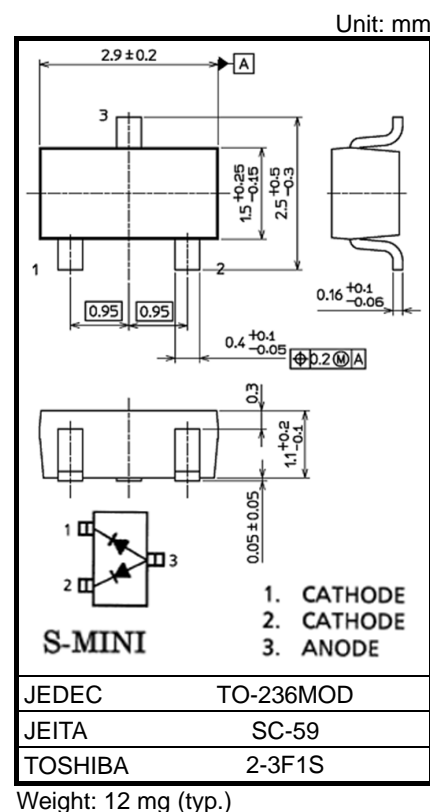
## Ultra High Speed Switching Application

- AEC-Q101 Qualified (Note1)
- Small package : SC-59
- Low forward voltage :  $V_F(3) = 0.92V$  (Typ.)
- Fast reverse recovery time:  $t_{rr} = 1.6ns$  (Typ.)
- Small total capacitance :  $C_T = 2.2pF$  (Typ.)

Note1: For detail information, please contact to our sales.

## Absolute Maximum Ratings ( $T_a = 25^\circ C$ )

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	85	V
Reverse voltage	$V_R$	80	V
Maximum (peak) forward current	$I_{FM}$	300 (*)	mA
Average forward current	$I_O$	100 (*)	mA
Surge current (10ms)	$I_{FSM}$	2 (*)	A
Power dissipation	P	150	mW
Junction temperature	$T_j$	125	$^\circ C$
Storage temperature	$T_{stg}$	-55 to 125	$^\circ C$



Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

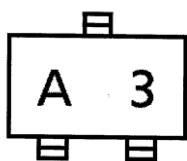
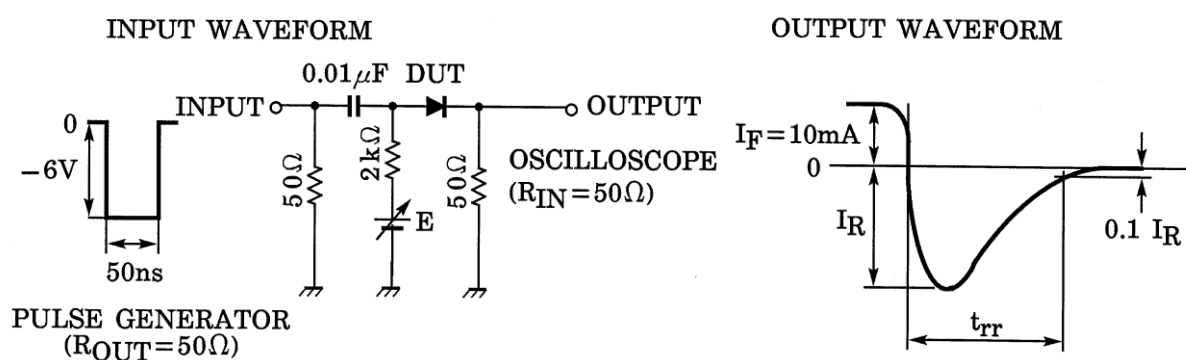
\*: Unit rating. Total rating = Unit rating  $\times$  1.5.

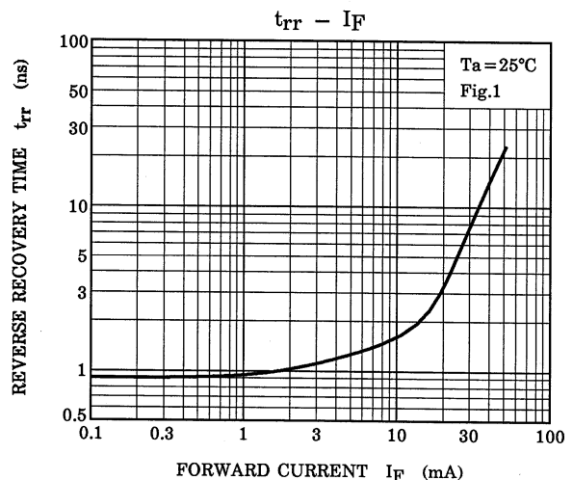
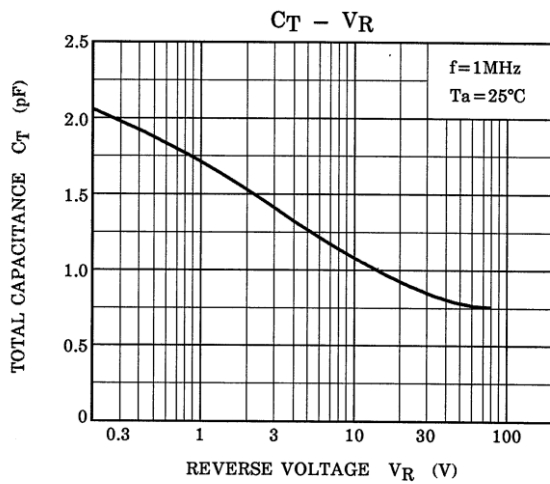
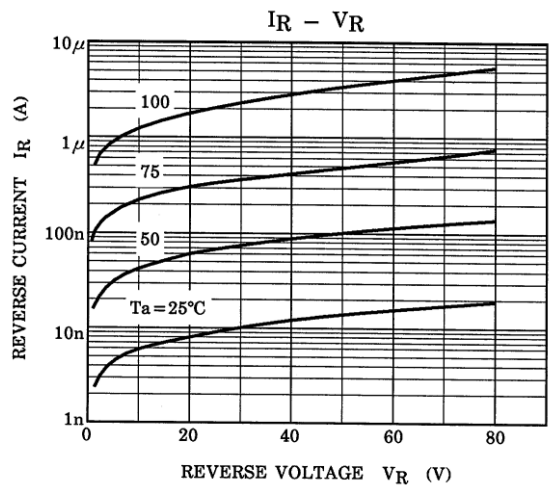
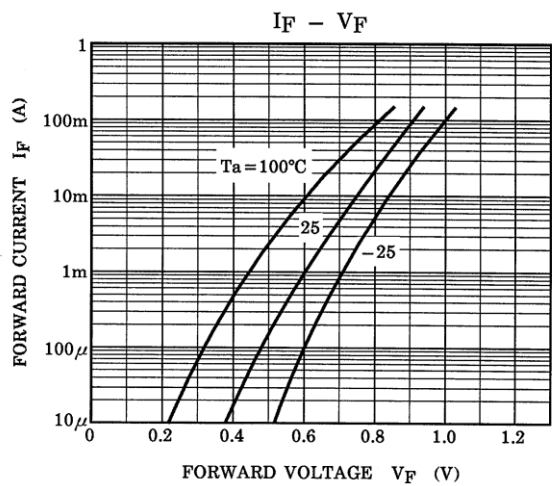
## Electrical Characteristics

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit
Forward voltage	$V_F(1)$	$I_F = 1mA$	—	0.61	—	V
	$V_F(2)$	$I_F = 10mA$	—	0.74	—	
	$V_F(3)$	$I_F = 100mA$	—	0.92	1.20	
Reverse current	$I_R(1)$	$V_R = 30V$	—	—	0.1	$\mu A$
	$I_R(2)$	$V_R = 80V$	—	—	0.5	
Total capacitance	$C_T$	$V_R = 0V, f = 1MHz$	—	2.2	4.0	pF
Reverse recovery time	$t_{rr}$	$I_F = 10mA$ (Fig.1)	—	1.6	4.0	ns

Start of commercial production  
1982-06

## Marking

Fig.1 Reverse recovery time ( $t_{rr}$ ) test circuit



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