FEATURES

- TI AM335x Application Processor
  - **Up to 1GHz ARM Cortex A8 MPU**
  - NEON SIMD Coprocessor
  - 32 KB L1 Program Cache
  - 32 KB L1 Data Cache
  - 256 KB L2 Cache
  - 64 KB RAM
  - 176 KB boot ROM
  - JTAG Emulation/Debug

- AM335x Processor Choices
  - AM3359 (PRU's, 3D and EtherCat)
  - AM3358 (PRU's and 3D)
  - AM3357 (PRU's and EtherCat)
  - AM3356 (PRU's)
  - AM3354 (3D)
  - AM3352

- **Up To 1 GB DDR3 or 256 MB DDR2 CPU RAM**

- Up to 1 GB Parallel NAND FLASH

- 8 MB Serial NOR FLASH

- 2 Programmable Real-time Units (PRUs) – Processor Dependent
- Integrated Power Management
- SGX530 3D Graphics Accelerator – Processor Dependent
- Watchdog Timer
- Real-time clock
- Power Reset and Clock Management (PRCM)
- Crypto Hardware Accelerators (AES, SHA, PKA, RNG)

STANDARD DDR3 SO-DIMM-204 INTERFACE

- 2 10/100/1000 Mbps EMACs
- 24-bit WXGA LCD Interface
- Touch Screen Controller
- 8 Channel, 12-bit SAR ADC
- 2 CAN Interfaces
- 6 UARTs
- 2 USB Ports
- 2 4-Channel McASPs
- 3 MMC/SD/SDIO
- 2 SPI, 2 I2C, GPIO
- eHRPWM, eQEP
- Single 3.3V to 5.0V Input Power Supply

APPLICATIONS

- Embedded Instrumentation
- Industrial Automation
- Industrial Instrumentation
- Medical Instrumentation
- Weighing Scales
- Closed Loop Motor Control

BENEFITS

- Rapid Development / Deployment
- Multiple Connectivity and Interface Options
- Rich User Interfaces
- High System Integration
- High Level OS Support
  - Linux Kernel
  - QNX
  - Windows CE Ready

DESCRIPTION

The MitySOM-335x series of highly configurable, small form-factor processor cards features one of Texas Instruments Sitara AM335x Processors. The module includes NAND FLASH and DDR2 or DDR3 RAM memory subsystems. A MitySOM-335x provides a complete and flexible CPU infrastructure for highly integrated embedded systems.

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The onboard AM335x processor provides Cortex-A8 32-bit RISC processor with a NEON SIMD coprocessor. This MPU is capable of running a rich set of real-time operating systems containing software applications programming interfaces (APIs) expected by modern system designers. The ARM architecture supports several operating systems, including Linux, QNX, and Windows CE.

In addition to the Cortex-A8, the AM335x family also offers available dual Programmable Real-Time Units (PRUs) when using the AM3356, AM3357, AM3358 or AM3359 processors. These PRUs are 200MHz RISC processors that run independently of the main Cortex-A8 CPU and have access to all the on-chip peripherals as well as all external memory. These can be used for any purpose; typical applications include the implementation of custom, industrial serial or Ethernet protocols such as PROFIBUS or EtherCAT. In addition, the PRUs can continue to run while the core CPU is in sleep mode in order to monitor for system wakeup events.

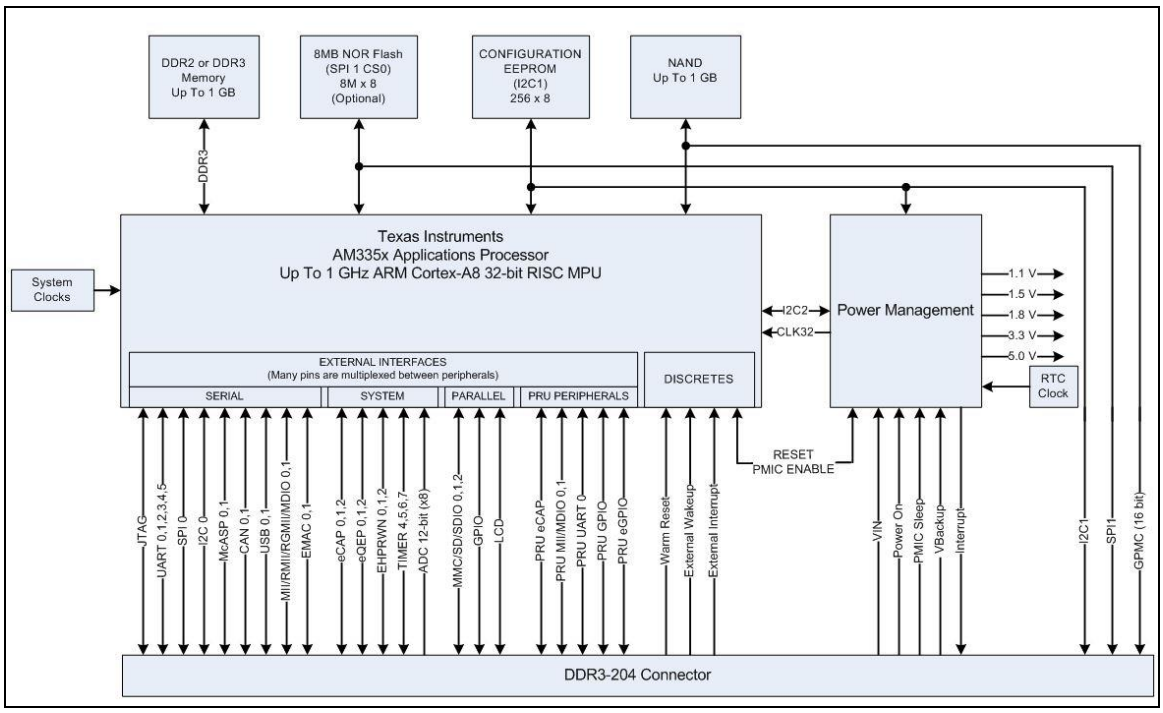

Figure 1 MitySOM-335x Block Diagram

Figure 1 provides a top level block diagram of the MitySOM-335x processor card. As shown in the figure, the primary interface to the MitySOM-335x is through a standard DDR3 SO-DIMM-204 card edge interface. The interface provides power, synchronous serial connectivity, and many other interfaces provided by the Sitara processor. Details of the SO-DIMM-204 connector interface are included in the SO-DIMM-204 Interface Description, below.

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MitySOM-335x Onboard DDR Memory Options

DDR2 Memory Option

The AM335x processor includes one dedicated 16 bit DDR SDRAM memory interface. The MitySOM-335x can include up to 256 MB of DDR2 RAM integrated on board the module. The memory bus interface is capable of burst transfer rates of 800 MB / second.

DDR3 Memory Option

The AM335x processor includes one dedicated 16 bit DDR SDRAM memory interface. The MitySOM-335x includes up to 1 GB of DDR3 RAM integrated on board the module. The memory bus interface is capable of burst transfer rates of 1200 MB / second.

MitySOM-335x Onboard Storage Memory

NAND FLASH (Optional)

Up to 1GB of on-board NAND FLASH memory is connected to the AM335x processor using the general purpose memory controller (GPMC) bus. The FLASH memory is 8 bits wide and is connected to the first chip select line of the GPMC (CE0). The FLASH memory is typically used to store the following types of data:

- Bootloaders
- ARM Linux / Windows CE / QNX embedded root file-system
- runtime ARM software
- runtime application data (non-volatile storage)

The GPMC bus is also accessible on the SO-DIMM-204 connector. It can be used to access external memories such as SDRAM, SRAM, NOR flash, NAND flash, or memory-mapped ASICs and FPGAs. The inteface is a maximum of 16-bits wide, but can also be used for 8-bit access.

NOR FLASH (Optional)

8 MB of on-board NOR FLASH memory is connected to the AM335x using the Serial Peripheral Interface (SPI1). The AM335x provides up to 2 SPI interfaces with both interfaces available on the SO-DIMM connector.

Configuration EEPROM

The MitySOM-335x contains a 256 x 8-bit EEPROM that is used to hold configuration data for the module. The EEPROM is connected to the AM335x using the I2C1 interface available on AM335x.

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External Interfaces

The AM335x makes extensive use of functional pin multiplexing to provide a highly configurable device that can be tailored to a multitude of applications. A list of the interfaces/functions that are available to the user is provided below.

- 2 Universal Serial Bus (USB) 2.0 High-Speed On the Go ports
- 2 Controller-Area Network (CAN) ports
- 2 Multichannel Audio Serial Ports (McASP)
- 2 Industrial Gigabit Ethernet MAC's (10/100/1000 Mbps)
- 3 MMC/SD/SDIO ports
- 8 input, 12 bit A/D Converter
- LCD Controller
- 3 Enhanced Capture (eCAP) Modules
- 3 Enhanced High-Resolution PWM (eHRPWN) modules
- 3 32-bit Enhanced Quadrature Pulse Encoder (eQPE) modules
- 4 Timers
- 2 Serial Peripheral (SPI) ports
    - SPI Port 1 is also connected to the on-board NOR FLASH memory
- 6 Universal Asynchronous Receive/Transmit (UART) ports
- 2 Inter-Integrated Circuit (I2C) ports
    - I2C Port 1 is also connected to the on-board EEPROM and PMIC
- General Purpose Memory Controller (GPMC) interface
    - A subset of this interface is also connected to the on-board NAND FLASH
- JTAG/Debugger port

Additionally, most of the pin multiplexed signals can be configured as general purpose I/O signals with interrupt capability.

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Software and Application Development Support

Users of the AM335x are encouraged to develop applications using the MitySOM-335x software development kit provided by Critical Link LLC. The SDK is an expansion of the TI platform support package for the AM335x and includes an implementation of an OpenEmbedded board support package providing an Angstrom based Linux root filesystem/distribution and compatible gcc compiler tool-chain with debugger.

Growth Options

The AM335x has been designed to support several upgrade options. These options include various speed grades, memory configurations, and operating temperature specifications including commercial and industrial temperature ranges. The available options are listed in the section below containing ordering information. For additional ordering information and details regarding these options, or to inquire about a particular configuration not listed below, please contact a Critical Link sales representative.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage, Vcc	5.2 V
Storage Temperature Range	-65°C to 80°C

OPERATING CONDITIONS

Commercial Temperature Range	0°C to 70°C
Industrial Temperature Range	-40°C to 85°C

SO-DIMM-204 Interface Description

The primary interface connector for the MitySOM-335x is the SO-DIMM card edge interface which contains 4 classes of signals:

- Power (PWR)
- Dedicated signals mapped to the on-board Power Management device (PM)
- Dedicated signals mapped to the AM335xZCZ device (335D)
- Multi-function signals mapped to the AM335xZCZ device (335M)

Table 1 contains a summary of the MitySOM-335x pin mapping.

Note that not all signals/mux options are available with all AM335x processor options (i.e. PRU's) and the I2C1 and I2C2 interface signals/mux options cannot be changed as they are used for dedicated functions on the MitySOM-335x module.

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Table 1 SO-DIMM Pin-Out

PIN	Class	Signal	PMIC Pin	AM3359 Pin	Power Domain	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option
1	PWR	VIN	-	-	-								
2	PWR	GND	-	-	-								
3	PWR	VIN	-	-	-								
4	PWR	GND	-	-	-								
5	PWR	VIN	-	-	-								
6	PWR	GND	-	-	-								
7	PWR	VIN	-	-	-								
8	PWR	GND	-	-	-								
9	PWR	VIN	-	-	-								
10	PWR	GND	-	-	-								
11	PWR	VIN	-	-	-								
12	PWR	GND	-	-	-								
13	PWR	VIN	-	-	-								
14	PWR	GND	-	-	-								
15	PWR	VIN	-	-	-								
16	PWR	GND	-	-	-								
17	PWR	GND	-	-	-								
18	PWR	GND	-	-	-								
19	PWR	GND	-	-	-								
20	PWR	GND	-	-	-								
21[2]	PWR	VIO_3P3	-	-	-								
22[2]	PWR	VIO_1P8	-	-	-								
23[2]	PWR	VIO_3P3	-	-	-								
24[2]	PWR	VIO_1P8	-	-	-								
25[2]	PWR	VIO_3P3	-	-	-								
26[2]	PWR	VIO_1P8	-	-	-								
27[2]	PWR	VIO_3P3	-	-	-								
28[2]	PWR	VIO_1P8	-	-	-								
29	335M	LCD_DATA0	-	R1	3.3V	lcd_data0	gpmc_a0	pr1_mii_mt0_clk	ehrpwm2A	pr1_pru1_pru_r30_0	pr1_pru1_pru_r31_0	gpio2_6	
30	PWR	LED_RTN	-	-									
31	335M	LCD_DATA1	-	R2	3.3V	lcd_data1	gpmc_a1	pr1_mii0_txen	ehrpwm2B	pr1_pru1_pru_r30_1	pr1_pru1_pru_r31_1	gpio2_7	
32[1]	PM	PWR_ON	33	-	3.3V								
33	335M	LCD_DATA2	-	R3	3.3V	lcd_data2	gpmc_a2	pr1_mii0_txd3	ehrpwm2_tripzone_input	pr1_pru1_pru_r30_2	pr1_pru1_pru_r31_2	gpio2_8	
34	PWR	VBACKUP	27	-									
35	335M	LCD_DATA3	-	R4	3.3V	lcd_data3	gpmc_a3	pr1_mii0_txd2	ehrpwm0_synco	pr1_pru1_pru_r30_3	pr1_pru1_pru_r31_3	gpio2_9	
36	PM	PMIC_SLEEP	37	-	3.3V								
37	PWR	GND	-	-	-								
38	PWR	GND	-	-	-								
39	335M	LCD_DATA4	-	T1	3.3V	lcd_data4	gpmc_a4	pr1_mii0_txd1	eQEP2A_in	pr1_pru1_pru_r30_4	pr1_pru1_pru_r31_4	gpio2_10	
40	PWR	GND	-	-	-								
41	335M	LCD_DATA5	-	T2	3.3V	lcd_data5	gpmc_a5	pr1_mii0_txd0	eQEP2B_in	pr1_pru1_pru_r30_5	pr1_pru1_pru_r31_5	gpio2_11	
42	PWR	GND	-	-	-								
43	335M	LCD_DATA6	-	T3	3.3V	lcd_data6	gpmc_a6	pr1_edio_data_in6	eQEP2_index	pr1_edio_data_out6	pr1_pru1_pru_r30_6	pr1_pru1_pru_r31_6	gpio2_12
44	PWR	VDDS_HV2	-	P10	VDDSHV2	VDDSHV2							

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PIN	Class	Signal	PMIC Pin	AM3359 Pin	Power Domain	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option
45	335M	LCD_DATA7	-	T4	3.3V	lcd_data7	gpmc_a7	pr1_edio_data_in7	eQEP2_strobe	pr1_edio_data_out7	pr1_pru1_pru_r30_7	pr1_pru1_pru_r31_7	gpio2_13
46	PWR	VDDS_HV2	-	P11	VDDSHV2	VDDSHV2							
47	335M	LCD_DATA8	-	U1	3.3V	lcd_data8	gpmc_a12	ehrpwm1_tripzone_input	mcasp0_aclkx	uart5_txd	pr1_mii0_rxd3	uart2_ctsn	gpio2_14
48	PWR	VDDS_HV4	-	H14	VDDSHV4	VDDSHV4							
49	335M	LCD_DATA9	-	U2	3.3V	lcd_data9	gpmc_a13	ehrpwm0_synco	mcasp0_fsx	uart5_rxd	pr1_mii0_rxd2	uart2_rtsn	gpio2_15
50	PWR	VDDS_HV4	-	J14	VDDSHV4	VDDSHV4							
51	335M	LCD_DATA10	-	U3	3.3V	lcd_data10	gpmc_a14	ehrpwm1A	mcasp0_axr0	pr1_mii0_rxd1	uart3_ctsn	gpio2_16	
52	PM	PMIC_INT_N	45	-	3.3V								
53	335M	LCD_DATA11	-	U4	3.3V	lcd_data11	gpmc_a15	ehrpwm1B	mcasp0_ahclkr	mcasp0_axr2	pr1_mii0_rxd0	uart3_rtsn	gpio2_17
54	PWR	GND	-	-	-								
55	PWR	GND	-	-	-								
56	PWR	GND	-	-	-								
57	335M	LCD_DATA12	-	V2	3.3V	lcd_data12	gpmc_a16	eQEP1A_in	mcasp0_aclkr	mcasp0_axr2	pr1_mii0_rxlink	uart4_ctsn	gpio0_8
58	335M	GPMC_A0	-	R13	3.3V	gpmc_a0	gmii2_txen	rgmii2_tctl	rmii2_txen	gpmc_a16	pr1_mii_mt1_clk	ehrpwm1_tripzone_input	gpio1_16
59	335M	LCD_DATA13	-	V3	3.3V	lcd_data13	gpmc_a17	eQEP1B_in	mcasp0_fsr	mcasp0_axr3	pr1_mii0_rxer	uart4_rtsn	gpio0_9
60	335M	GPMC_A1	-	V14	3.3V	gpmc_a1	gmii2_rxdv	rgmii2_rctl	mmc2_dat0	gpmc_a17	pr1_mii1_txd3	ehrpwm0_synco	gpio1_17
61	335M	LCD_DATA14	-	V4	3.3V	lcd_data14	gpmc_a18	eQEP1_index	mcasp0_axr1	uart5_rxd	pr1_mii_mr0_clk	uart5_ctsn	gpio0_10
62	335M	GPMC_A2	-	U14	3.3V	gpmc_a2	gmii2_txd3	rgmii2_td3	mmc2_dat1	gpmc_a18	pr1_mii1_txd2	ehrpwm1A	gpio1_18
63	335M	LCD_DATA15	-	T5	3.3V	lcd_data15	gpmc_a19	eQEP1_strobe	mcasp0_ahclkx	mcasp0_axr3	pr1_mii0_rxdv	uart5_rtsn	gpio0_11
64	335M	GPMC_A3	-	T14	3.3V	gpmc_a3	gmii2_txd2	rgmii2_td2	mmc2_dat2	gpmc_a19	pr1_mii1_txd1	ehrpwm1B	gpio1_19
65	335M	LCD_PCLK	-	V5	3.3V	lcd_pclk	gpmc_a10	pr1_mii0_crs	pr1_edio_data_in4	pr1_edio_data_out4	pr1_pru1_pru_r30_10	pr1_pru1_pru_r31_10	gpio2_24
66	335M	GPMC_A4	-	R14	3.3V	gpmc_a4	gmii2_txd1	rgmii2_td1	rmii2_txd1	gpmc_a20	pr1_mii1_txd0	eQEP1A_in	gpio1_20
67	335M	LCD_VSYNC	-	U5	3.3V	lcd_vsync	gpmc_a8	pr1_edio_data_in2	pr1_edio_data_out2	pr1_pru1_pru_r30_8	pr1_pru1_pru_r31_8	gpio2_22	
68	335M	GPMC_A5	-	V15	3.3V	gpmc_a5	gmii2_txd0	rgmii2_td0	rmii2_txd0	gpmc_a21	pr1_mii1_rxd3	eQEP1B_in	gpio1_21
69	335M	LCD_HSYNC	-	R5	3.3V	lcd_hsync	gpmc_a9	pr1_edio_data_in3	pr1_edio_data_out3	pr1_pru1_pru_r30_9	pr1_pru1_pru_r31_9	gpio2_23	
70	335M	GPMC_A6	-	U15	3.3V	gpmc_a6	gmii2_txclk	rgmii2_tclk	mmc2_dat4	gpmc_a22	pr1_mii1_rxd2	eQEP1_index	gpio1_22
71	335M	LCD_AC_BIAS_EN	-	R6	3.3V	lcd_ac_bias_en	gpmc_a11	pr1_mii1_crs	pr1_edio_data_in5	pr1_edio_data_out5	pr1_pru1_pru_r30_11	pr1_pru1_pru_r31_11	gpio2_25
72	335M	GPMC_A7	-	T15	3.3V	gpmc_a7	gmii2_rxclk	rgmii2_rclk	mmc2_dat5	gpmc_a23	pr1_mii1_rxd1	eQEP1_strobe	gpio1_23
73	PWR	GND	-	-	-								
74	PWR	GND	-	-	-								
75	335D	GPMC_AD0	-	U7	3.3V	gpmc_ad0							
76	335M	GPMC_A8	-	V16	3.3V	gpmc_a8	gmii2_rxd3	rgmii2_rd3	mmc2_dat6	gpmc_a24	pr1_mii1_rxd0	mcasp0_aclkx	gpio1_24
77	335D	GPMC_AD1	-	V7	3.3V	gpmc_ad1							
78	335M	GPMC_A9	-	U16	3.3V	gpmc_a9	gmii2_rxd2	rgmii2_rd2	mmc2_dat7	gpmc_a25	pr1_mii_mr1_clk	mcasp0_fsx	gpio1_25
79	335D	GPMC_AD2	-	R8	3.3V	gpmc_ad2							
80	335M	GPMC_A10	-	T16	3.3V	gpmc_a10	gmii2_rxd1	rgmii2_rd1	rmii2_rxd1	gpmc_a26	pr1_mii1_rxdv	mcasp0_axr0	gpio1_26
81	335D	GPMC_AD3	-	T8	3.3V	gpmc_ad3							
82	335M	GPMC_A11	-	V17	3.3V	gpmc_a11	gmii2_rxd0	rgmii2_rd0	rmii2_rxd0	gpmc_a27	pr1_mii1_rxer	mcasp0_axr1	gpio1_27
83	335D	GPMC_AD4	-	U8	3.3V	gpmc_ad4							
84	335M	GPMC_CLK	-	V12	VDDSHV2	gpmc_clk	lcd_memory_clk	gpmc_wait1	mmc2_clk	pr1_mii1_crs	pr1_mdio_mdclk	mcasp0_fsr	gpio2_1
85	335D	GPMC_AD5	-	V8	3.3V	gpmc_ad5							
86	335D	GPMC_BEN0_CLE	-	T6	3.3V	gpmc_be0n_cle							
87	335D	GPMC_AD6	-	R9	3.3V	gpmc_ad6							
88	335D	GPMC_ADVN_ALE	-	R7	3.3V	gpmc_advn_ale							

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PIN	Class	Signal	PMIC Pin	AM3359 Pin	Power Domain	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option
89	335D	GPMC_AD7	-	T9	3.3V	gpmc_ad7							
90	335D	GPMC_OEN_RE_N	-	T7	3.3V	gpmc_oen_ren							
91	PWR	GND	-	-	-								
92	PWR	GND	-	-	-								
93	335M	GPMC_AD8	-	U10	VDDSHV2	gpmc_ad8	lcd_data23	mmc1_dat0	mmc2_dat4	ehrpwm2A	pr1_mii_mt0_clk	gpio0_22	
94	335M	GPMC_CSN3	-	T13	VDDSHV2	gpmc_csn3	mmc2_cmd	pr1_mii0_crs	pr1_mdio_data	EMU4	gpio2_0		
95	335M	GPMC_AD9	-	T10	VDDSHV2	gpmc_ad9	lcd_data22	mmc1_dat1	mmc2_dat5	ehrpwm2B	pr1_mii0_col	gpio0_23	
96		No Connect											
97	335M	GPMC_AD10	-	T11	VDDSHV2	gpmc_ad10	lcd_data21	mmc1_dat2	mmc2_dat6	ehrpwm2_tripzone_input	pr1_mii0_txen	gpio0_26	
98	335D	GPMC_WE_N	-	U6	3.3V	gpmc_wen							
99	335M	GPMC_AD11	-	U12	VDDSHV2	gpmc_ad11	lcd_data20	mmc1_dat3	mmc2_dat7	ehrpwm0_synco	pr1_mii0_txd3	gpio0_27	
100	335D	GPMC_WAIT0	-	T17	3.3V	gpmc_wait0							
101	335M	GPMC_AD12	-	T12	VDDSHV2	gpmc_ad12	lcd_data19	mmc1_dat4	mmc2_dat0	eQEP2A_in	pr1_mii0_txd2	pr1_pru0_pru_r30_14	gpio1_12
102	335M	GPMC_BEN1	-	U18	3.3V	gpmc_be1n	gmii2_col	gpmc_csn6	mmc2_dat3	gpmc_dir	pr1_mii1_rxlink	mcasp0_aclkr	gpio1_28
103	335M	GPMC_AD13	-	R12	VDDSHV2	gpmc_ad13	lcd_data18	mmc1_dat5	mmc2_dat1	eQEP2B_in	pr1_mii0_txd1	pr1_pru0_pru_r30_15	gpio1_13
104	335D	GPMC_WP_N	-	U17	3.3V	gpmc_wpn							
105	335M	GPMC_AD14	-	V13	VDDSHV2	gpmc_ad14	lcd_data17	mmc1_dat6	mmc2_dat2	eQEP2_index	pr1_mii0_txd0	pr1_pru0_pru_r31_14	gpio1_14
106		No Connect											
107	335M	GPMC_AD15	-	U13	VDDSHV2	gpmc_ad15	lcd_data16	mmc1_dat7	mmc2_dat3	eQEP2_strobe	pr1_ecap0_ecap_capin_apwm_o	pr1_pru0_pru_r31_15	gpio1_15
108		No Connect											
109	PWR	GND	-	-	-								
110	PWR	GND	-	-	-								
111	335M	GPMC_CSN2	-	V9	3.3V	gpmc_csn2	gpmc_be1n	mmc1_cmd	pr1_edio_data_in7	pr1_edio_data_out7	pr1_pru1_pru_r30_13	pr1_pru1_pru_r31_13	gpio1_31
112	335M	GMII1_RXD0	-	M16	3.3V	gmii1_rxd0	rmii1_rxd0	rgmii1_rd0	mcasp1_ahclkx	mcasp1_ahclkr	mcasp1_aclkr	mcasp0_axr3	gpio2_21
113	335M	GPMC_CSN1	-	U9	3.3V	gpmc_csn1	gpmc_clk	mmc1_clk	pr1_edio_data_in6	pr1_edio_data_out6	pr1_pru1_pru_r30_12	pr1_pru1_pru_r31_12	gpio1_30
114	335M	GMII1_RXD1	-	L15	3.3V	gmii1_rxd1	rmii1_rxd1	rgmii1_rd1	mcasp1_axr3	mcasp1_fsr	eQEP0_strobe	mmc2_clk	gpio2_20
115	335D	USB0_VBUS	-	P15		USB0_VBUS							
116	335M	GMII1_RXD2	-	L16	3.3V	gmii1_rxd2	uart3_txd	rgmii1_rd2	mmc0_dat4	mmc1_dat3	uart1_rin	mcasp0_axr1	gpio2_19
117	335D	USB0_ID	-	P16		USB0_ID							
118	335M	GMII1_RXD3	-	L17	3.3V	gmii1_rxd3	uart3_rxd	rgmii1_rd3	mmc0_dat5	mmc1_dat2	uart1_dtrn	mcasp0_axr0	gpio2_18
119	335D	USB1_VBUS	-	T18		USB1_VBUS							
120	335M	GMII1_RXCLK	-	L18	3.3V	gmii1_rxclk	uart2_txd	rgmii1_rclk	mmc0_dat6	mmc1_dat1	uart1_dsrn	mcasp0_fsx	gpio3_10
121	335D	USB1_DP	-	R17		USB1_DP							
122	335M	GMII1_RXDV	-	J17	3.3V	gmii1_rxdv	lcd_memory_clk	rgmii1_rctl	uart5_txd	mcasp1_aclkx	mmc2_dat0	mcasp0_aclkr	gpio3_4
123	335D	USB1_DM	-	R18		USB1_DM							
124		No Connect											
125	335D	USB1_CE	-	P18		USB1_CE							
126	335M	GMII1_TXCLK	-	K18	3.3V	gmii1_txclk	uart2_rxd	rgmii1_tclk	mmc0_dat7	mmc1_dat0	uart1_dcdn	mcasp0_aclkx	gpio3_9
127	PWR	GND	-	-	-								
128	335M	GMII1_TXD0	-	K17	3.3V	gmii1_txd0	rmii1_txd0	rgmii1_td0	mcasp1_axr2	mcasp1_aclkr	eQEP0B_in	mmc1_clk	gpio0_28
129	335D	USB1_ID	-	P17		USB1_ID							
130	335M	GMII1_TXD1	-	K16	3.3V	gmii1_txd1	rmii1_txd1	rgmii1_td1	mcasp1_fsr	mcasp1_axr1	eQEP0A_in	mmc1_cmd	gpio0_21
131	335D	USB0_DM	-	N18		USB0_DM							
132	335M	GMII1_TXD2	-	K15	3.3V	gmii1_txd2	dcan0_rx	rgmii1_td2	uart4_txd	mcasp1_axr0	mmc2_dat2	mcasp0_ahclkx	gpio0_17

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PIN	Class	Signal	PMIC Pin	AM3359 Pin	Power Domain	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option
133	335D	USB0_DP	-	N17		USB0_DP							
134	335M	GMII1_TXD3	-	J18	3.3V	gmii1_txd3	dcan0_tx	rgmii1_td3	uart4_rxd	mcasp1_fsx	mmc2_dat1	mcasp0_fsr	gpio0_16
135	335D	USB0_CE	-	M15		USB0_CE							
136	335M	GMII1_TXEN	-	J16	3.3V	gmii1_txen	rmii1_txen	rgmii1_tctl	timer4	mcasp1_axr0	eQEP0_index	mmc2_cmd	gpio3_3
137	335M	USB1_DRVVBUS	-	F15	3.3V	USB1_DRVVBUS	gpio3_13						
138	335M	GMII1_COL	-	H16	3.3V	gmii1_col	rmii2_refclk	spi1_sclk	uart5_rxd	mcasp1_axr2	mmc2_dat3	mcasp0_axr2	gpio3_0
139	335M	USB0_DRVVBUS	-	F16	3.3V	USB0_DRVVBUS	gpio0_18						
140		No Connect											
141	335M	MDC	-	M18	3.3V	mdio_clk	timer5	uart5_txd	uart3_rtsn	mmc0_sdwp	mmc1_clk	mmc2_clk	gpio0_1
142		No Connect											
143	335M	MDIO	-	M17	3.3V	mdio_data	timer6	uart5_rxd	uart3_ctsn	mmc0_sdcd	mmc1_cmd	mmc2_cmd	gpio0_0
144	335M	MCASP0_AXR1	-	D13	3.3V	mcasp0_axr1	eQEP0_index	mcasp1_axr0	EMU3	pr1_pru0_pru_r30_6	pr1_pru0_pru_r31_6	gpio3_20	
145	335M	RMII1_REFCLK	-	H18	3.3V	rmii1_refclk	xdma_event_intr2	spi1_cs0	uart5_txd	mcasp1_axr3	mmc0_pow	mcasp1_ahclkx	gpio0_29
146	PWR	GND	-	-	-								
147	335D	I2C1_SDA	-	H17	3.3V	I2C1_SDA							
148	335M	MCASP0_FSR	-	C13	3.3V	mcasp0_fsr	eQEP0B_in	mcasp0_axr3	mcasp1_fsx	EMU2	pr1_pru0_pru_r30_5	pr1_pru0_pru_r31_5	gpio3_19
149	335D	I2C1_SCL	-	J15	3.3V	I2C1_SCL							
150	335M	MCASP0_ACLKR	-	B12	3.3V	mcasp0_aclkr	eQEP0A_in	mcasp0_axr2	mcasp1_aclkx	mmc0_sdwp	pr1_pru0_pru_r30_4	pr1_pru0_pru_r31_4	gpio3_18
151	335M	MMC0_CMD	-	G18	VDDSHV4	mmc0_cmd	gpmc_a25	uart3_rtsn	uart2_txd	dcan1_rx	pr1_pru0_pru_r30_13	pr1_pru0_pru_r31_13	gpio2_31
152	335M	MCASP0_ACLKX	-	A13	3.3V	mcasp0_aclkx	ehrpwm0A	spi1_sclk	mmc0_sdcd	pr1_pru0_pru_r30_0	pr1_pru0_pru_r31_0	gpio3_14	
153	335M	MMC0_CLK	-	G17	VDDSHV4	mmc0_clk	gpmc_a24	uart3_ctsn	uart2_rxd	dcan1_tx	pr1_pru0_pru_r30_12	pr1_pru0_pru_r31_12	gpio2_30
154	335M	MCASP0_AHCLKX	-	A14	3.3V	mcasp0_ahclkx	eQEP0_strobe	mcasp0_axr3	mcasp1_axr1	EMU4	pr1_pru0_pru_r30_7	pr1_pru0_pru_r31_7	gpio3_21
155	335M	MMC0_DAT0	-	G16	VDDSHV4	mmc0_dat0	gpmc_a23	uart5_rtsn	uart3_txd	uart1_rin	pr1_pru0_pru_r30_11	pr1_pru0_pru_r31_11	gpio2_29
156	335D	EXTINT_N	-	B18	3.3V	nNMI							
157	335M	MMC0_DAT1	-	G15	VDDSHV4	mmc0_dat1	gpmc_a22	uart5_ctsn	uart3_rxd	uart1_dtrn	pr1_pru0_pru_r30_10	pr1_pru0_pru_r31_10	gpio2_28
158	335D	WARMRST_N	-	A10	3.3V	nRESETIN_OUT							
159	335M	MMC0_DAT2	-	F18	VDDSHV4	mmc0_dat2	gpmc_a21	uart4_rtsn	timer6	uart1_dsrn	pr1_pru0_pru_r30_9	pr1_pru0_pru_r31_9	gpio2_27
160	335M	EMU0	-	C14	3.3V	EMU0	gpio3_7						
161	335M	MMC0_DAT3	-	F17	VDDSHV4	mmc0_dat3	gpmc_a20	uart4_ctsn	timer5	uart1_dcdn	pr1_pru0_pru_r30_8	pr1_pru0_pru_r31_8	gpio2_26
162	335M	EMU1	-	B14	3.3V	EMU1	gpio3_8						
163	PWR	GND	-	-	-								
164	PWR	GND	-	-	-								
165	335M	UART0_CTSN	-	E18	3.3V	uart0_ctsn	uart4_rxd	dcan1_tx	I2C1_SDA	spi1_d0	timer7	pr1_edc_sync0_out	gpio1_8
166	335D	TCK	-	A12	3.3V	TCK							
167	335M	UART0_RTSN	-	E17	3.3V	uart0_rtsn	uart4_txd	dcan1_rx	I2C1_SCL	spi1_d1	spi1_cs0	pr1_edc_sync1_out	gpio1_9
168	335D	TDI	-	B11	3.3V	TDI							
169	335M	UART0_TXD	-	E16	3.3V	uart0_txd	spi1_cs1	dcan0_rx	I2C2_SCL	eCAP1_in_PWM1_out	pr1_pru1_pru_r30_15	pr1_pru1_pru_r31_15	gpio1_11
170	335D	TDO	-	A11	3.3V	TDO							
171	335M	UART0_RXD	-	E15	3.3V	uart0_rxd	spi1_cs0	dcan0_tx	I2C2_SDA	eCAP2_in_PWM2_out	pr1_pru1_pru_r30_14	pr1_pru1_pru_r31_14	gpio1_10
172	335D	TMS	-	C11	3.3V	TMS							

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PIN	Class	Signal	PMIC Pin	AM3359 Pin	Power Domain	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option	Signal Option
173	335M	UART1_RXD	-	D16	3.3V	uart1_rxd	mmc1_sdwp	dcan1_tx	I2C1_SDA	pr1_uart0_rxd	pr1_pru1_pru_r31_16	gpio0_14	
174	335D	TRSTN	-	B10	3.3V	nTRST							
175	335M	UART1_TXD	-	D15	3.3V	uart1_txd	mmc2_sdwp	dcan1_rx	I2C1_SCL	pr1_uart0_txd	pr1_pru0_pru_r31_16	gpio0_15	
176	PWR	VREFN	-	A9	1.8V	VREFN							
177	335M	I2C0_SDA	-	C17	3.3V	I2C0_SDA	timer4	uart2_ctsn	eCAP2_in_PWM2_out	gpio3_5			
178	PWR	VREFP	-	B9	1.8V	VREFP							
179	335M	I2C0_SCL	-	C16	3.3V	I2C0_SCL	timer7	uart2_rtsn	eCAP1_in_PWM1_out	gpio3_6			
180	335D	EXT_WAKEUP	-	C5	1.8V	EXT_WAKEUP							
181	PWR	GND	-	-	-								
182	PWR	GND	-	-	-								
183	335M	SPI0_D0	-	B17	3.3V	spi0_d0	uart2_txd	I2C2_SCL	ehrpwm0B	pr1_uart0_rts_n	pr1_edio_latch_in	EMU3	gpio0_3
184	335D	AIN0	-	B6	1.8V	AIN0							
185	335M	SPI0_D1	-	B16	3.3V	spi0_d1	mmc1_sdwp	I2C1_SDA	ehrpwm0_tripzone_input	pr1_uart0_rxd	pr1_edio_data_in0	pr1_edio_data_out0	gpio0_4
186	335D	AIN1	-	C7	1.8V	AIN1							
187	335M	SPI0_SCLK	-	A17	3.3V	spi0_sclk	uart2_rxd	I2C2_SDA	ehrpwm0A	pr1_uart0_cts_n	pr1_edio_sof	EMU2	gpio0_2
188	335D	AIN2	-	B7	1.8V	AIN2							
189	335M	SPI0_CS1	-	C15	3.3V	spi0_cs1	uart3_rxd	eCAP1_in_PWM1_out	mmc0_pow	xdma_event_intr2	mmc0_sdcd	EMU4	gpio0_6
190	335D	AIN3	-	A7	1.8V	AIN3							
191	335M	SPI0_CS0	-	A16	3.3V	spi0_cs0	mmc2_sdwp	I2C1_SCL	ehrpwm0_synci	pr1_uart0_txd	pr1_edio_data_in1	pr1_edio_data_out1	gpio0_5
192	335D	AIN4	-	C8	1.8V	AIN4							
193	335D	SPI1_SCLK	-	C18	3.3V	spi1_sclk							
194	335D	AIN5	-	B8	1.8V	AIN5							
195	335D	SPI1_D0_MOSI	-	B13	3.3V	spi1_d0							
196	335D	AIN6	-	A8	1.8V	AIN6							
197	335D	SPI1_D1_MISO	-	D12	3.3V	spi1_d1							
198	335D	AIN7	-	C9	1.8V	AIN7							
199	PWR	GND	-	-	-								
200	PWR	GND	-	-	-								
201	335M	XDMA_EVENT_INTR1	-	D14	3.3V	xdma_event_intr1	tclkin	clkout2	timer7	pr1_pru0_pru_r31_16	EMU3	gpio0_20	
202	PWR	AGND	-	-	-								
203	335M	XDMA_EVENT_INTR0	-	A15	3.3V	xdma_event_intr0	timer4	clkout1	spi1_cs1	pr1_pru1_pru_r31_16	EMU2	gpio0_19	
204	PWR	AGND	-	-	-								

Note 1: The PowerOn pin (32) has a pull-up resistor on the module so it can be left floating if user control is not desired.

Note 2: Please reference Table 2 for information on the maximum current supply of these voltage outputs.

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ELECTRICAL CHARACTERISTICS

Table 2: Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIN	Voltage supply, volt input.		3.2	3.3	5.2	Volts
I_{VIO_3P3}	Max current draw[3]	3.3 volt IO output			500	mA
I_{VIO_1P8}	Max current draw[3]	1.8 volt IO output			500	mA
$I_{3.3}$	Quiescent Current draw[1]	3.3 volt input, **DDR2**	-	240	-	mA
$I_{3.3\text{-}max}$	Max current draw[1]	3.3 volt input, **DDR2**	-	520	TBS	mA
$I_{3.3}$	Quiescent Current draw[1]	3.3 volt input, **DDR3**	-	300	-	mA
$I_{3.3\text{-}max}$	Max current draw[1]	3.3 volt input, **DDR3**	-	520	TBS	mA
$I_{VBackup}$	VBACKUP Current draw[2]	3.3 VIN applied to SoM	-	<1	1	uA
$I_{VBackup\text{-}Active}$	VBACKUP Current draw	PMIC RTC active	-	10.2	-	uA
FCPU	CPU internal clock Frequency (PLL output)		275	800	1000	MHz
FEMIF	GPMC bus frequency		-		-	MHz

1. Power utilization of the MitySOM-335x is heavily dependent on end-user application. Major factors include: ARM CPU PLL configuration, CPU Utilization, and external DDR2/3 RAM utilization.
2. VBACKUP current measurement limited by test equipment, current consumption was less than 1 micro amp.
3. The MitySOM-335x module provides both 1.8V (Pins 22, 24, 26 and 28) and 3.3V (Pins 21, 23, 25 and 27) output supplies from the module. These outputs are sequenced from the PMIC and the maximum power output specified should not be exceeded as these supplies also power the module itself.

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ORDERING INFORMATION

The following table lists the standard module configurations. For shipping status, availability, and lead time of these or other configurations please contact your Critical Link representative.

Table 3: Standard Model Numbers

Model	ARM Speed	NOR	NAND Flash	RAM	Operating Temp
3359-GX-226-RC	720 MHz	8MB	256MB	256MB DDR2	0°C to 70° C
3359-GX-226-RL	720 MHz	8MB	256MB	256MB DDR2	-40° C to 70° C
3354-HX-X38-RI	800 MHz	N/A	512MB	512MB DDR3	-40° C to 85° C
3354-GX-X38-RC	720 MHz	N/A	512MB	512MB DDR3	0°C to 70° C
3354-GX-XX7-RC	720 MHz	N/A	N/A	256MB DDR3	0°C to 70° C
3352-GX-X27-RC	720 MHz	N/A	256MB	256MB DDR3	0°C to 70° C

Note: TI's AM335x Silicon Revision 1.0 has maximum frequency of 720MHz

MECHANICAL INTERFACE

A mechanical outline of the MitySOM-335x is illustrated in Figure 2, below.

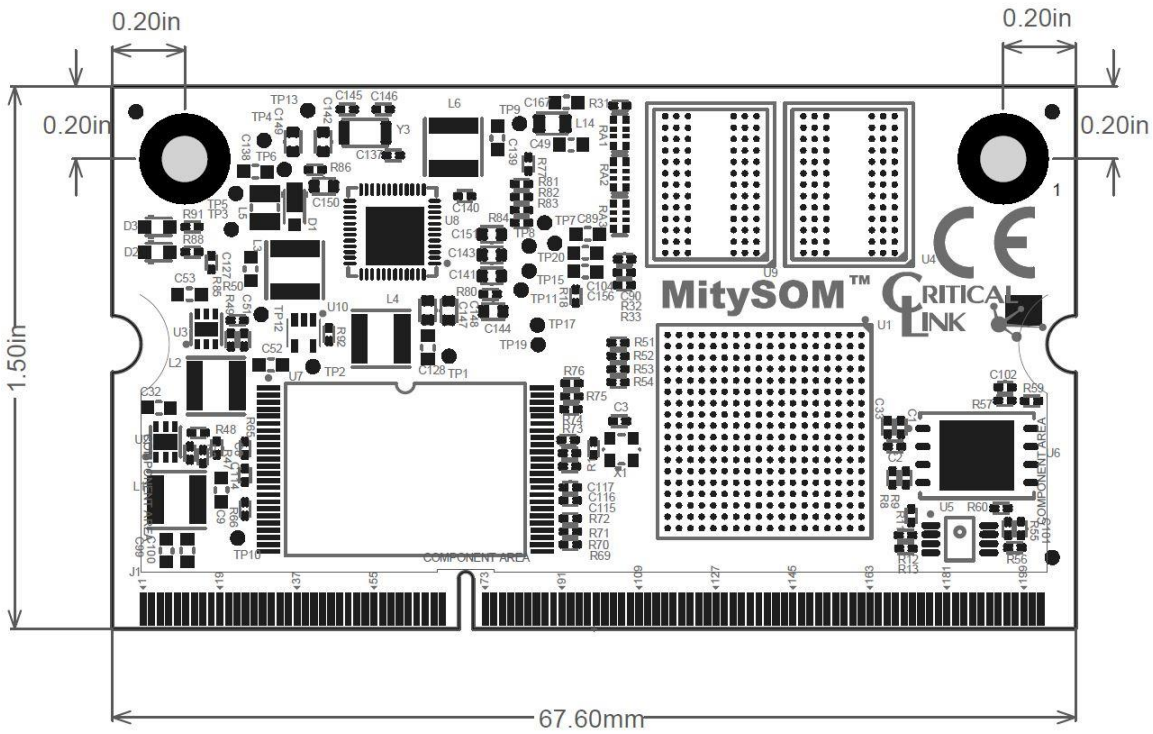

Figure 2 MitySOM-335x Mechanical Outline

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REVISION HISTORY

Date	Change Description
1-NOV-2011	Draft Spec.
16-NOV-2011	Pre-release updates.
3-DEC-2011	Add mechanical outline.
7-DEC-2011	Supplemented pin descriptions. Added External interfaces. Added on board storage description New block diagram showing third I2C interface
13-DEC-2011	Corrected pin list (pins 30,32,34,52)
8-FEB-2012	Update photo, remove 3359-EX-227-RC from orderable parts list.
20-MAR-2012	Remove preliminary markings and update input voltage level.
10-JUL-2012	Part number correction and add MIL-STD-810F.
3-MAR-2013	Change to MitySOM-335x Processor Card and DDR3 support.
27-MAR-2013	Add notes about I2C interface availability and VIO output current maximums
8-JUL-2013	Update maximum CPU speed to 1GHZ and update available module numbers.
17-MAR-2014	Update MitySOM product name.

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- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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