



# TPS25924x 12-V eFuse with Over Voltage Protection and Blocking FET Control

## 1 Features

- $V_{\text{OPERATING}} = 4.5 \text{ V to } 13.8 \text{ V}$ ,  $V_{\text{ABSMAX}} = 20 \text{ V}$
- Integrated 28-m $\Omega$  Pass MOSFET
- Fixed 15-V Over Voltage Clamp
- 1-A to 5-A Adjustable  $I_{\text{LIMIT}}$
- $\pm 8\%$   $I_{\text{LIMIT}}$  Accuracy at 3.7A
- Reverse Current Blocking Support
- Programmable OUT Slew Rate, UVLO
- Built-in Thermal Shutdown
- UL 2367 Recognition Pending
- Safe During Single Point Failure Test (UL60950)
- Small Foot Print – 10L (3 mm x 3 mm) VSON

## 2 Applications

- Adapter Powered Devices
- HDD and SSD Drives
- Set Top Boxes
- Servers / AUX Supplies
- Fan Control
- PCI/PCIe Cards

## 3 Description

The TPS25924x family of eFuses is a highly integrated circuit protection and power management solution in a tiny package. The devices use few external components and provide multiple protection modes. They are a robust defense against overloads, shorts circuits, voltage surges, excessive inrush current, and reverse current.

Current limit level can be set with a single external resistor. Over voltage events are limited by internal clamping circuits to a safe fixed maximum, with no external components required.

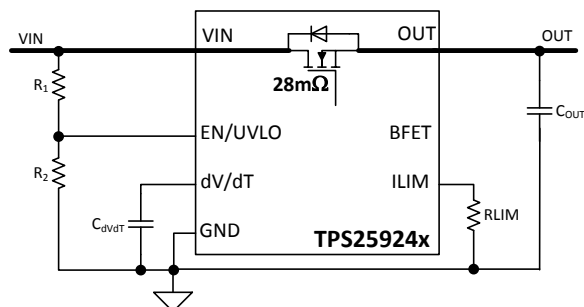
Applications with particular voltage ramp requirements can set dV/dT with a single capacitor to ensure proper output ramp rates. Many systems, such as SSDs, must not allow holdup capacitance energy to dump back through the FET body diode onto a drooping or shorted input bus. The BFET pin is for such systems. An external NFET can be connected “Back to Back (B2B)” with the TPS25924x output and the gate driven by BFET to prevent current flow from load to source (see [Figure 43](#)).

### Device Information<sup>(1)</sup>

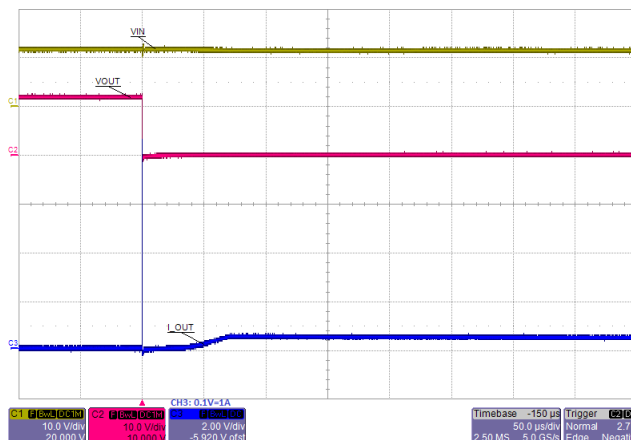
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS259241	VSON (10)	3.00 mm x 3.00 mm
TPS259240		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Application Schematic



### Transient: Output Short Circuit



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>17</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Application Information.....	17
<b>3 Description</b> .....	<b>1</b>	9.2 Typical Applications .....	17
<b>4 Revision History</b> .....	<b>2</b>	<b>10 Power Supply Recommendations</b> .....	<b>23</b>
<b>5 Device Comparison Table</b> .....	<b>3</b>	10.1 Transient Protection .....	23
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	10.2 Output Short-Circuit Measurements .....	23
<b>7 Specifications</b> .....	<b>4</b>	<b>11 Layout</b> .....	<b>24</b>
7.1 Absolute Maximum Ratings .....	4	11.1 Layout Guidelines .....	24
7.2 ESD Ratings .....	4	11.2 Layout Example .....	24
7.3 Recommended Operating Conditions.....	4	<b>12 Device and Documentation Support</b> .....	<b>25</b>
7.4 Thermal Information .....	5	12.1 Device Support .....	25
7.5 Electrical Characteristics.....	5	12.2 Documentation Support .....	25
7.6 Timing Requirements .....	6	12.3 Related Links .....	25
7.7 Typical Characteristics .....	7	12.4 Community Resources.....	25
<b>8 Detailed Description</b> .....	<b>13</b>	12.5 Trademarks .....	25
8.1 Overview .....	13	12.6 Electrostatic Discharge Caution.....	25
8.2 Functional Block Diagram .....	13	12.7 Glossary .....	25
8.3 Feature Description.....	13	<b>13 Mechanical, Packaging, and Orderable</b>	
8.4 Device Functional Modes.....	16	<b>Information</b> .....	<b>25</b>

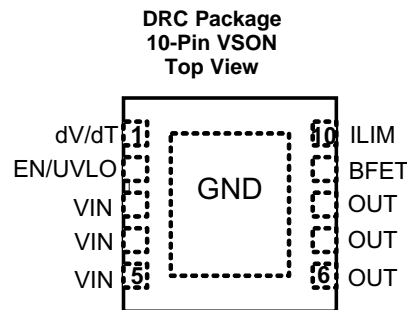
## 4 Revision History

Changes from Original (August 2015) to Revision A	Page
• Changed from Product Preview to Production Data .....	1

## 5 Device Comparison Table

PART NUMBER	UV	OV CLAMP	FAULT RESPONSE	STATUS
TPS259241	4.3 V	15 V	Auto Retry	Active
TPS259240	4.3 V	15 V	Latched	Active

## 6 Pin Configuration and Functions



### Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
BFET	9	Connect this pin to the gate of a blocking NFET. See the <a href="#">Feature Description</a> section. This pin can be left floating if it is not used.
dV/dT	1	Tie a capacitor from this pin to GND to control the ramp rate of OUT at device turn-on.
EN/UVLO	2	This is a dual function control pin. When used as an ENABLE pin and pulled down, it shuts off the internal pass MOSFET and pulls BFET to GND. When pulled high, it enables the device and BFET. As an UVLO pin, it can be used to program different UVLO trip point via external resistor divider.
GND	Thermal Pad	GND
ILIM	10	A resistor from this pin to GND will set the overload and short circuit limit.
OUT	6-8	Output of the device
VIN	3-5	Input supply voltage

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted) <sup>(1)</sup> <sup>(2)</sup>

		MIN	MAX	UNIT
Supply voltage <sup>(1)</sup>	VIN	−0.3	20	V
	VIN (10 ms Transient)		22	
Output voltage	OUT	−0.3	VIN + 0.3	V
	OUT (Transient < 1 μs)		−1.2	V
Voltage	ILIM	−0.3	7	V
	EN/UVLO	−0.3	7	
	dV/dT	−0.3	7	
	BFET	−0.3	30	
Storage temperature range, T <sub>stg</sub>		−65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential voltages, are with respect to network ground terminal.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage range	VIN	4.5	12	13.8	V
	BFET	0		VIN+6	
	dV/dT, EN/UVLO	0		6	
	ILIM	0		3	
Continuous output current	I <sub>OUT</sub>	0		5	A
Resistance	ILIM	10	100	162	kΩ
External capacitance	OUT	0.1	1	1000	μF
	dV/dT		1	1000	nF
Operating junction temperature range, T <sub>J</sub>		−40	25	125	°C
Operating Ambient temperature range, T <sub>A</sub>		−40	25	85	°C

## 7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

THERMAL METRIC		TPS25924x	UNIT
		DRC (VSON)	
		10 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	45.9	°C/W
R <sub>θJCTop</sub>	Junction-to-case (top) thermal resistance	53	
R <sub>θJB</sub>	Junction-to-board thermal resistance	21.2	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.2	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	21.4	
R <sub>θJCbot</sub>	Junction-to-case (bottom) thermal resistance	5.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

–40°C ≤ T<sub>J</sub> ≤ 125°C, V<sub>IN</sub> = 12 V, V<sub>EN</sub> /UVLO = 2 V, R<sub>ILIM</sub> = 100 kΩ, C<sub>dVdT</sub> = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VIN (INPUT SUPPLY)</b>						
V <sub>UVR</sub>	UVLO threshold, rising		4.15	4.3	4.45	V
V <sub>UVhyst</sub>	UVLO hysteresis <sup>(1)</sup>			5%		
I <sub>QON</sub>	Supply current	Enabled: EN/UVLO = 2 V	0.3	0.42	0.55	mA
I <sub>QOFF</sub>		EN/UVLO = 0 V		0.13	0.225	mA
V <sub>OVC</sub>	Over-voltage clamp	V <sub>IN</sub> > 16.5 V, I <sub>OUT</sub> = 10 mA	13.8	15	16.5	V
<b>EN/UVLO (ENABLE/UVLO INPUT)</b>						
V <sub>ENR</sub>	EN Threshold voltage, rising		1.37	1.4	1.44	V
V <sub>ENF</sub>	EN Threshold voltage, falling		1.32	1.35	1.39	V
I <sub>EN</sub>	EN Input leakage current	0 V ≤ V <sub>EN</sub> ≤ 5 V	–100	0	100	nA
<b>dV/dT (OUTPUT RAMP CONTROL)</b>						
I <sub>dVdT</sub>	dV/dT Charging current <sup>(1)</sup>	V <sub>dVdT</sub> = 0 V		220		nA
R <sub>dVdT_disch</sub>	dV/dT Discharging resistance	EN/UVLO = 0 V, I <sub>dVdT</sub> = 10 mA sinking	50	73	100	Ω
V <sub>dVdTmax</sub>	dV/dT Max capacitor voltage <sup>(1)</sup>			5.5		V
GAIN <sub>dVdT</sub>	dV/dT to OUT gain <sup>(1)</sup>	ΔV <sub>dVdT</sub>		4.85		V/V
<b>ILIM (CURRENT LIMIT PROGRAMMING)</b>						
I <sub>ILIM</sub>	ILIM Bias current <sup>(1)</sup>			10		μA
I <sub>OL</sub>	Overload current limit <sup>(2)</sup>	R <sub>ILIM</sub> = 10 kΩ, V <sub>VIN-OUT</sub> = 1 V		1.02		A
		R <sub>ILIM</sub> = 45.3 kΩ, V <sub>VIN-OUT</sub> = 1 V	1.79	2.10	2.42	
		R <sub>ILIM</sub> = 100 kΩ, V <sub>VIN-OUT</sub> = 1 V	3.46	3.75	4.03	
		R <sub>ILIM</sub> = 150 kΩ, V <sub>VIN-OUT</sub> = 1 V	4.5	5.1	5.7	
I <sub>OL-R-Short</sub>		R <sub>ILIM</sub> = 0 Ω, Shorted Resistor Current Limit (Single Point Failure Test: UL60950) <sup>(1)</sup>		0.84		A
I <sub>OL-R-Open</sub>		R <sub>ILIM</sub> = OPEN, Open Resistor Current Limit (Single Point Failure Test: UL60950) <sup>(1)</sup>		0.73		A
I <sub>SCL</sub>	Short-circuit current limit <sup>(2)</sup>	R <sub>ILIM</sub> = 10 kΩ, V <sub>VIN-OUT</sub> = 12 V		1		A
		R <sub>ILIM</sub> = 45.3 kΩ, V <sub>VIN-OUT</sub> = 12 V	1.66	1.98	2.37	
		R <sub>ILIM</sub> = 100 kΩ, V <sub>VIN-OUT</sub> = 12 V	2.90	3.32	3.85	
		R <sub>ILIM</sub> = 150 kΩ, V <sub>VIN-OUT</sub> = 12 V	3.7	4.5	5.5	
RATIO <sub>FASTRIP</sub>	Fast-Trip comparator level w.r.t. overload current limit <sup>(1)</sup>	I <sub>FASTRIP</sub> : I <sub>OL</sub>		160%		
V <sub>OpenILIM</sub>	ILIM Open resistor detect threshold <sup>(1)</sup>	V <sub>ILIM</sub> Rising, R <sub>ILIM</sub> = OPEN		3.1		V

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

(2) Pulsed testing techniques used during this test maintain junction temperature approximately equal to ambient temperature.

## Electrical Characteristics (continued)

–40°C ≤ T<sub>J</sub> ≤ 125°C, V<sub>IN</sub> = 12 V, V<sub>EN/UVLO</sub> = 2 V, R<sub>ILIM</sub> = 100 kΩ, C<sub>dVdT</sub> = OPEN. All voltages referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT (PASS FET OUTPUT)						
R <sub>DS(on)</sub>	FET ON resistance	T <sub>J</sub> = 25°C	21	28	37	mΩ
		T <sub>J</sub> = 125°C		39	48	
I <sub>OUT-OFF-LKG</sub>	OUT Bias current in off state	V <sub>EN/UVLO</sub> = 0 V, V <sub>OUT</sub> = 0 V (Sourcing)	–5	0	1.2	μA
I <sub>OUT-OFF-SINK</sub>		V <sub>EN/UVLO</sub> = 0 V, V <sub>OUT</sub> = 300 mV (Sinking)	10	15	20	
BFET (BLOCKING FET GATE DRIVER)						
I <sub>BFET</sub>	BFET Charging current <sup>(1)</sup>	V <sub>BFET</sub> = V <sub>OUT</sub>	2			μA
V <sub>BFETmax</sub>	BFET Clamp voltage <sup>(1)</sup>		V <sub>VIN</sub> + 6.4			V
R <sub>BFETdisch</sub>	BFET Discharging resistance to GND	V <sub>EN/UVLO</sub> = 0 V, I <sub>BFET</sub> = 100 mA	15	26	36	Ω
TSD (THERMAL SHUT DOWN)						
T <sub>SHDN</sub>	TSD Threshold, rising <sup>(1)</sup>		150			°C
T <sub>SHDNhyst</sub>	TSD Hysteresis <sup>(1)</sup>		10			°C
	Thermal fault: latched or autoretry	TPS259240	LATCHED			
		TPS259241	AUTO-RETRY			

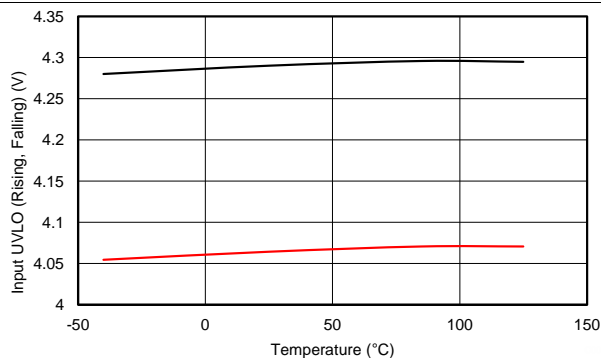
## 7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>ON</sub>	Turn-on delay <sup>(1)</sup>	EN/UVLO → H to I <sub>VIN</sub> = 100 mA, 1-A resistive load at OUT		220		μs
t <sub>OFFdly</sub>	Turn Off delay <sup>(1)</sup>	EN/UVLO↓ to BFET↓, C <sub>BFET</sub> = 0		0.4		μs
dV/dT (OUTPUT RAMP CONTROL)						
t <sub>dVdT</sub>	Output ramp time	EN/UVLO → H to OUT = 11.7 V, C <sub>dVdT</sub> = 0	0.7	1	1.3	ms
		EN/UVLO → H to OUT = 11.7 V, C <sub>dVdT</sub> = 1 nF <sup>(1)</sup>		12		
ILIM (CURRENT LIMIT PROGRAMMING)						
t <sub>FastOffDly</sub>	Fast-Trip comparator delay <sup>(1)</sup>	I <sub>OUT</sub> > I <sub>FASTRIP</sub> to I <sub>OUT</sub> = 0 (Switch Off)		300		ns
BFET (BLOCKING FET GATE DRIVER)						
t <sub>BFET-ON</sub>	BFET Turn-On duration <sup>(1)</sup>	EN/UVLO → H to V <sub>BFET</sub> = 12 V, C <sub>BFET</sub> = 1 nF		4.2		ms
		EN/UVLO → H to V <sub>BFET</sub> = 12 V, C <sub>BFET</sub> = 10 nF		42		
t <sub>BFET-OFF</sub>	BFET Turn-Off duration <sup>(1)</sup>	EN/UVLO → L to V <sub>BFET</sub> = 1 V, C <sub>BFET</sub> = 1 nF		0.4		μs
		EN/UVLO → L to V <sub>BFET</sub> = 1 V, C <sub>BFET</sub> = 10 nF		1.4		
THERMAL SHUTDOWN (TSD)						
t <sub>TSDdly</sub>	Retry delay after TSD recovery, T <sub>J</sub> < [T <sub>SHDN</sub> - 10°C] <sup>(1)</sup>	TPS259241 only		100		μs

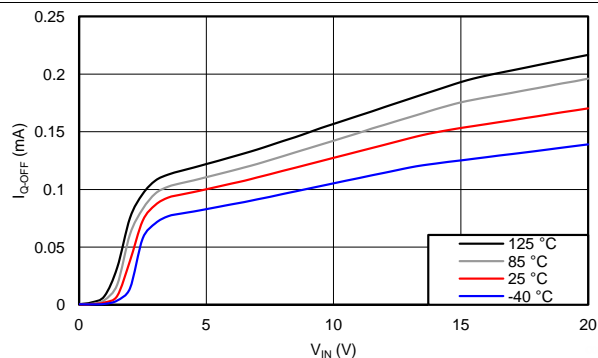
(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

## 7.7 Typical Characteristics

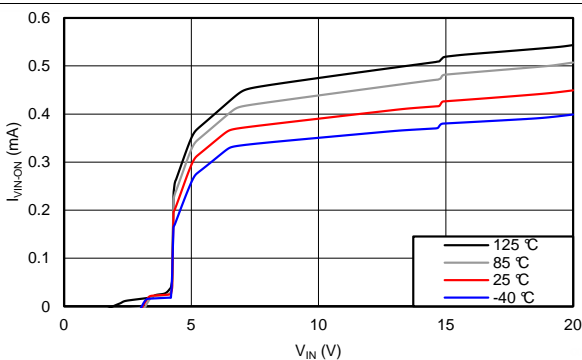
$T_J = 25^\circ\text{C}$ ,  $V_{\text{VIN}} = 12\text{ V}$ ,  $V_{\text{EN/UVLO}} = 2\text{ V}$ ,  $R_{\text{ILIM}} = 100\text{ k}\Omega$ ,  $C_{\text{VIN}} = 0.1\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 1\text{ }\mu\text{F}$ ,  $C_{\text{dVdT}} = \text{OPEN}$  (unless stated otherwise)



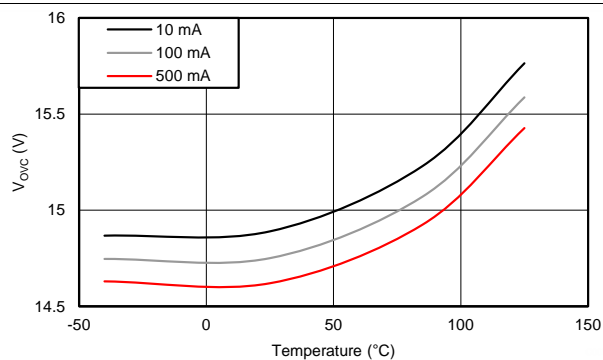
**Figure 1. Input UVLO vs Temperature**



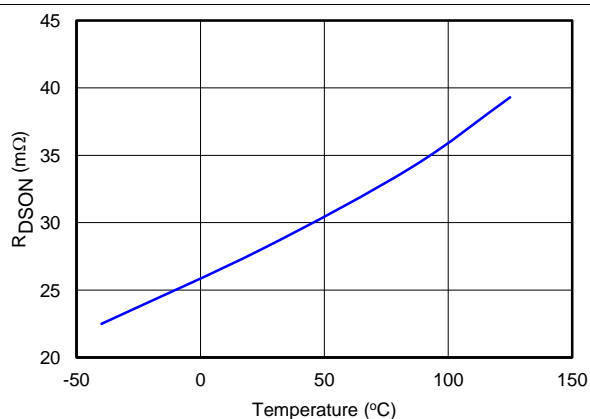
**Figure 2.  $I_{\text{Q-OFF}}$  vs  $V_{\text{IN}}$**



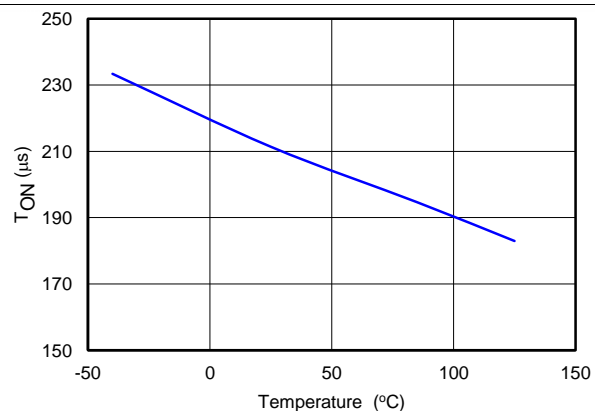
**Figure 3.  $I_{\text{VIN-ON}}$  vs  $V_{\text{IN}}$**



**Figure 4.  $V_{\text{OVC}}$  vs Temperature Across  $I_{\text{OUT}}$**



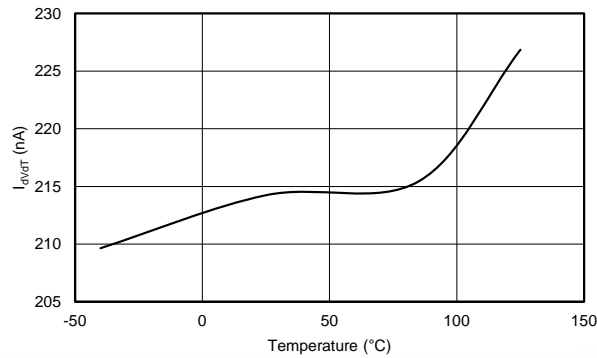
**Figure 5.  $R_{\text{DS(on)}}$  vs Temperature**



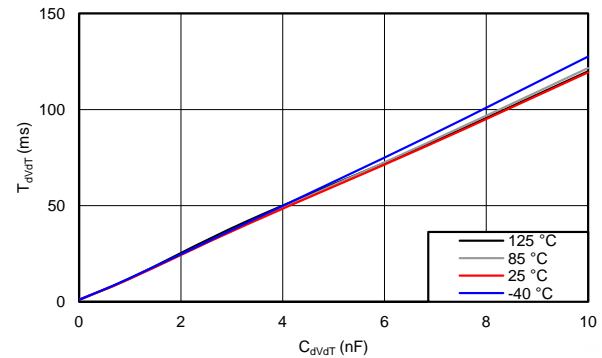
**Figure 6.  $T_{\text{ON}}$  vs Temperature**

## Typical Characteristics (continued)

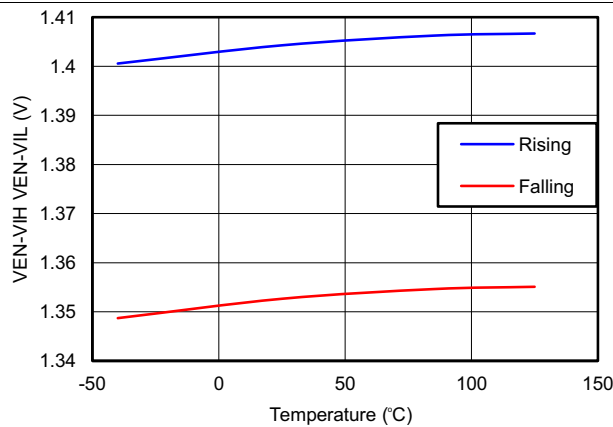
$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$ ,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)



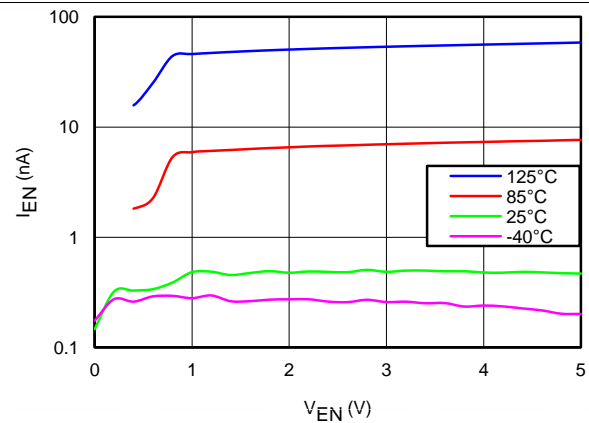
**Figure 7.  $I_{dVdT}$  vs Temperature**



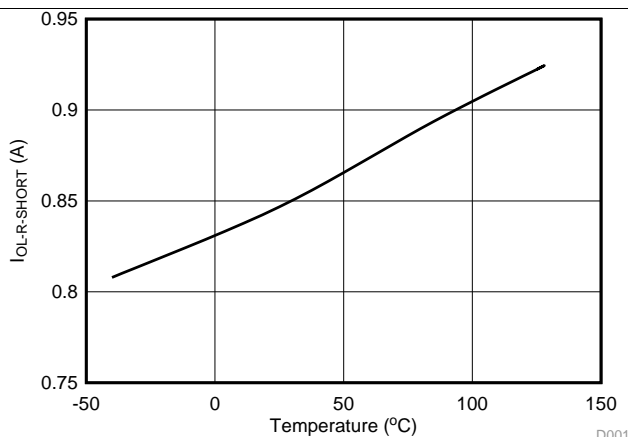
**Figure 8.  $T_{dVdT}$  vs  $C_{dVdT}$**



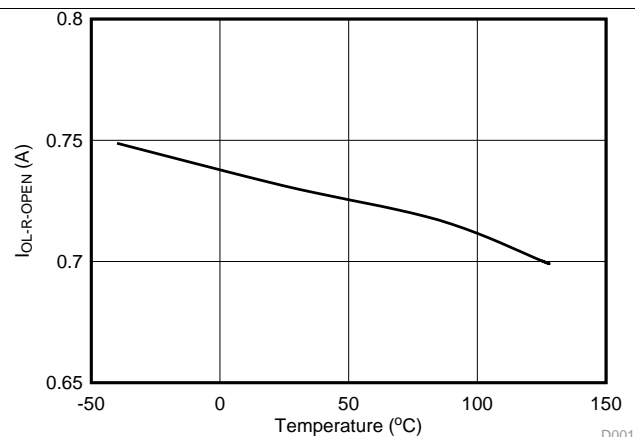
**Figure 9.  $V_{EN-VIH}$ ,  $V_{EN-VIL}$  vs Temperature**



**Figure 10.  $I_{EN}$  (Leakage Current) vs  $V_{EN}$**



**Figure 11.  $I_{OL-R-Short}$  vs Temperature**

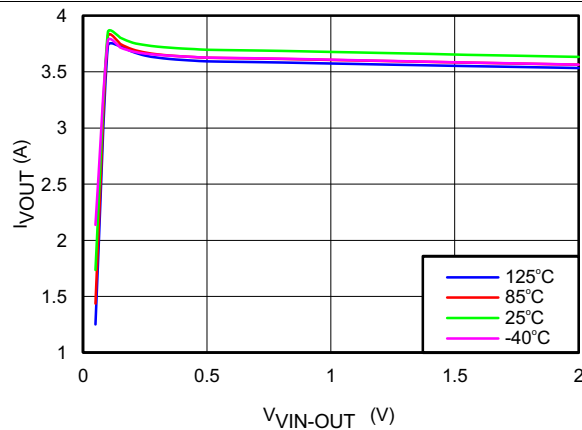


**Figure 12.  $I_{OL-R-Open}$  vs Temperature**



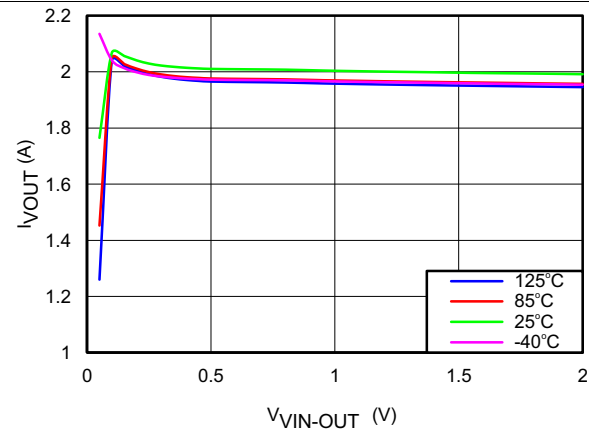
## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{VIN} = 12\text{ V}$ ,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)



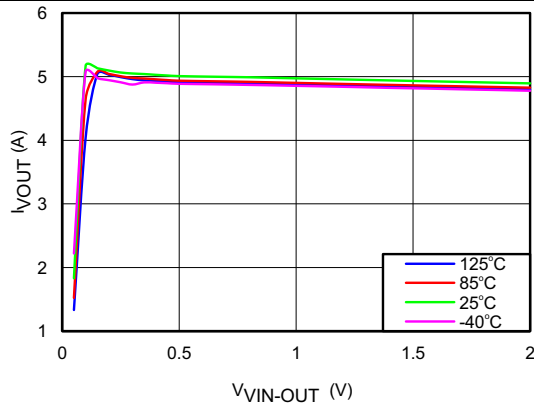
$R_{ILIM} = 100\text{ k}\Omega$

**Figure 13.  $I_{OUT}$  vs  $V_{VIN-OUT}$**



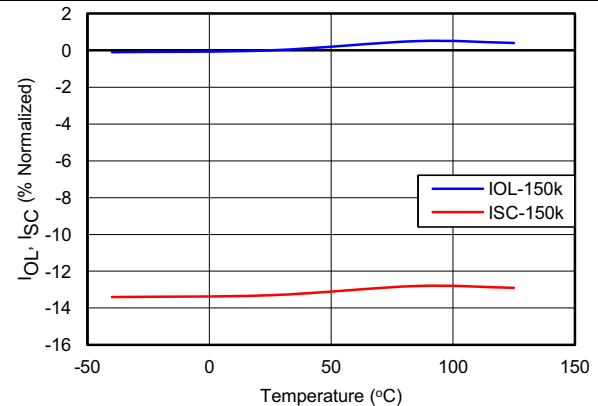
$R_{ILIM} = 45.3\text{ k}\Omega$

**Figure 14.  $I_{OUT}$  vs  $V_{VIN-OUT}$**



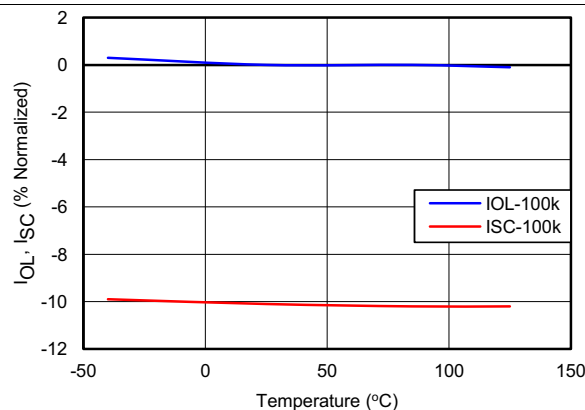
$R_{ILIM} = 150\text{ k}\Omega$

**Figure 15.  $I_{OUT}$  vs  $V_{VIN-OUT}$**



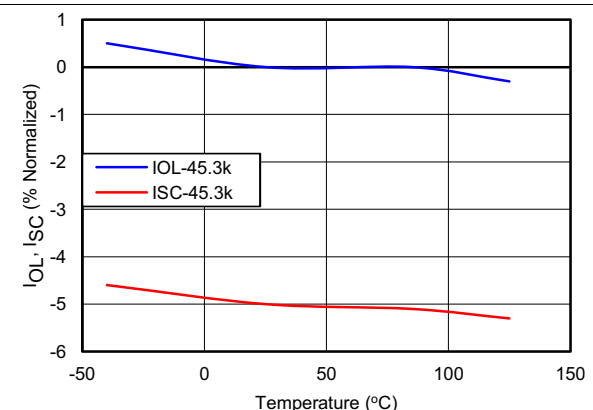
$R_{ILIM} = 150\text{ k}\Omega$

**Figure 16.  $I_{OL}$ ,  $I_{SC}$  vs Temperature**



$R_{ILIM} = 100\text{ k}\Omega$

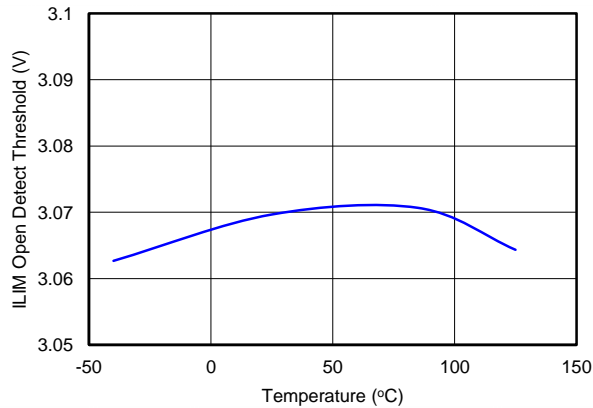
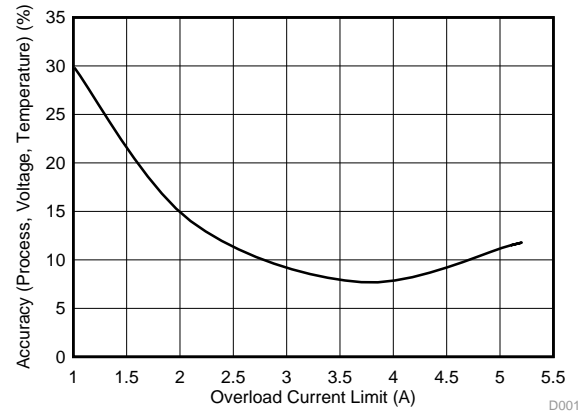
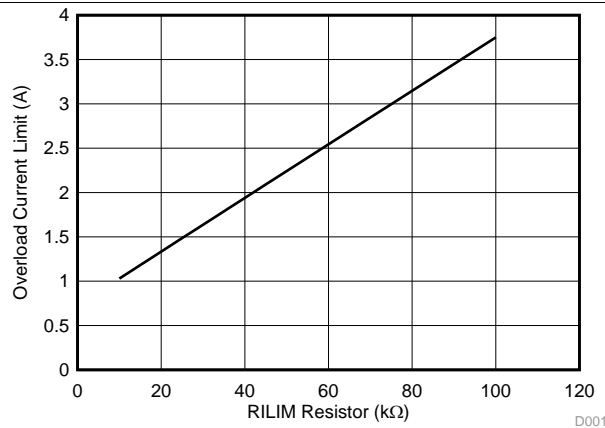
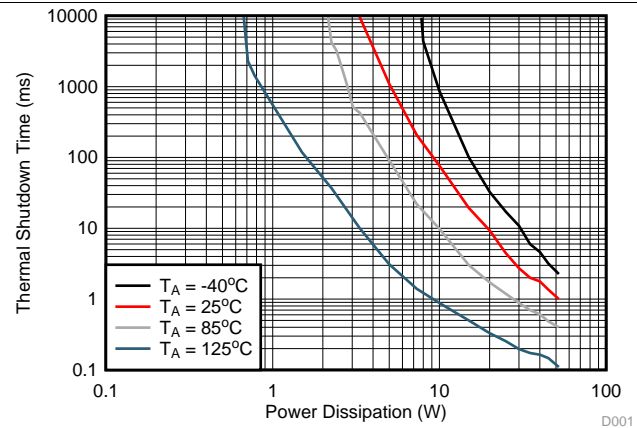
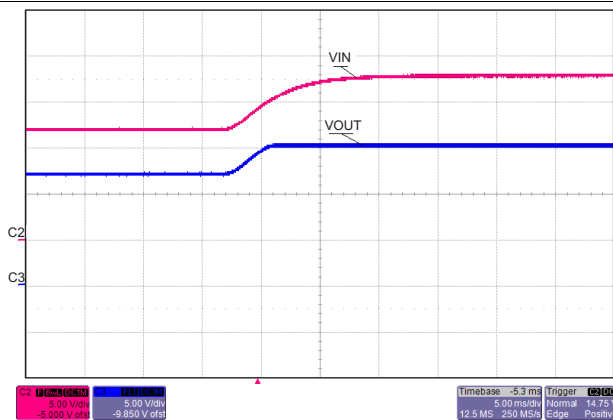
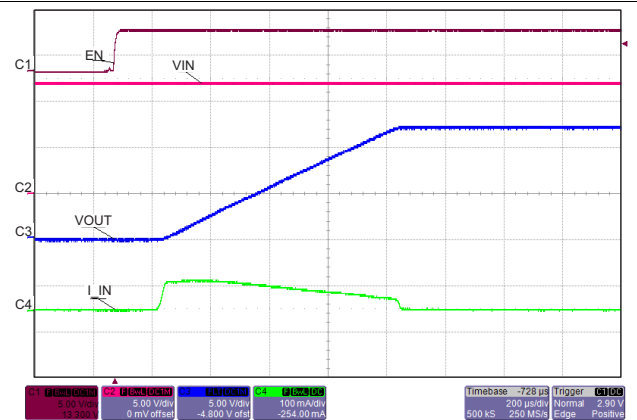
**Figure 17.  $I_{OL}$ ,  $I_{SC}$  vs Temperature**



$R_{ILIM} = 45.3\text{ k}\Omega$

**Figure 18.  $I_{OL}$ ,  $I_{SC}$  vs Temperature**

## Typical Characteristics (continued)

 $T_J = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)

**Figure 19.  $V_{OpenILIM}$  vs Temperature**

**Figure 20. Accuracy vs Overload Current Limit**

**Figure 21. Overload Current Limit vs RILIM Resistor**

**Figure 22. Thermal Shutdown Time vs Power Dissipation**

**Figure 23. Transient: Over-Voltage Clamp**

 $C_{dVdT} = \text{OPEN}$ ,  $C_{OUT} = 4.7\text{ }\mu\text{F}$ 
**Figure 24. Transient: Output Ramp**

## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)

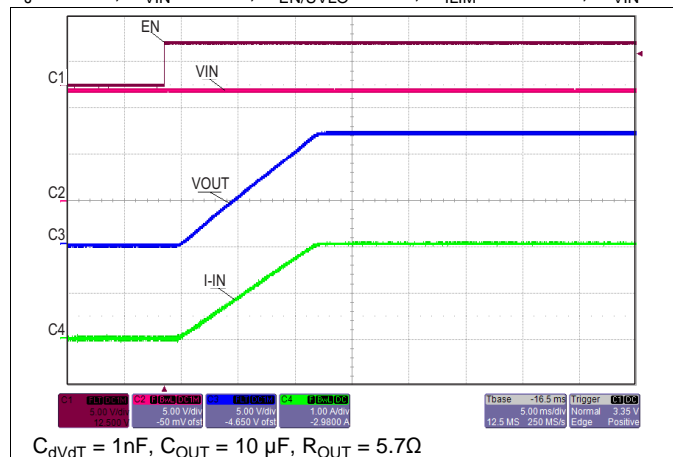


Figure 25. Transient: Output Ramp

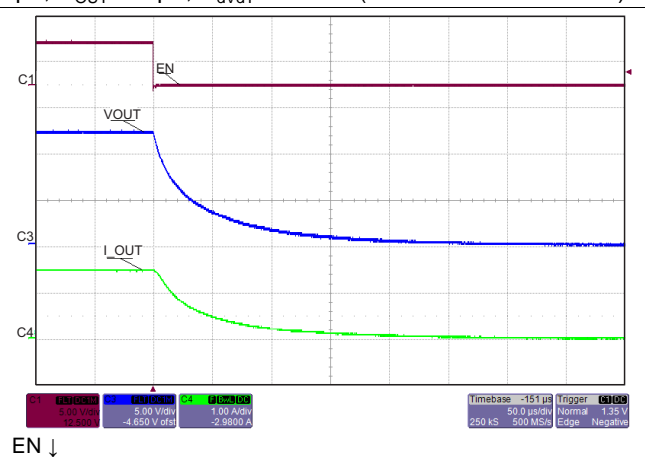


Figure 26. Transient: Turn Off Delay

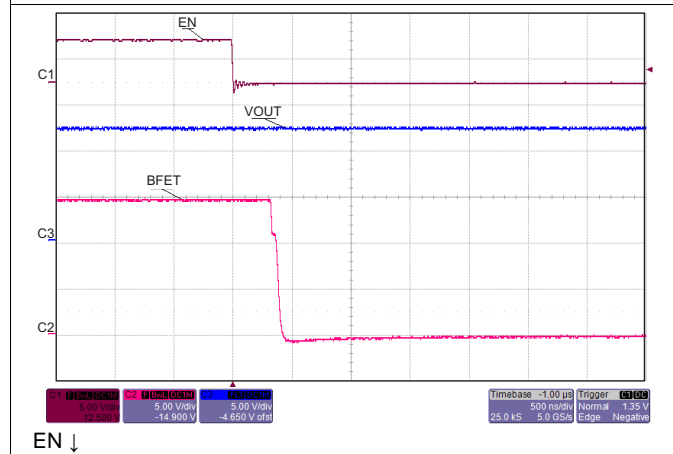


Figure 27. Turn Off Delay to BFET

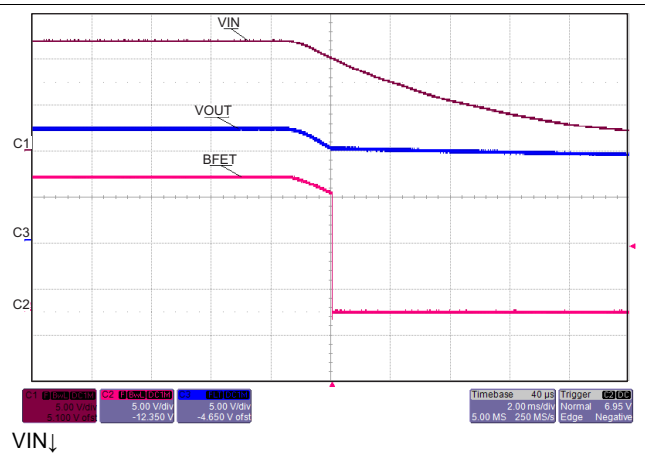


Figure 28. Turn Off Delay to BFET

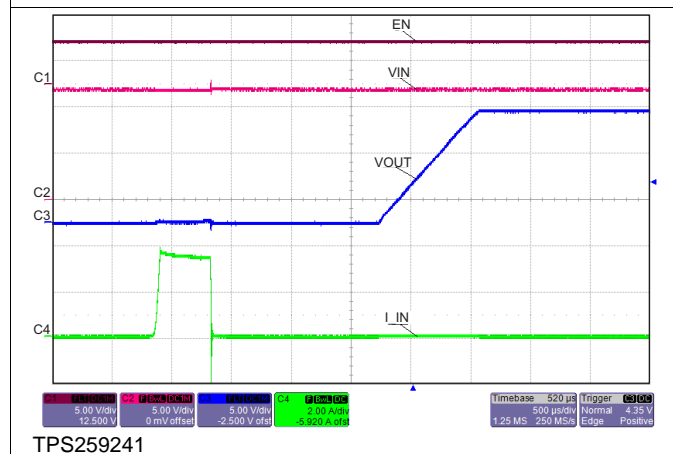


Figure 29. Transient: Recovery From Short Circuit / Over Current

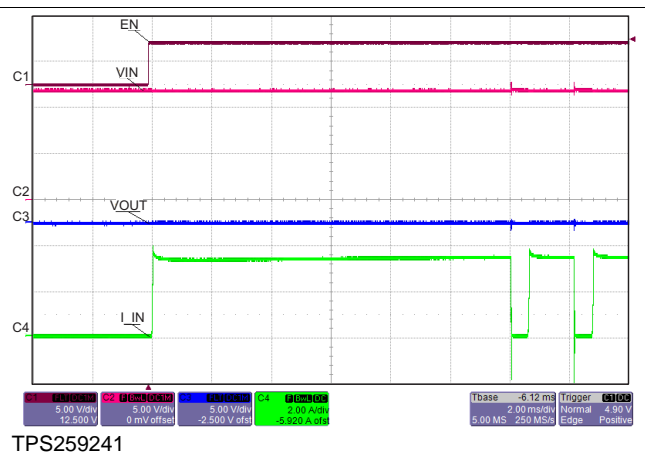


Figure 30. Transient: Wake Up to Short Circuit

# TPS259240, TPS259241

SLVSCU9A – AUGUST 2015 – REVISED AUGUST 2015

www.ti.com

## Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $V_{EN/UVLO} = 2\text{ V}$ ,  $R_{ILIM} = 100\text{ k}\Omega$ ,  $C_{VIN} = 0.1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $C_{dVdT} = \text{OPEN}$  (unless stated otherwise)

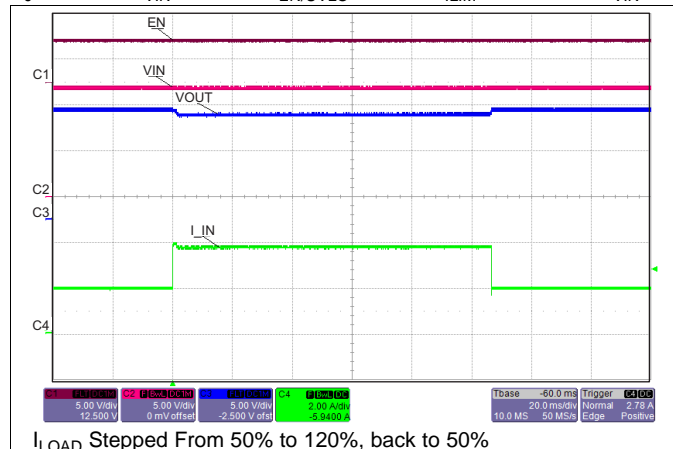


Figure 31. Transient: Overload Current Limit

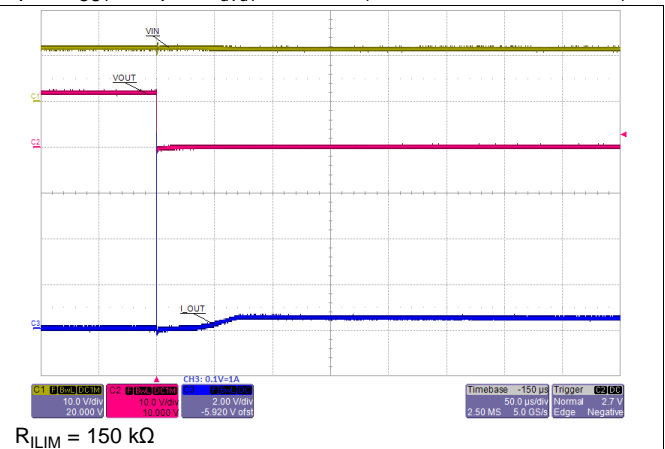


Figure 32. Transient: Output Short Circuit

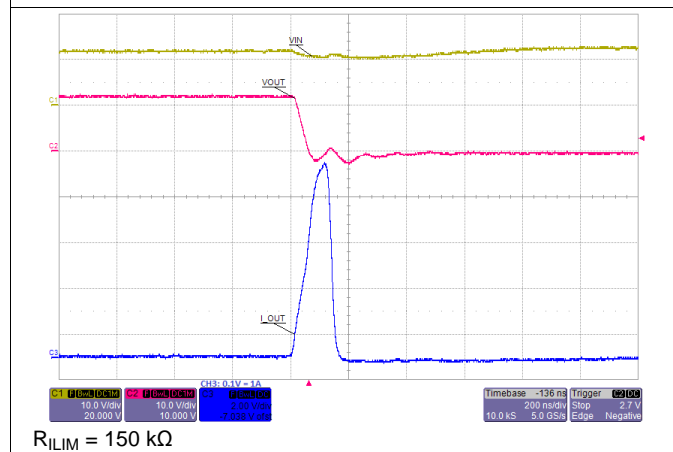


Figure 33. Short Circuit (Zoom): Fast-Trip Comparator

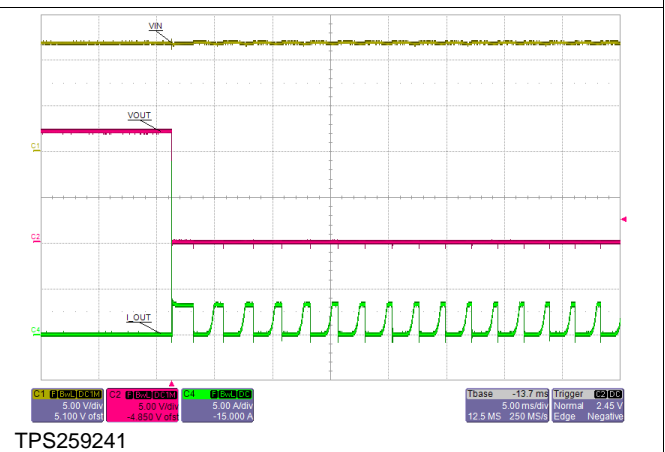


Figure 34. Transient: Thermal Fault Auto-Retry

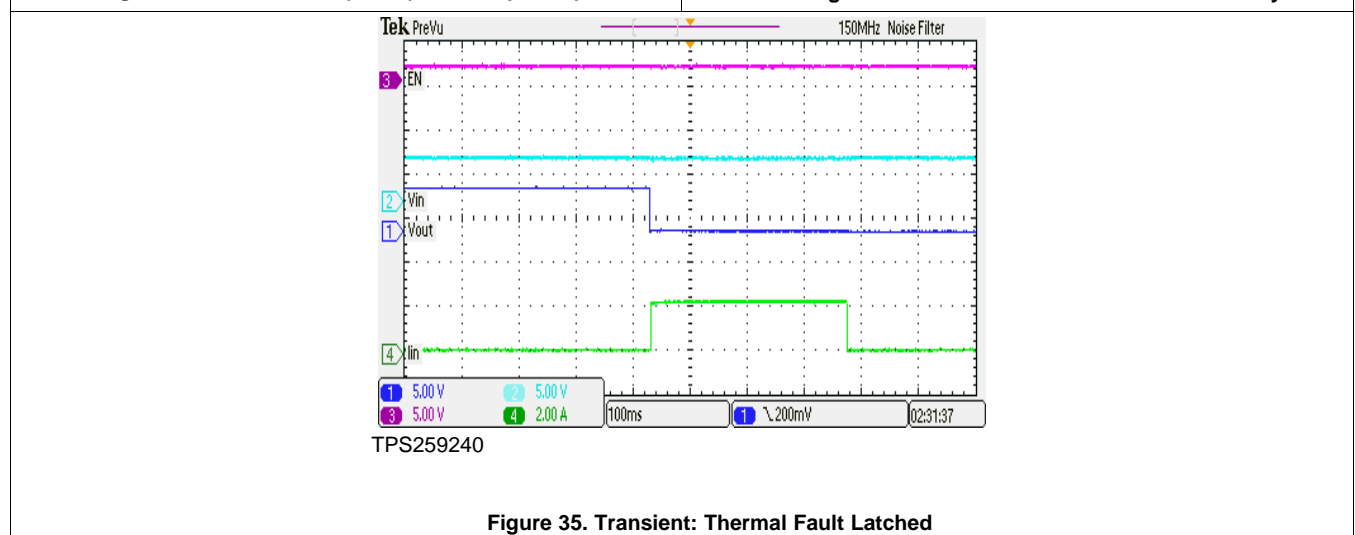


Figure 35. Transient: Thermal Fault Latched

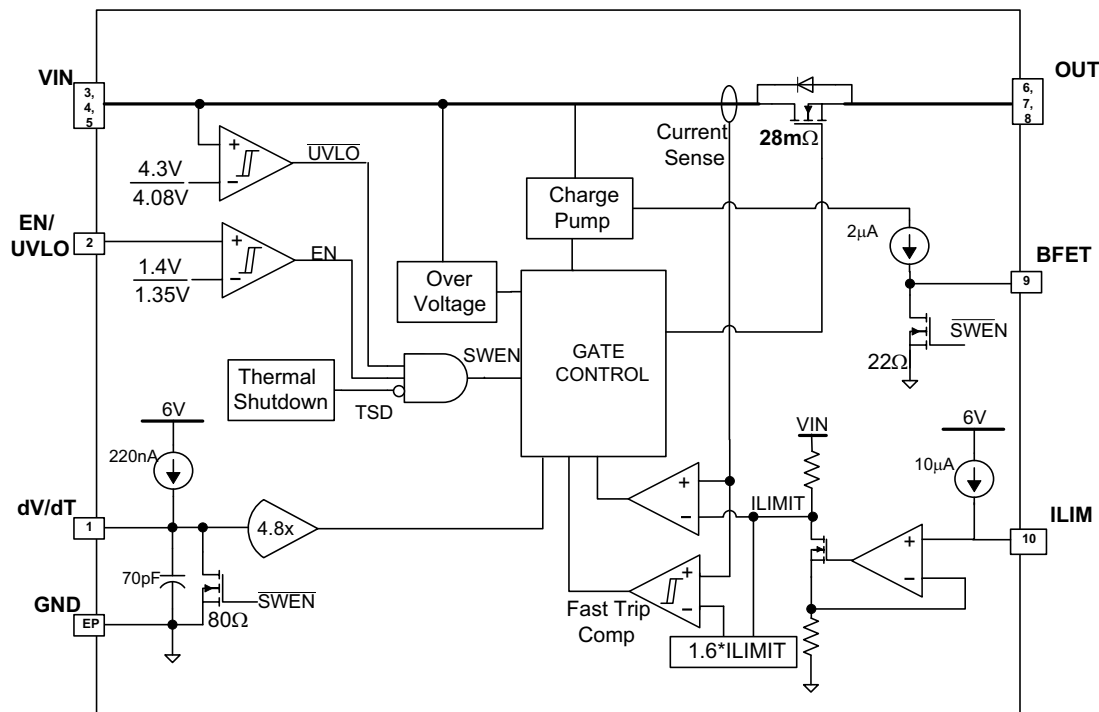
## 8 Detailed Description

### 8.1 Overview

The TPS25924x is an e-fuse with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When VIN exceeds the undervoltage-lockout threshold ( $V_{UVLO}$ ), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET. As VIN rises, the internal MOSFET of the device will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (below  $V_{ENF}$ ), internal MOSFET is turned off. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit  $I_{OL}$  is not exceeded and input voltage spikes are safely clamped to  $V_{OVC}$  level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature ( $T_J$ ) exceeds  $T_{SHDN}$ , typically 150°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In TPS259240, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259241 device will remain off during a cooling period until device temperature falls below  $T_{SHDN} - 10^\circ\text{C}$ , after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 GND

This is the most negative voltage in the circuit and is used as a reference for all voltage measurements unless otherwise specified.

## Feature Description (continued)

### 8.3.2 VIN

Input voltage to the TPS25924x. A ceramic bypass capacitor close to the device from VIN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V to 13.8 V for TPS25924x. The device can continuously sustain a voltage of 20 V on VIN pin. However, above the recommended maximum bus voltage, the device will be in over-voltage protection (OVP) mode, limiting the output voltage to  $V_{OVC}$ . The power dissipation in OVP mode is  $P_{D\_OVP} = (V_{VIN} - V_{OVC}) \times I_{OUT}$ , which can potentially heat up the device and cause thermal shutdown.

### 8.3.3 dV/dT

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate (minimum  $T_{dVdT}$ ) on the output. Equation governing slew rate at start-up is shown below:

$$\frac{dV_{OUT}}{dt} = \frac{I_{dVdT} \times GAIN_{dVdT}}{C_{dVdT} + C_{INT}} \quad (1)$$

Where:

$$I_{dVdT} = 220 \text{ nA (TYP)}$$

$$C_{INT} = 70 \text{ pF (TYP)}$$

$$GAIN_{dVdT} = 4.85$$

$$\frac{dV_{OUT}}{dT} = \text{Desired output slew rate}$$

The total ramp time ( $T_{dVdT}$ ) for 0 to VIN can be calculated using the following equation:

$$T_{dVdT} = 10^6 \times V_{IN} \times (C_{dVdT} + 70 \text{ pF}) \quad (2)$$

For details on how to select an appropriate charging time/rate, refer to the applications section [Setting Output Voltage Ramp Time \( \$T\_{dVdT}\$ \)](#).

### 8.3.4 BFET

Connect this pin to an external NFET that can be used to disconnect input supply from rest of the system in the event of power failure at VIN. The BFET pin is controlled by either input UVLO ( $V_{UVR}$ ) event or EN/UVLO (see [Table 1](#)). BFET can source charging current of 2  $\mu$ A (TYP) and sink (discharge) current from the gate of the external FET via a 26- $\Omega$  internal discharge resistor to initiate fast turn-off, typically <1  $\mu$ s. Due to 2  $\mu$ A charging current, it is recommended to use >10 M $\Omega$  impedance when probing the BFET node.

**Table 1. BFET**

EN/UVLO > $V_{ENR}$	VIN > $V_{UVR}$	BFET MODE
H	H	Charge
X	L	Discharge
L	X	Discharge

### 8.3.5 EN/UVLO

As an input pin, it controls both the ON/OFF state of the internal MOSFET and that of the external blocking FET. In its high state, the internal MOSFET is enabled and charging begins for the gate of external FET. A low on this pin will turn off the internal MOSFET and pull the gate of the external FET to GND via the built-in discharge resistor. High and Low levels are specified in the parametric table of the datasheet. The EN/UVLO pin is also used to clear a thermal shutdown latch in the TPS259240 by toggling this pin (H→L).

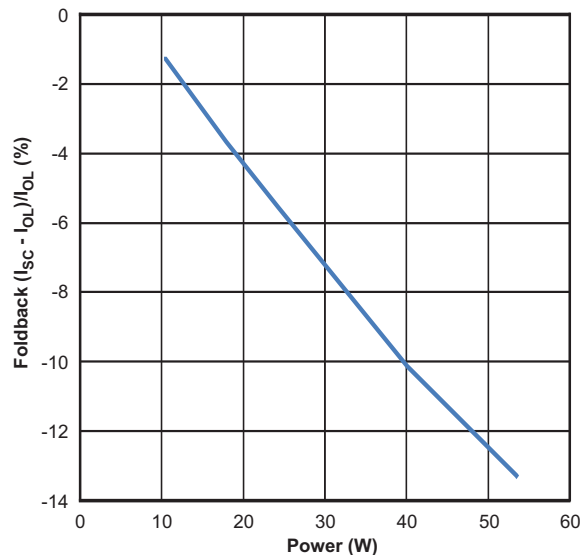
The internal de-glitch delay on EN/UVLO falling edge is intentionally kept low (1  $\mu$ s typical) for quick detection of power failure. When used with a resistor divider from supply to EN/UVLO to GND, power-fail detection on EN/UVLO helps in quick turn-off of the BFET driver, thereby stopping the flow of reverse current (see typical application diagram, [Figure 43](#)). For applications where a higher de-glitch delay on EN/UVLO is desired, or when the supply is particularly noisy, it is recommended to use an external bypass capacitor from EN/UVLO to GND.

### 8.3.6 ILIM

The device continuously monitors the load current and keeps it limited to the value programmed by  $R_{ILIM}$ . After start-up event and during normal operation, current limit is set to  $I_{OL}$  (over-load current limit).

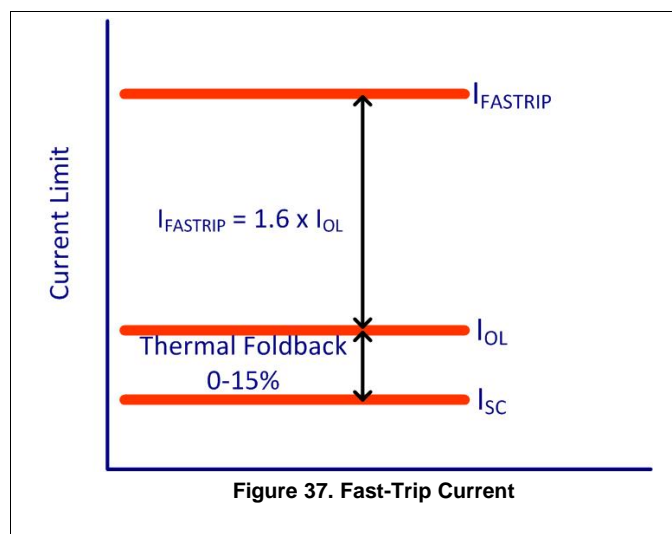
$$I_{OL} = (0.7 + 3 \times 10^{-5} \times R_{ILIM}) \quad (3)$$

When power dissipation in the internal MOSFET [ $P_D = (V_{VIN} - V_{OUT}) \times I_{OUT}$ ] exceeds 10 W, there is a 2% – 12% thermal foldback in the current limit value so that  $I_{OL}$  drops to  $I_{SC}$ . In each of the two modes, MOSFET gate voltage is regulated to throttle short-circuit and overload current flowing to the load. Eventually, the device shuts down due to over temperature.

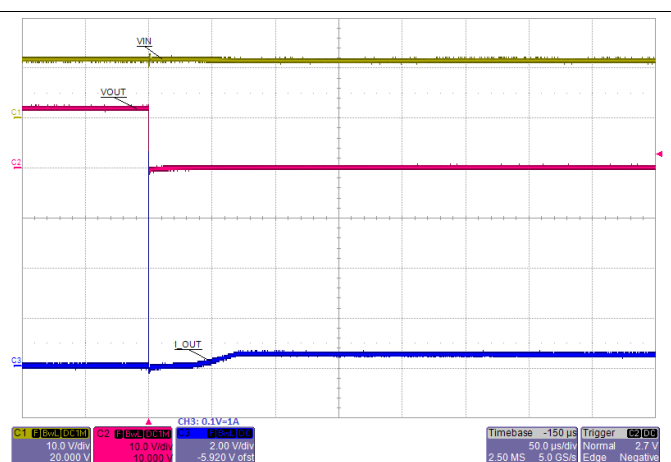


**Figure 36. Thermal Foldback in Current Limit**

During a transient short circuit event, the current through the device increases very rapidly. The current-limit amplifier cannot respond very quickly to this event due to its limited bandwidth. Therefore, the TPS25924x incorporates a fast-trip comparator, which shuts down the pass device very quickly when  $I_{OUT} > I_{FASTrip}$ , and terminates the rapid short-circuit peak current. The trip threshold is set to 60% higher than the programmed over-load current limit ( $I_{FASTrip} = 1.6 \times I_{OL}$ ). After the transient short-circuit peak current has been terminated by the fast-trip comparator, the current limit amplifier smoothly regulates the output current to  $I_{OL}$  (see figure below).



**Figure 37. Fast-Trip Current**



**Figure 38. Fast-Trip and Current Limit Amplifier Response for Short Circuit**

## 8.4 Device Functional Modes

The TPS25924x is a hot-swap controller with integrated power switch that is used to manage current/voltage/start-up voltage ramp to a connected load. The device starts its operation by monitoring the VIN bus. When  $V_{VIN}$  exceeds the undervoltage-lockout threshold ( $V_{UVL}$ ), the device samples the EN/UVLO pin. A high level on this pin enables the internal MOSFET and also start charging the gate of external blocking FET (if connected) via the BFET pin. As VIN rises, the internal MOSFET of the device and external FET (if connected) will start conducting and allow current to flow from VIN to OUT. When EN/UVLO is held low (that is, below  $V_{ENF}$ ), the internal MOSFET is turned off and BFET pin is discharged, thereby, blocking the flow of current from VIN to OUT. User also has the ability to modify the output voltage ramp time by connecting a capacitor between dV/dT pin and GND.

Having successfully completed its start-up sequence, the device now actively monitors its load current and input voltage, ensuring that the adjustable overload current limit  $I_{OL}$  is not exceeded and input voltage spikes are safely clamped to  $V_{OVC}$  level at the output. This keeps the output device safe from harmful voltage and current transients. The device also has built-in thermal sensor. In the event device temperature ( $T_J$ ) exceeds  $T_{SHDN}$ , typically 150°C, the thermal shutdown circuitry will shut down the internal MOSFET thereby disconnecting the load from the supply. In the TPS259240, the output will remain disconnected (MOSFET open) until power to device is recycled or EN/UVLO is toggled (pulled low and then high). The TPS259241 device will remain off during a cooling period until device temperature falls below  $T_{SHDN} - 10^\circ\text{C}$ , after which it will attempt to restart. This ON and OFF cycle will continue until fault is cleared.



## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

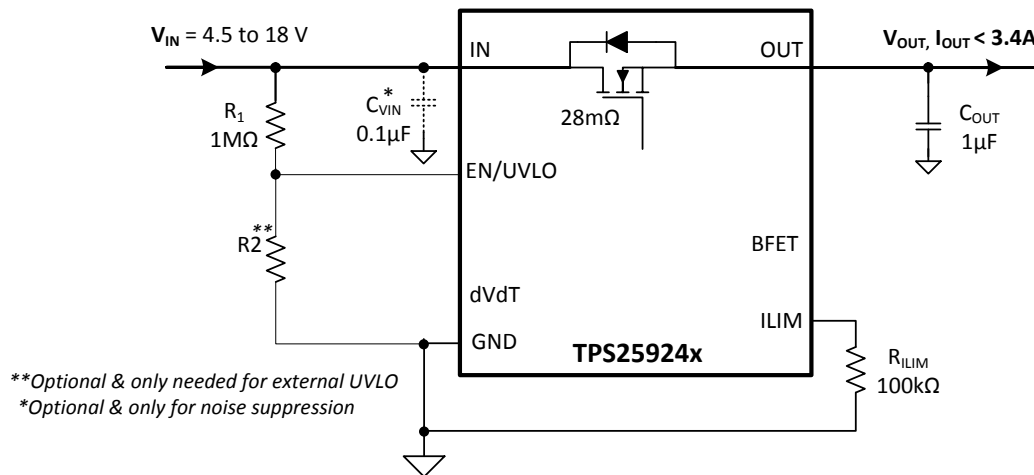
### 9.1 Application Information

The TPS25924x is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

The following design procedure can be used to select component values for the device. Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS2592xx Design Calculator* (SLUC570) is available on web folder. This section presents a simplified discussion of the design process.

### 9.2 Typical Applications

#### 9.2.1 Simple 3.7-A eFuse Protection for Set Top Boxes



**Figure 39. Typical Application Schematic: Simple 3.7-A e-Fuse for STBs**

#### 9.2.1.1 Design Requirements

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, $V_{IN}$	12 V
Undervoltage lockout set point, $V_{(UV)}$	Default: $V_{UVR} = 4.3$ V
Overvoltage protection set point, $V_{(OV)}$	Default: $V_{OVC} = 15$ V
Load at start-up, $R_{L(SU)}$	4 $\Omega$
Current limit, $I_{OL} = I_{ILIM}$	3.7 A
Load capacitance, $C_{OUT}$	1 $\mu$ F
Maximum ambient temperature, $T_A$	85°C

### 9.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25924x.

#### 9.2.1.2.1 Step by Step Design Procedure

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

#### 9.2.1.2.2 Programming the Current-Limit Threshold: $R_{ILIM}$ Selection

The  $R_{ILIM}$  resistor at the ILIM pin sets the over load current limit, this can be set using [Equation 4](#).

$$R_{ILIM} = \frac{I_{ILIM} - 0.7}{3 \times 10^{-5}} \quad (4)$$

For  $I_{OL} = I_{ILIM} = 3.7$  A, from [Equation 4](#),  $R_{ILIM} = 100$  k $\Omega$ , choose closest standard value resistor with 1% tolerance.

#### 9.2.1.2.3 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of  $R_1$  and  $R_2$  as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving [Equation 5](#).

$$V_{(UV)} = \frac{R_1 + R_2}{R_2} \times V_{ENR} \quad (5)$$

Where  $V_{ENR} = 1.4$  V is enable voltage rising threshold.

Since  $R_1$  and  $R_2$  will leak the current from input supply ( $V_{IN}$ ), these resistors should be selected based on the acceptable leakage current from input power supply ( $V_{IN}$ ). The current drawn by  $R_1$  and  $R_2$  from the power supply  $\{I_{R12} = V_{IN}/(R_1 + R_2)\}$ .

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current,  $I_{R12}$  must be chosen to be 20x greater than the leakage current expected.

For default UVLO of  $V_{UVR} = 4.3$  V, select  $R_2 = \text{OPEN}$ , and  $R_1 = 1$  M $\Omega$ . Since EN/UVLO pin is rated only to 7 V, it cannot be connected directly to  $V_{IN} = 12$  V. It has to be connected through  $R_1 = 1$  M $\Omega$  only, so that the pull-up current for EN/UVLO pin is limited to  $< 20$   $\mu$ A.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold,  $V_{UVR}$ . This is calculated using [Equation 6](#).

$$V_{(PFAIL)} = 0.96 \times V_{UVR} \quad (6)$$

Where  $V_{UVR}$  is 4.3 V, Power fail threshold set is 4.1 V.

#### 9.2.1.2.4 Setting Output Voltage Ramp Time ( $T_{dVdT}$ )

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor  $C_{dVdT}$  needed is calculated considering the two possible cases:

##### 9.2.1.2.4.1 Case 1: Start-Up without Load: Only Output Capacitance $C_{OUT}$ Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference as well as the power dissipated across the internal FET decreases. The average power dissipated in the device during start-up is calculated using [Equation 8](#).

For TPS25924x, the inrush current is determined as:

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{T_{dVdT}} \quad (7)$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (8)$$

Equation 8 assumes that load does not draw any current until the output voltage has reached its final value.

#### 9.2.1.2.4.2 Case 2: Start-Up with Load: Output Capacitance $C_{OUT}$ and Load Draws Current During Start-Up

When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load during start-up ( $R_{L(SU)}$ ), load current ramps up proportionally with increase in output voltage during  $T_{dVdT}$  time. The average power dissipation in the internal FET during charging time due to resistive load is given by:

$$P_{D(LOAD)} = \left( \frac{1}{6} \right) \times \frac{V_{(IN)}^2}{R_{L(SU)}} \quad (9)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (10)$$

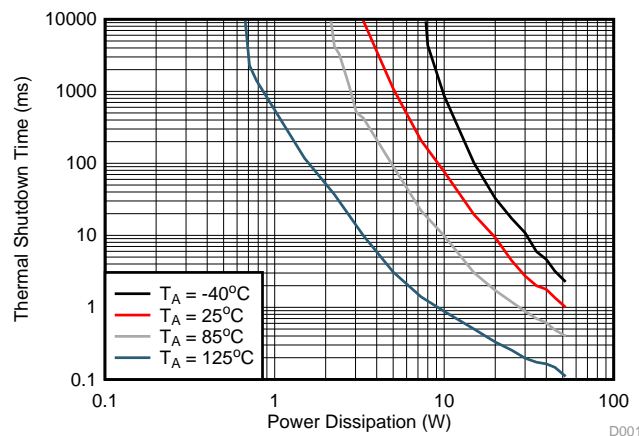
Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (11)$$

If  $I_{(STARTUP)} > I_{OL}$ , the device limits the current to  $I_{OL}$  and the current limited charging time is determined by:

$$T_{dVdT(Current-Limited)} = C_{OUT} \times R_{L(SU)} \times \left[ \frac{I_{OL}}{I_{(INRUSH)}} - 1 + \ln \left( \frac{I_{(INRUSH)}}{I_{OL} - \frac{V_{(IN)}}{R_{L(SU)}}} \right) \right] \quad (12)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in Figure 40.



**Figure 40. Thermal Shutdown Limit Plot**

For the design example under discussion, select ramp-up capacitor  $C_{dVdT} = \text{OPEN}$ . Then, using Equation 2.

$$T_{dVdT} = 10^6 \times 12 \times (0 + 70 \text{ pF}) = 840 \text{ } \mu\text{s} \quad (13)$$

The inrush current drawn by the load capacitance ( $C_{OUT}$ ) during ramp-up using Equation 7.

$$I_{(INRUSH)} = 1 \text{ } \mu\text{F} \times \frac{12}{840 \text{ } \mu\text{s}} = 15 \text{ mA} \quad (14)$$

The inrush Power dissipation is calculated, using Equation 8.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 15 \text{ m} = 90 \text{ mW} \quad (15)$$

For 90 mW of power loss, the thermal shut down time of the device should not be less than the ramp-up time  $T_{dV/dT}$  to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph [Figure 40](#) at  $T_A = 85^\circ\text{C}$ , for 90 mW of power, the shutdown time is infinite. So it is safe to use 0.79 ms as start-up time without any load on output.

Considering the start-up with load  $4\ \Omega$ , the additional power dissipation, when load is present during start up is calculated, using [Equation 9](#).

$$P_{D(\text{LOAD})} = \frac{12 \times 12}{6 \times 4} = 6\ \text{W} \quad (16)$$

The total device power dissipation during start up, using [Equation 10](#) is:

$$P_{D(\text{STARTUP})} = 6 + 90\ \text{m} = 6.09\ \text{W} \quad (17)$$

From thermal shutdown limit graph at  $T_A = 85^\circ\text{C}$ , the thermal shutdown time for 6.09 W is more than 10 ms. So it is well within acceptable limits to not use an external capacitor ( $C_{dV/dT}$ ) with start-up load of  $4\ \Omega$ .

If, due to large  $C_{OUT}$ , there is a need to decrease the power loss during start-up, it can be done with increase of  $C_{dV/dT}$  capacitor.

### 9.2.1.2.5 Support Component Selection - $C_{VIN}$

$C_{VIN}$  is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001  $\mu\text{F}$  to 0.1  $\mu\text{F}$  is recommended for  $C_{VIN}$ .

### 9.2.1.3 Application Curves

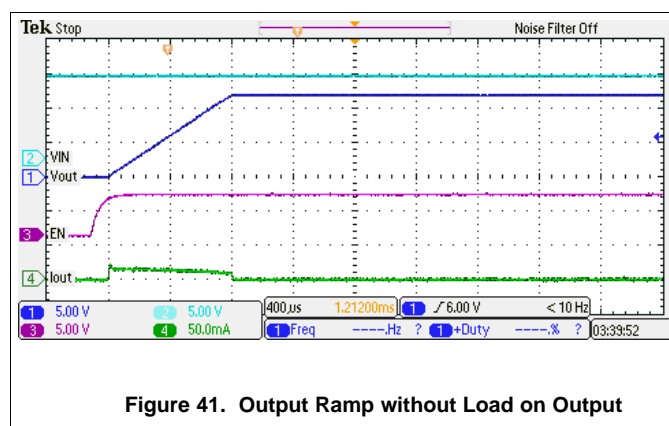


Figure 41. Output Ramp without Load on Output

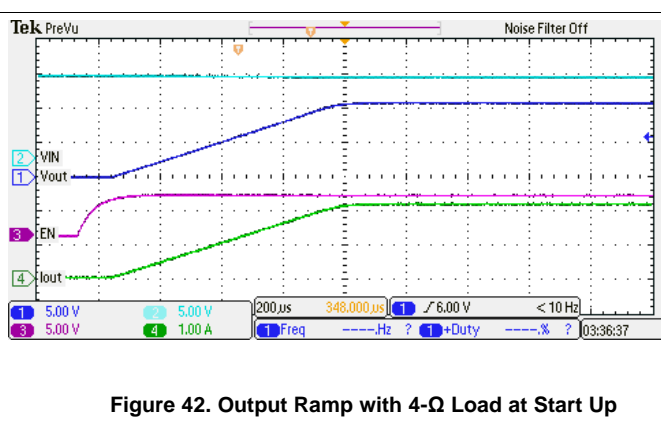


Figure 42. Output Ramp with 4- $\Omega$  Load at Start Up

## 9.2.2 Inrush and Reverse Current Protection for Hold-Up Capacitor Application (for example, SSD)

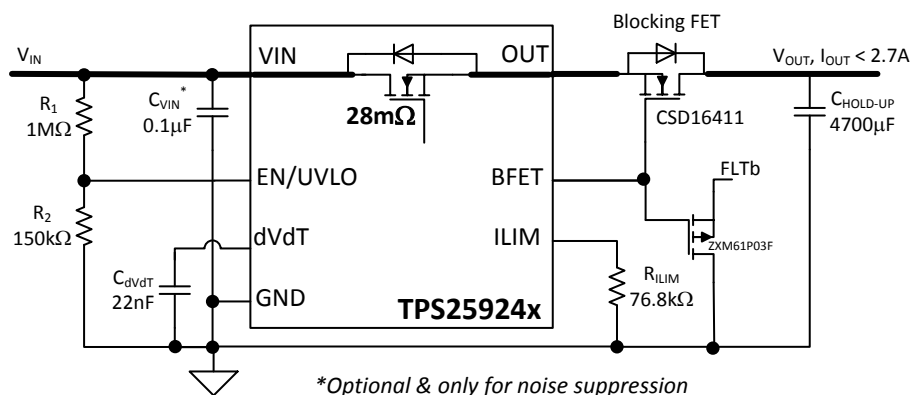


Figure 43. Inrush and Reverse Current Protection for Hold-Up Capacitor Application (for example, SSD) (TPS25924x UVLO is used as power fail comparator)

### 9.2.2.1 Design Requirements

**Table 3. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, $V_{IN}$	12 V
Undervoltage lockout set point, $V_{(UV)}$	10.8 V
Overvoltage protection set point, $V_{(OV)}$	Default: $V_{(OV)} = 15$ V
Load at start-up, $R_{L(SU)}$	1000 $\Omega$
Current limit, $I_{OL} = I_{ILIM}$	3 A
Load capacitance, $C_{OUT}$	4700 $\mu$ F
Maximum ambient temperature, $T_A$	85°C

### 9.2.2.2 Detailed Design Procedure

#### 9.2.2.2.1 Programming the Current-Limit Threshold: $R_{ILIM}$ Selection

The  $R_{ILIM}$  resistor at the ILIM pin sets the over load current limit, this can be set using [Equation 4](#).

For  $I_{OL} = I_{ILIM} = 3$  A, from [Equation 4](#),  $R_{ILIM} = 76.8$  k $\Omega$ . Choose closest standard value resistor with 1% tolerance.

#### 9.2.2.2.2 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) trip point is adjusted using the external voltage divider network of  $R_1$  and  $R_2$  as connected between IN, EN/UVLO and GND pins of the device. The values required for setting the undervoltage are calculated solving [Equation 5](#).

For UVLO of  $V_{(UV)} = 10.8$  V, select  $R_2 = 150$  k $\Omega$ , and  $R_1 = 1$  M $\Omega$ .

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold,  $V_{(UV)}$ . This is calculated using [Equation 6](#).

Where  $V_{(UV)} = 10.73$  V, Power fail threshold set is  $V_{(PFail)} = 10.35$  V.

#### 9.2.2.2.3 Setting Output Voltage Ramp Time ( $T_{dVdT}$ )

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

For the design example under discussion, select ramp-up capacitor  $C_{dVdT} = 22$  nF. Then, using [Equation 2](#).

$$T_{dVdT} = 10^6 \times 12 \times (22 \text{ nF} + 70 \text{ pF}) = 265 \text{ ms} \quad (18)$$

The inrush current drawn by the load capacitance ( $C_{OUT}$ ) during ramp-up using [Equation 7](#).

$$I_{(INRUSH)} = 4700 \mu\text{F} \times \frac{12}{265 \text{ ms}} = 213 \text{ mA} \quad (19)$$

The inrush Power dissipation is calculated, using [Equation 8](#).

$$P_{D(INRUSH)} = 0.5 \times 12 \times 213 \text{ m} = 1278 \text{ mW} \quad (20)$$

Considering the start-up with load 1000  $\Omega$ , the additional power dissipation, when load is present during start up is calculated, using [Equation 9](#).

$$P_{D(LOAD)} = \frac{12 \times 12}{6 \times 1000} = 24 \text{ mW} \quad (21)$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = 1278 + 24 = 1302 \text{ mW} \quad (22)$$

From thermal shutdown limit graph at  $T_A = 85^\circ\text{C}$ , the thermal shutdown time for 1.3 W is more than 300 ms. So the device will start safely.

## TPS259240, TPS259241

SLVSCU9A–AUGUST 2015–REVISED AUGUST 2015

www.ti.com

If  $C_{dVdT} = 4.7 \text{ nF}$  was used, the device would have tried to charge the  $4700\text{-}\mu\text{F}$  output cap with inrush current of  $986 \text{ mA}$  in  $57.24 \text{ ms}$ , dissipating power of  $5.94 \text{ W}$ . This is outside the safe starting condition of the device, and would have led the device to enter thermal shutdown during start-up.

### 9.2.2.3 Application Curves

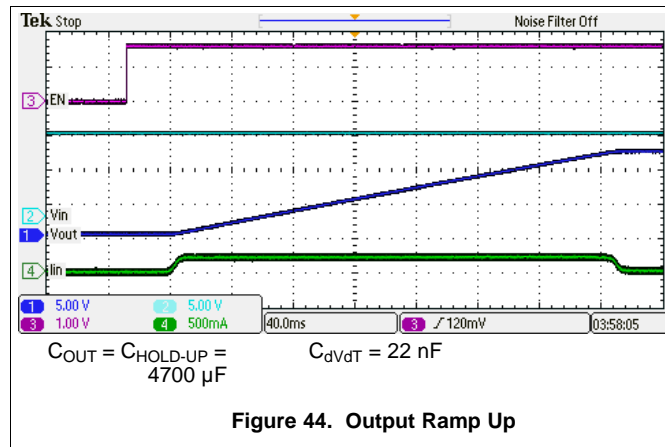


Figure 44. Output Ramp Up

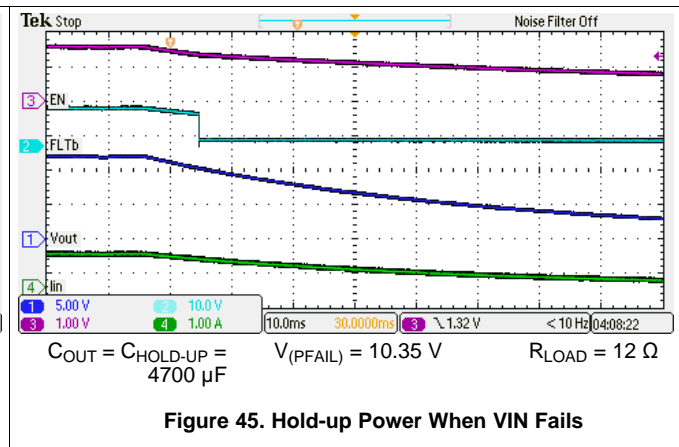


Figure 45. Hold-up Power When VIN Fails

## 10 Power Supply Recommendations

The device is designed for supply voltage range of  $4.5\text{ V} \leq V_{\text{IN}} \leq 18\text{ V}$ . If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than  $0.1\text{ }\mu\text{F}$  is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

### 10.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ( $C_{\text{IN}} = 0.001\text{ }\mu\text{F}$  to  $0.1\text{ }\mu\text{F}$ ) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with [Equation 23](#).

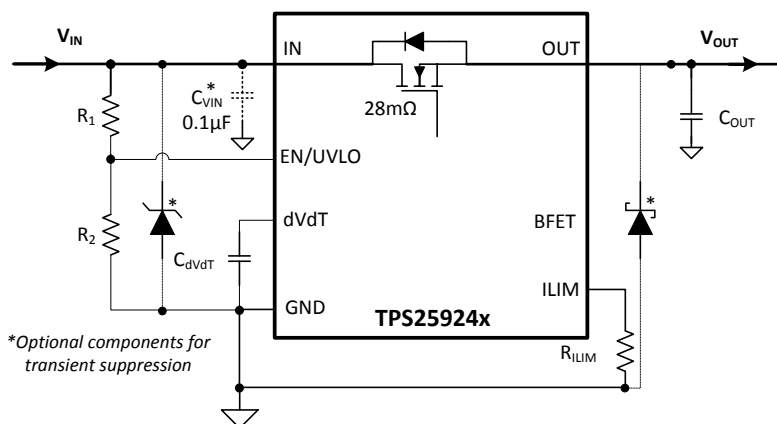
$$V_{\text{SPIKE(Absolute)}} = V_{\text{(IN)}} + I_{\text{(LOAD)}} \times \sqrt{\frac{L_{\text{(IN)}}}{C_{\text{(IN)}}}} \quad (23)$$

Where:

- $V_{\text{(IN)}}$  is the nominal supply voltage
- $I_{\text{(LOAD)}}$  is the load current
- $L_{\text{(IN)}}$  equals the effective inductance seen looking into the source
- $C_{\text{(IN)}}$  is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in [Figure 46](#).



**Figure 46. Circuit Implementation with Optional Protection Components**

### 10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.





## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

*TPS2592xx Design Calculator* ([SLUC570](#))

### 12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 4. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS259241	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
TPS259240	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.

WEBENCH is a registered trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259240DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	259240	<a href="#">Samples</a>
TPS259240DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	259240	<a href="#">Samples</a>
TPS259241DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	259241	<a href="#">Samples</a>
TPS259241DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	259241	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

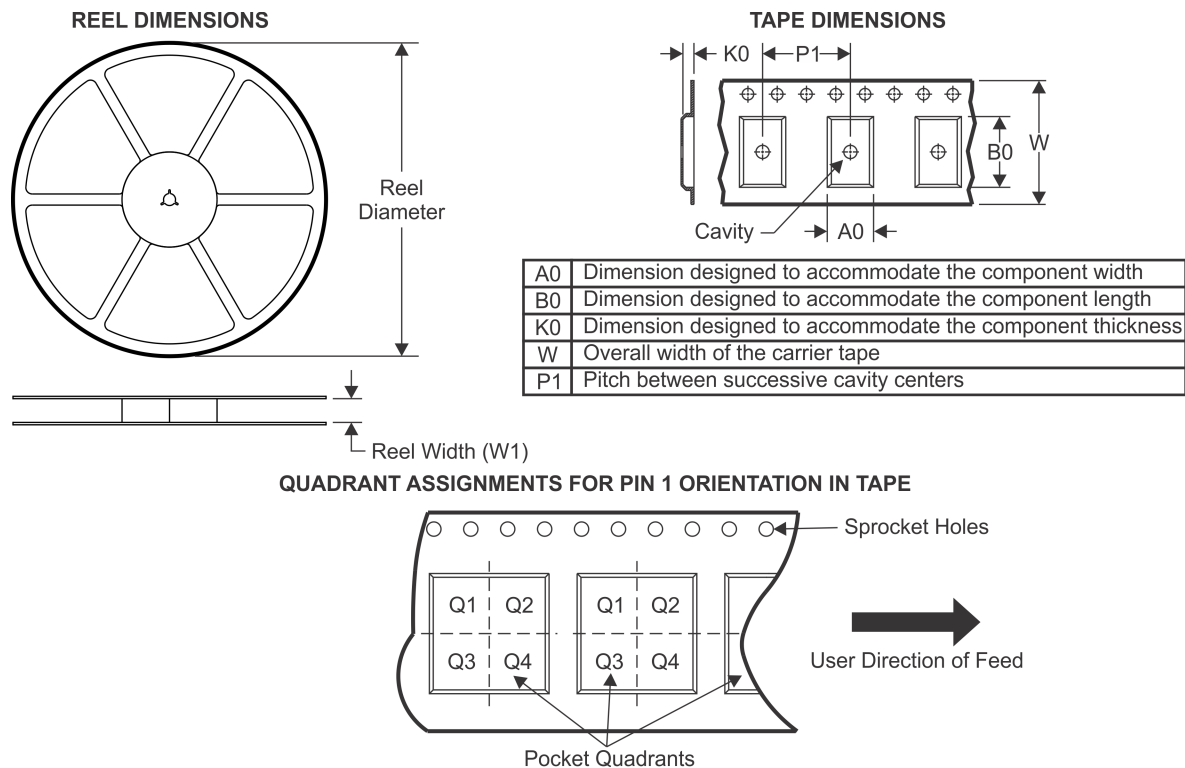
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

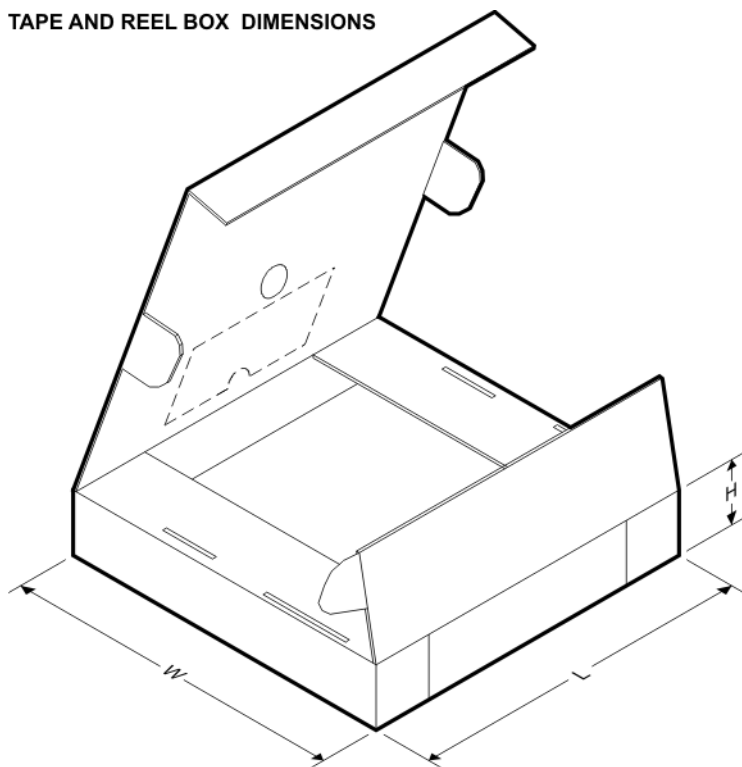
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259240DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259240DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS259241DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

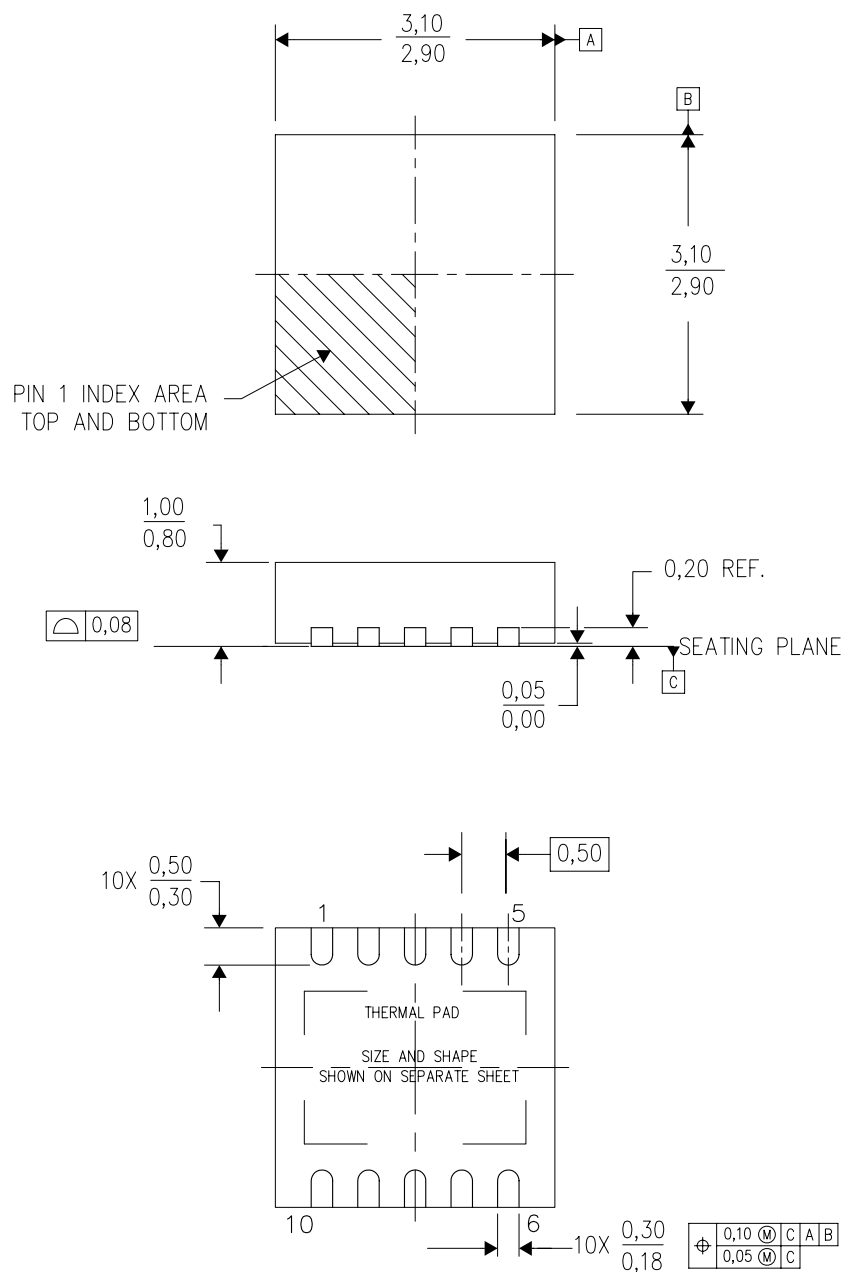


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259240DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS259240DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS259241DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS259241DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



4204102-3/L 09/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present.

DRC (S-PVSON-N10)

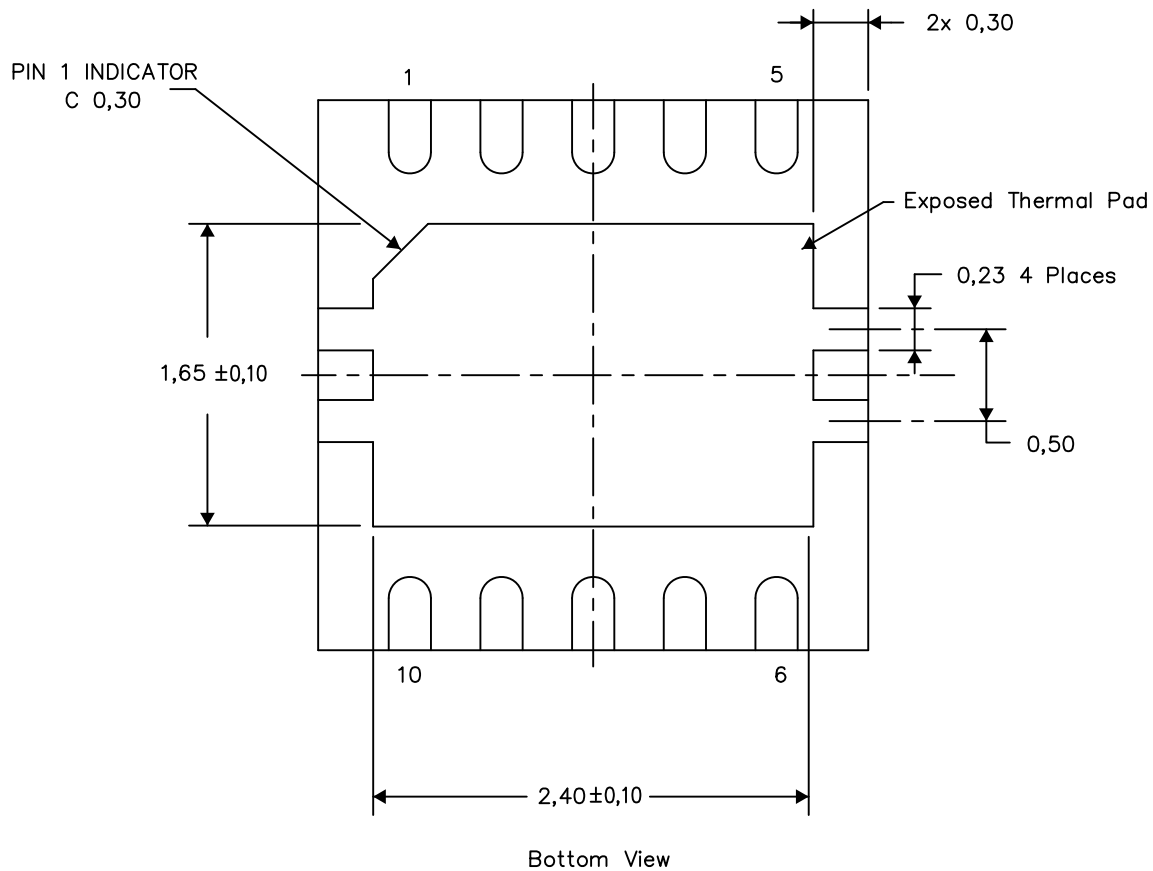
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



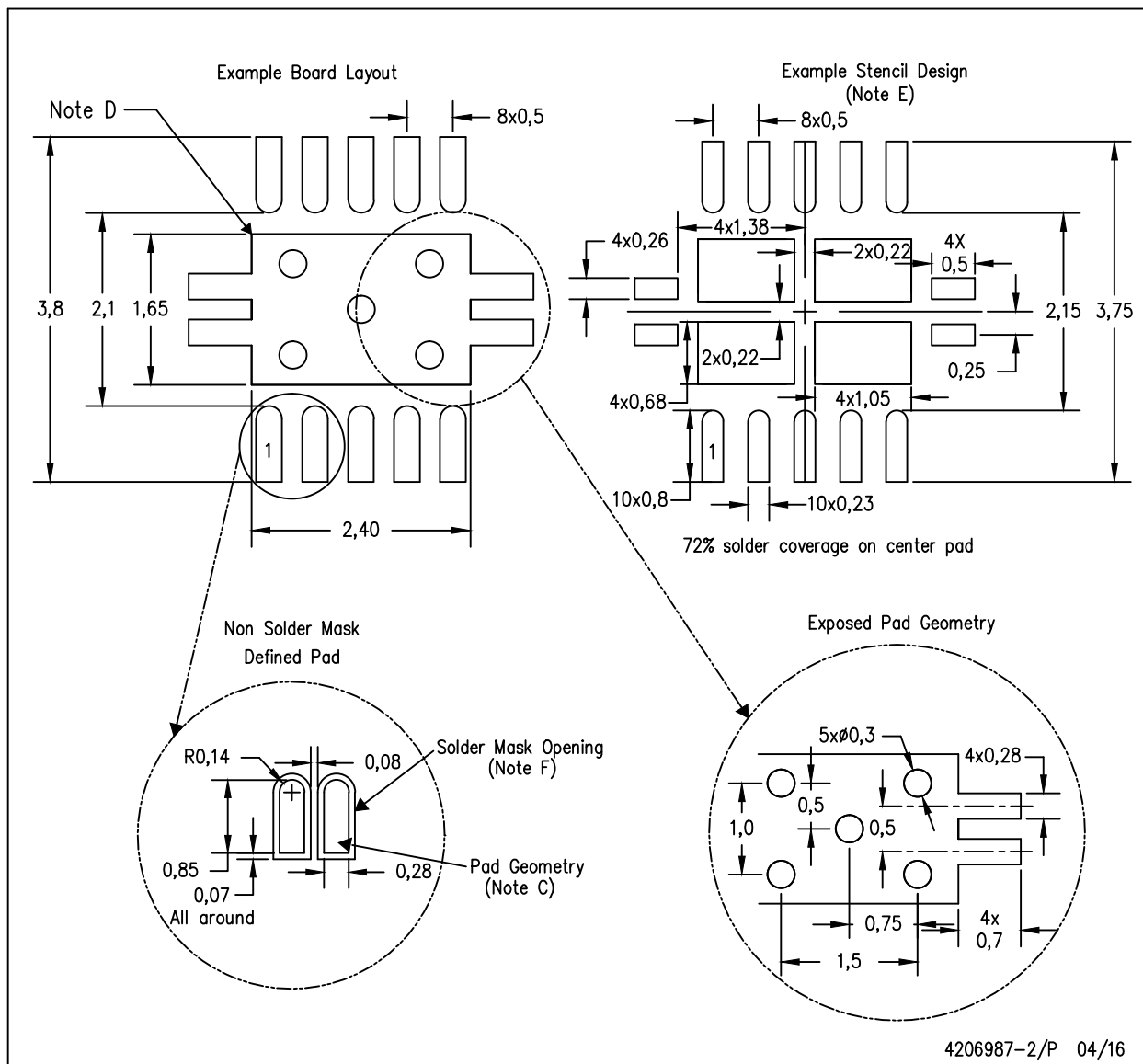
Exposed Thermal Pad Dimensions

4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Automotive and Transportation	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.