

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET
Product Summary

Device	BV _{DSS}	R _{DS(ON)} MAX	I _D MAX T _A = +25°C
Q1 N-Channel	25V	0.45Ω @ V _{GS} = 4.5V	0.68A
		0.60Ω @ V _{GS} = 2.7V	
		0.73Ω @ V _{GS} = 1.8V	
Q2 P-Channel	-25V	1.1Ω @ V _{GS} = -4.5V	-0.46A
		1.5Ω @ V _{GS} = -2.7V	
		2.2Ω @ V _{GS} = -1.8V	

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected Gate**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description

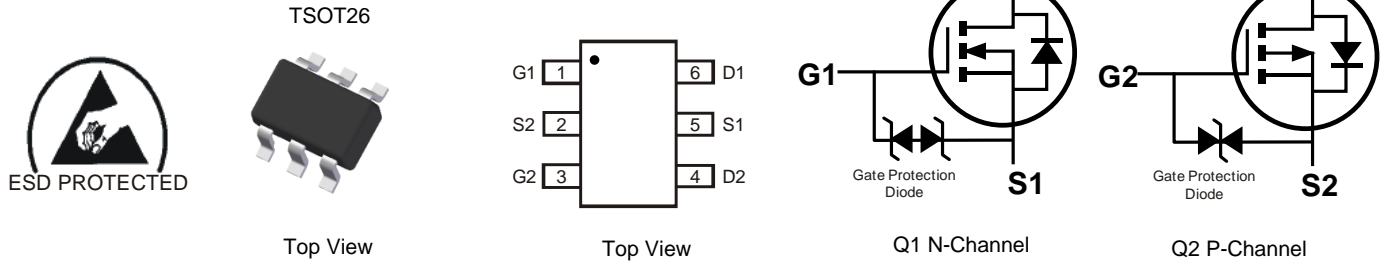
This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Backlighting
- DC-DC Converters
- Power Management Functions

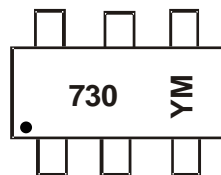
Mechanical Data

- Case: TSOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram
- Terminals: Finish – Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ^{e3}
- Weight: 0.013 grams (Approximate)


Ordering Information (Note 4)

Part Number	Case	Packaging
DMC3730UVT-7	TSOT26	3000 / Tape & Reel
DMC3730UVT-13	TSOT26	10,000 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information


730 = Product Type Marking Code
 YM = Date Code Marking
 Y or \bar{Y} = Year (ex: F = 2018)
 M = Month (ex: 9 = September)

Date Code Key

Year	2017	2018	2019	2020	2021	2022	2023	2024	2025
Code	E	F	G	H	I	J	K	L	M

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1 N-CHANNEL	Q2 P-CHANNEL	Unit
Drain-Source Voltage			V _{DSS}	25	-25	V
Gate-Source Voltage			V _{GSS}	±8	±8	V
Continuous Drain Current (Note 6) N-Channel: V _{GS} = 4.5V P-Channel: V _{GS} = -4.5V	Steady State	T _A = +25°C	I _D	0.68	-0.46	A
Maximum Continuous Body Diode Forward Current (Note 6)			I _S	0.3	-0.3	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	3	-2.5	A

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P _D	0.7	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R _{θJA}	180	°C/W
Total Power Dissipation (Note 6)		P _D	0.9	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	140	°C/W
Thermal Resistance, Junction to Case (Note 6)		R _{θJC}	60	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +175	°C

Electrical Characteristics N-CHANNEL – Q1 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	25	-	-	V	V _{GS} = 0V, I _D = 250µA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	-	-	1.0	µA	V _{DS} = 20V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	-	-	±10	µA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.45	0.7	1.1	V	V _{DS} = V _{GS} , I _D = 250µA
Static Drain-Source On-Resistance	R _{DS(ON)}	-	0.28	0.45	Ω	V _{GS} = 4.5V, I _D = 0.5A
		-	0.33	0.60		V _{GS} = 2.7V, I _D = 0.25A
		-	0.39	0.73		V _{GS} = 1.8V, I _D = 0.1A
		-	-	-		V _{GS} = 0V, I _S = 0.5A
Diode Forward Voltage	V _{SD}	-	0.75	1.2	V	V _{GS} = 0V, I _S = 0.5A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{ISS}	-	50	-	pF	V _{DS} = 10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{OSS}	-	28	-	pF	
Reverse Transfer Capacitance	C _{RSS}	-	9	-	pF	
Gate Resistance	R _g	-	64	-	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	-	1.64	-	nC	V _{DS} = 5V, I _D = 0.5A, V _{GS} = 4.5V
Gate-Source Charge	Q _{gs}	-	0.38	-	nC	
Gate-Drain Charge	Q _{gd}	-	0.45	-	nC	
Turn-On Delay Time	t _{D(ON)}	-	3	-	ns	V _{GS} = 4.5V, V _{DS} = 6V, R _g = 50Ω, I _D = 0.5A
Turn-On Rise Time	t _r	-	8	-	ns	
Turn-Off Delay Time	t _{D(OFF)}	-	17	-	ns	
Turn-Off Fall Time	t _f	-	13	-	ns	

Electrical Characteristics P-CHANNEL – Q2 (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-25	-	-	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current T _J = +25°C	I _{DSS}	-	-	-1.0	μA	V _{DS} = -20V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	-	-	±10	μA	V _{GS} = ±8V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	-0.5	-0.8	-1.1	V	V _{DS} = V _{GS} , I _D = -250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	-	0.65	1.1	Ω	V _{GS} = -4.5V, I _D = -0.5A
		-	0.80	1.5		V _{GS} = -2.7V, I _D = -0.25A
		-	1.0	2.2		V _{GS} = -1.8V, I _D = -0.1A
Diode Forward Voltage	V _{SD}	-	-0.7	-1.2	V	V _{GS} = 0V, I _S = -0.5A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{iSS}	-	63	-	pF	V _{DS} = -10V, V _{GS} = 0V, f = 1.0MHz
Output Capacitance	C _{oSS}	-	34	-	pF	
Reverse Transfer Capacitance	C _{rSS}	-	10	-	pF	
Gate Resistance	R _g	-	178	-	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	-	1.1	-	nC	V _{DS} = -5V, I _D = -0.25A , V _{GS} = -4.5V
Gate-Source Charge	Q _{gs}	-	0.32	-	nC	
Gate-Drain Charge	Q _{gd}	-	0.25	-	nC	
Turn-On Delay Time	t _{D(ON)}	-	7	-	ns	V _{GS} = -4.5V, V _{DS} = -6V, R _g = 50Ω, I _D = -0.5A
Turn-On Rise Time	t _R	-	9	-	ns	
Turn-Off Delay Time	t _{D(OFF)}	-	55	-	ns	
Turn-Off Fall Time	t _F	-	35	-	ns	

- Notes:
5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
 7. Short duration pulse test used to minimize self-heating effect.
 8. Guaranteed by design. Not subject to product testing.

Typical Characteristics - N-CHANNEL

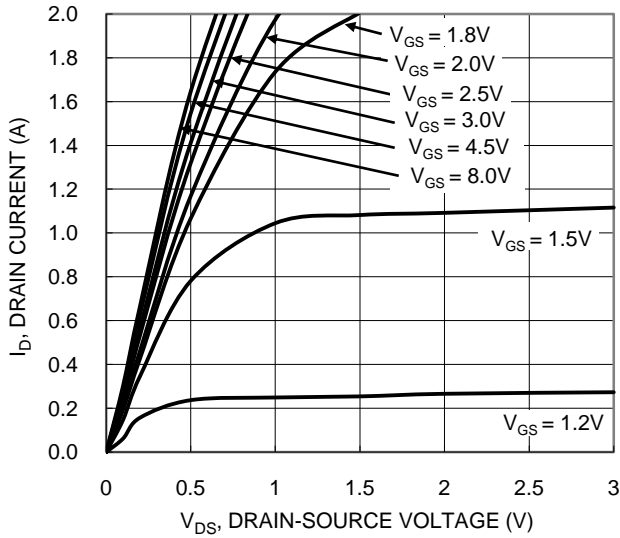


Figure 1. Typical Output Characteristic

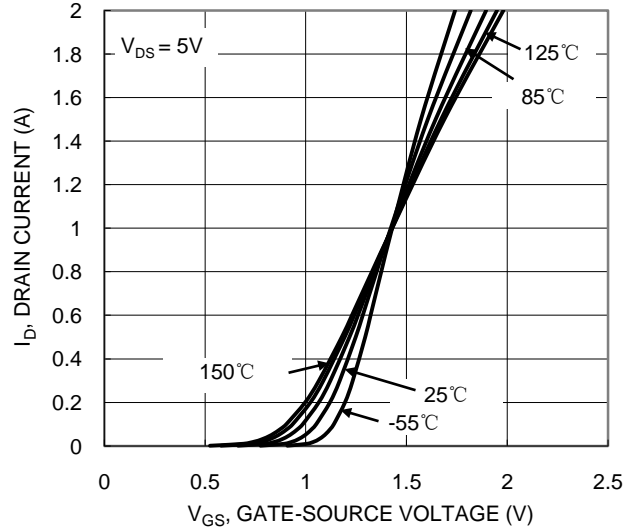


Figure 2. Typical Transfer Characteristic

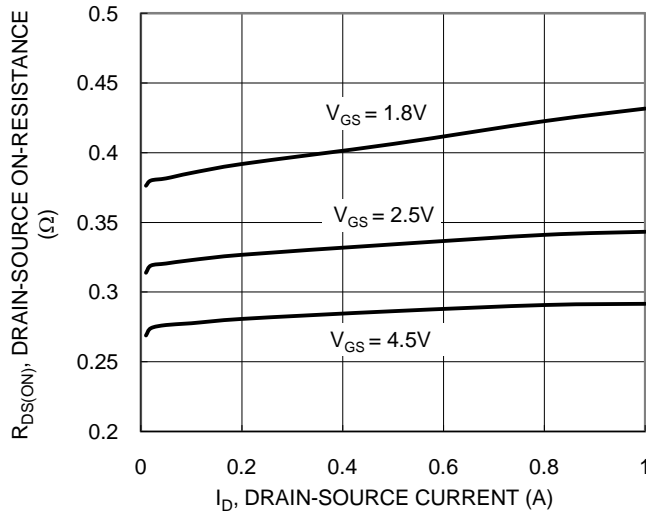


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

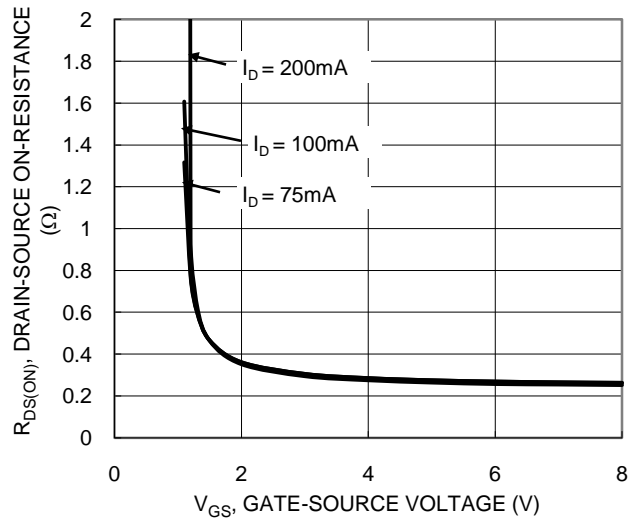


Figure 4. Typical Transfer Characteristic

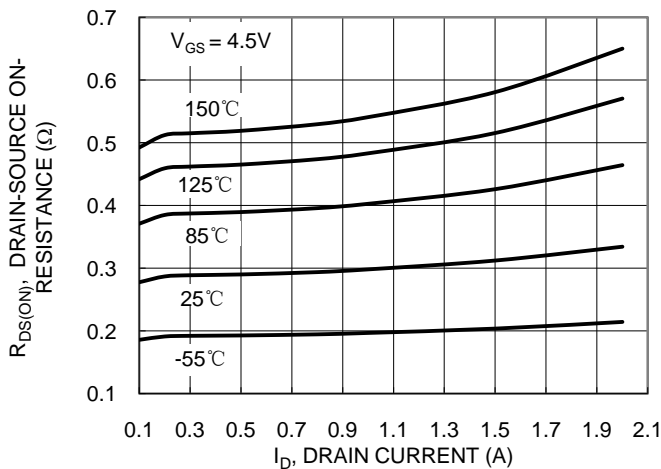


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

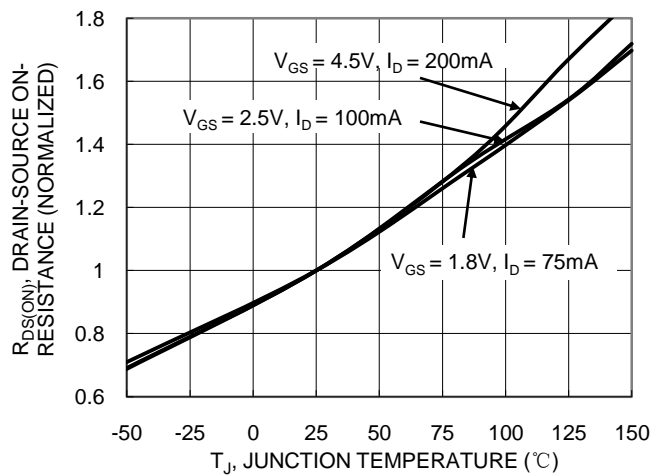


Figure 6. On-Resistance Variation with Junction Temperature

Typical Characteristics - N-CHANNEL (Cont.)

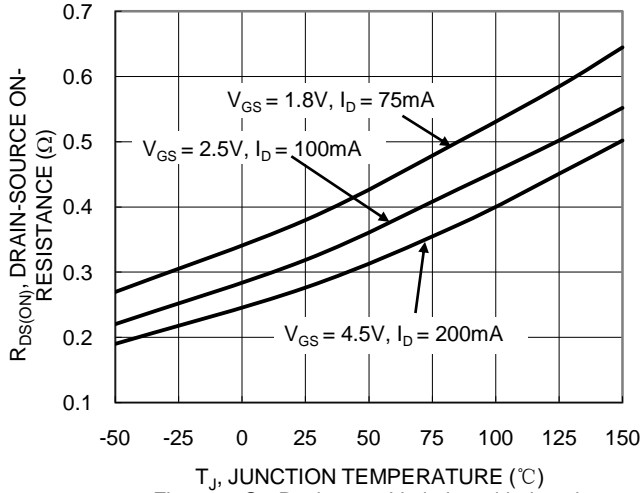


Figure 7. On-Resistance Variation with Junction Temperature

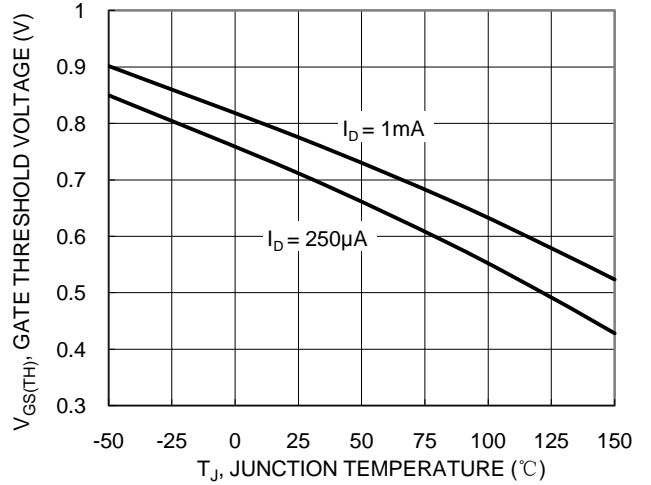


Figure 8. Gate Threshold Variation vs. Junction Temperature

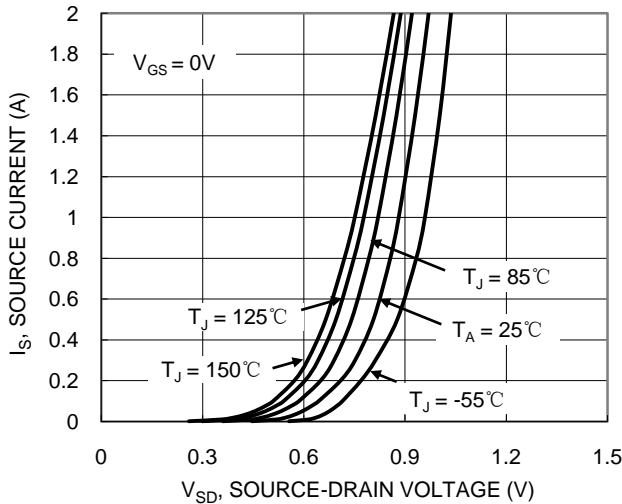


Figure 9. Diode Forward Voltage vs. Current

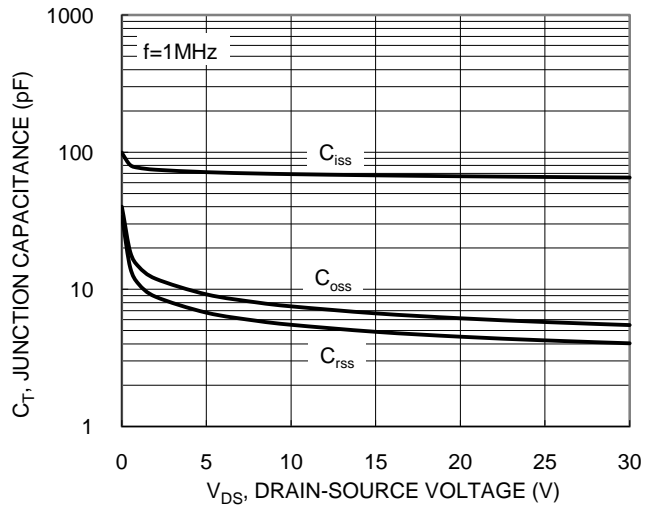


Figure 10. Typical Junction Capacitance

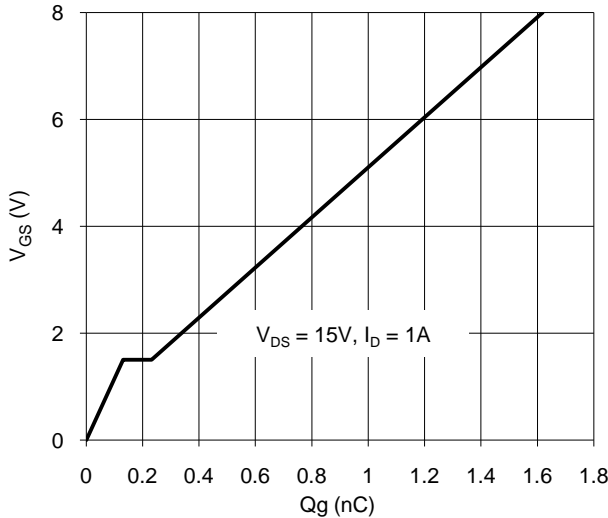


Figure 11. Gate Charge

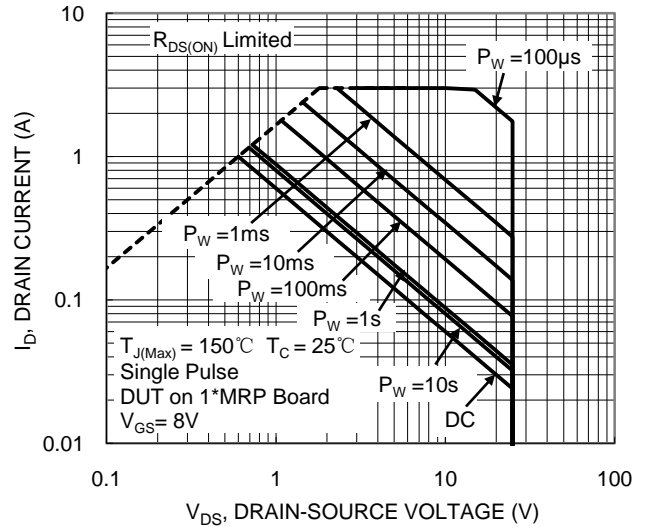


Figure 12. SOA, Safe Operation Area

Typical Characteristics - P-CHANNEL

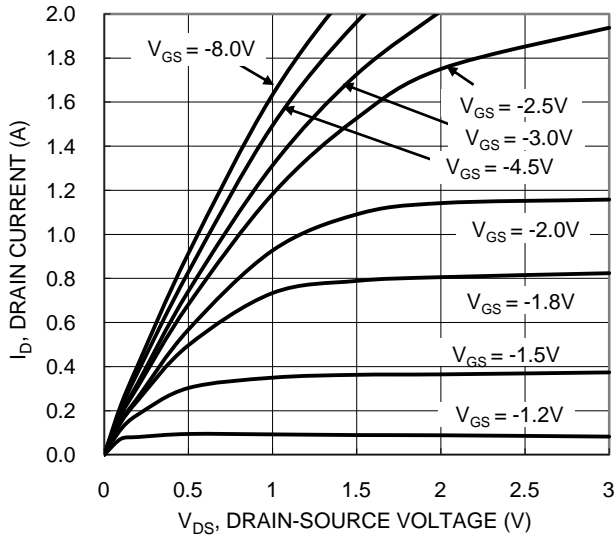


Figure 13. Typical Output Characteristic

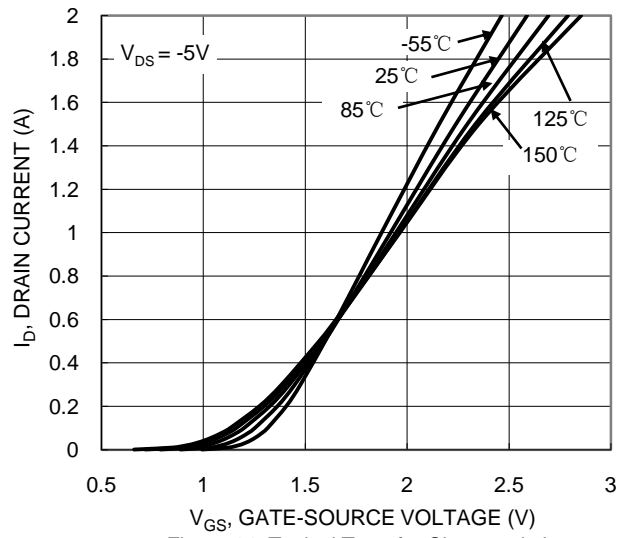


Figure 14. Typical Transfer Characteristic

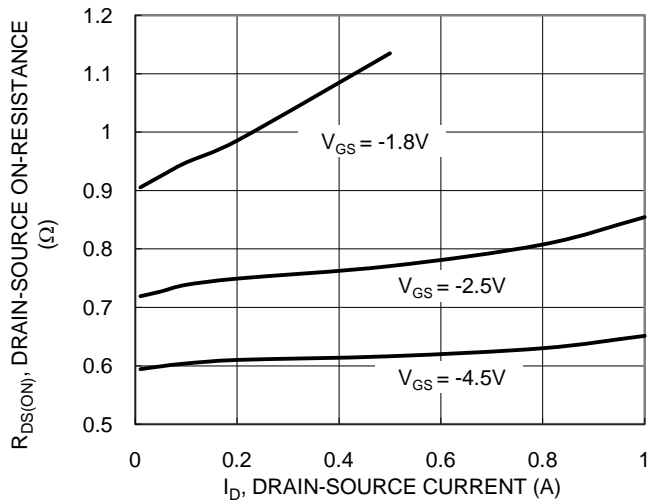


Figure 15. Typical On-Resistance vs. Drain Current and Gate Voltage

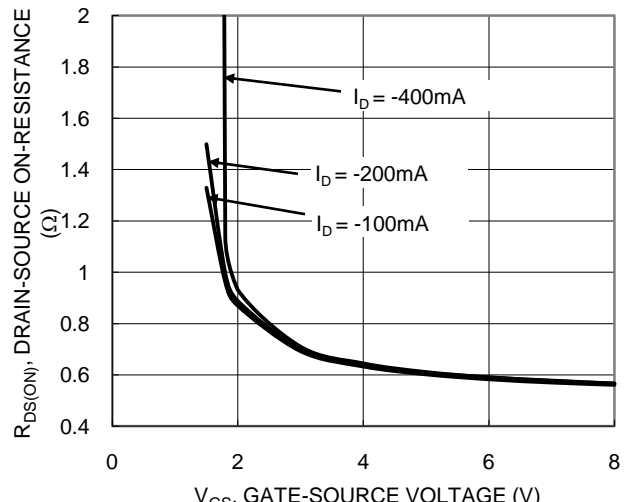


Figure 16. Typical Transfer Characteristic

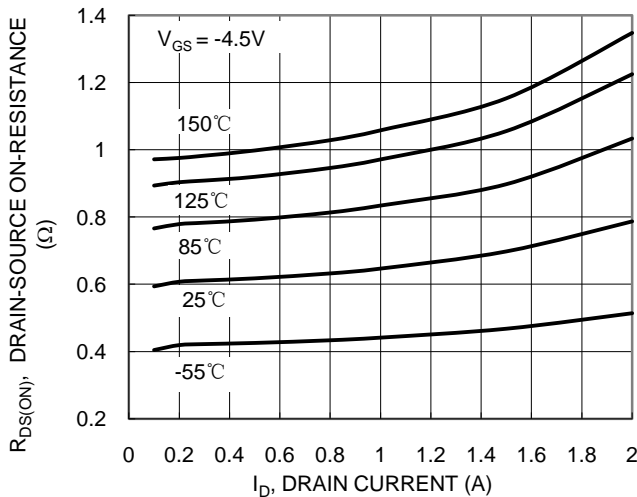


Figure 17. Typical On-Resistance vs. Drain Current and Junction Temperature

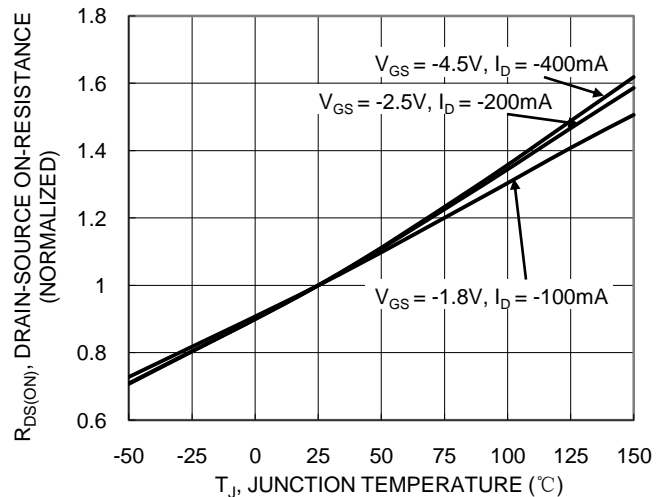


Figure 18. On-Resistance Variation with Junction Temperature

Typical Characteristics - P-CHANNEL (Cont.)

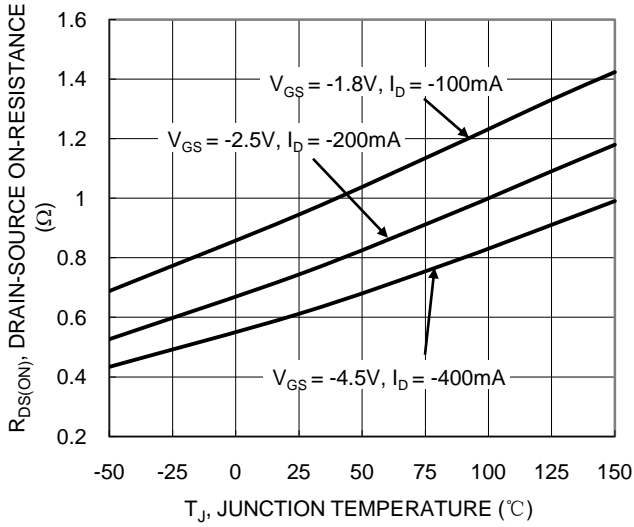


Figure 19. On-Resistance Variation with Junction Temperature

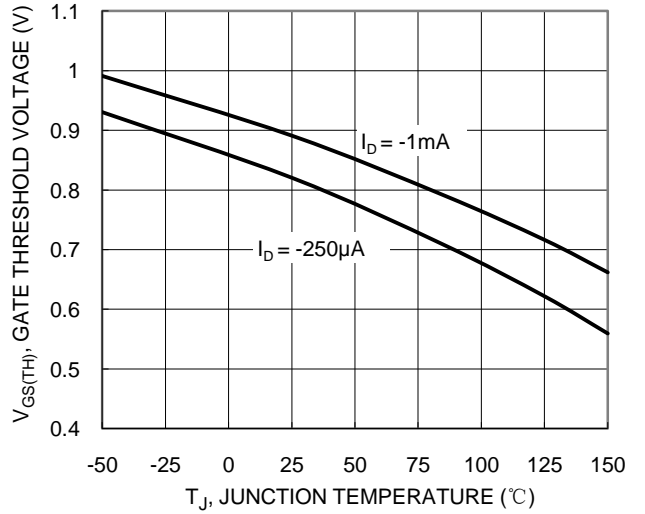


Figure 20. Gate Threshold Variation vs. Junction Temperature

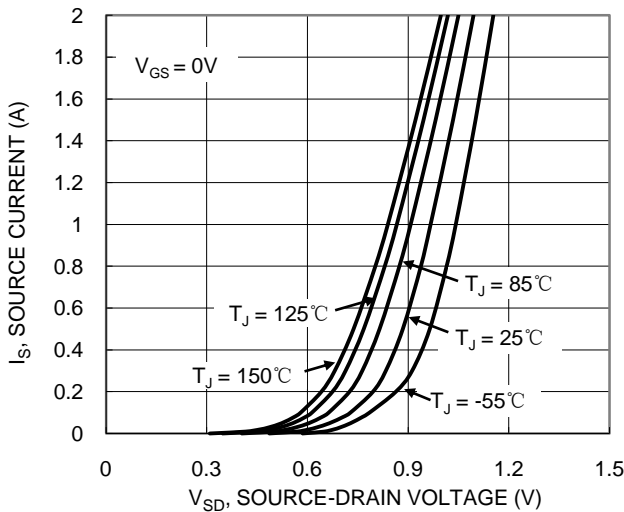


Figure 21. Diode Forward Voltage vs. Current

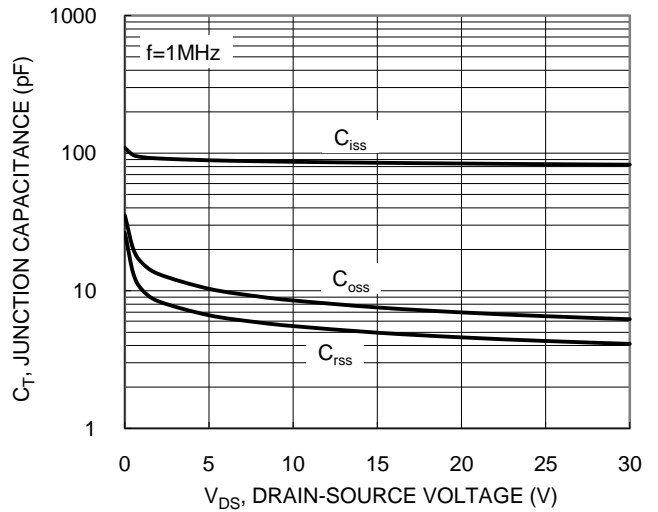


Figure 22. Typical Junction Capacitance

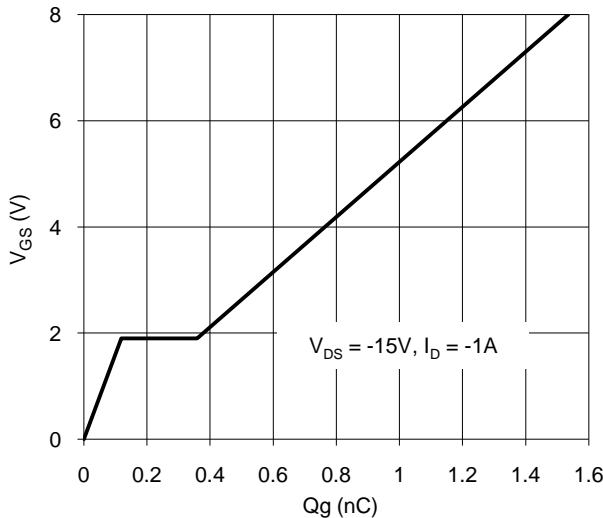


Figure 23. Gate Charge

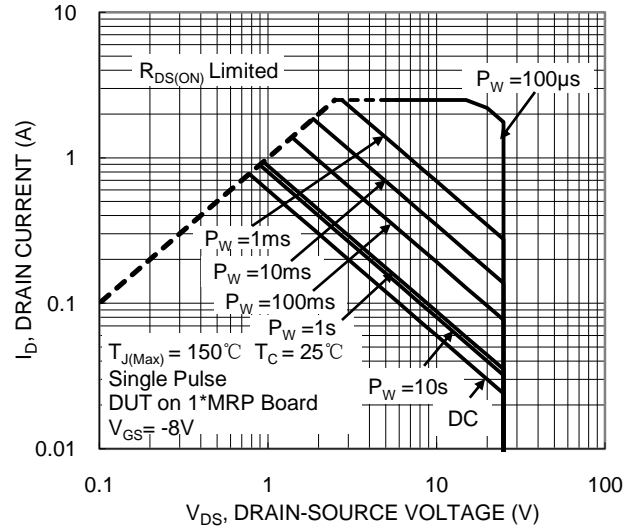


Figure 24. SOA, Safe Operation Area

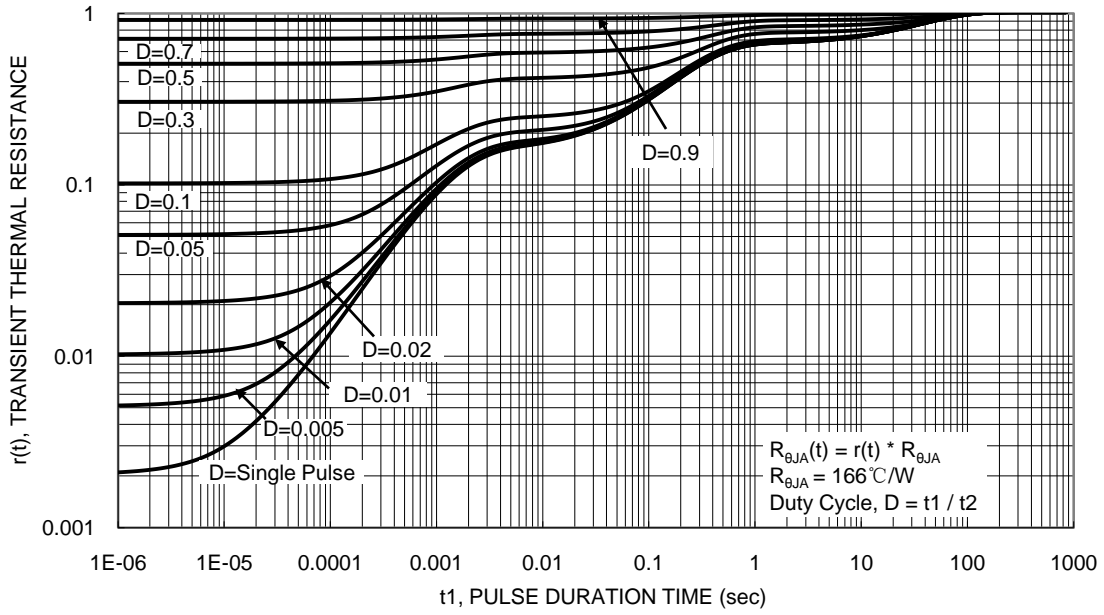
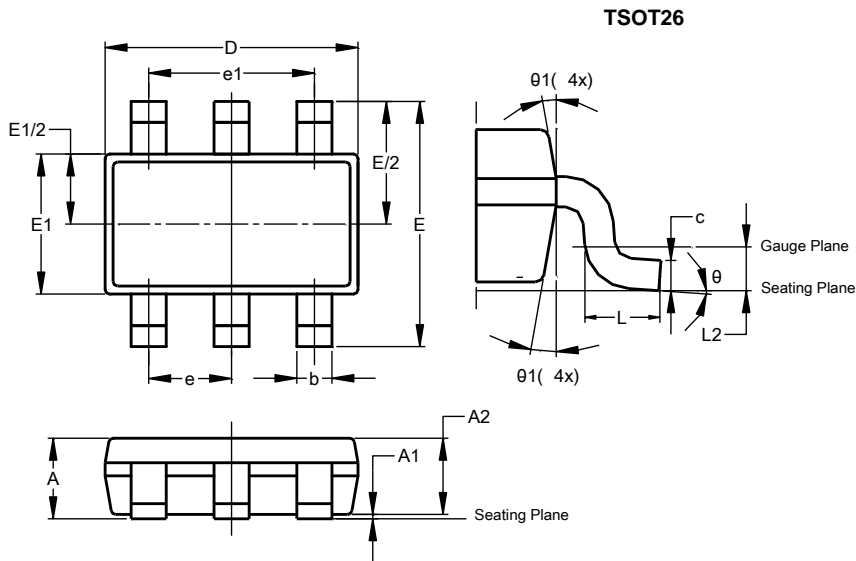


Figure 25. Transient Thermal Resistance

Package Outline Dimensions

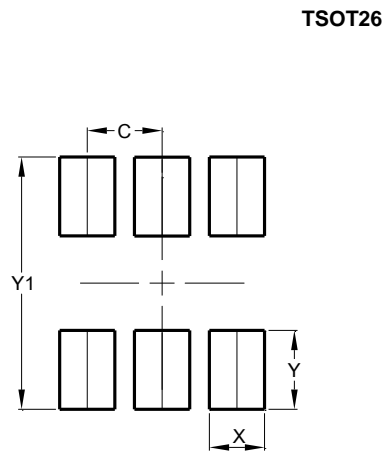
Please see <http://www.diodes.com/package-outlines.html> for the latest version.



TSOT26			
Dim	Min	Max	Typ
A	-	1.00	-
A1	0.010	0.100	-
A2	0.840	0.900	-
D	2.800	3.000	2.900
E	2.800 BSC		
E1	1.500	1.700	1.600
b	0.300	0.450	-
c	0.120	0.200	-
e	0.950 BSC		
e1	1.900 BSC		
L	0.30	0.50	-
L2	0.250 BSC		
θ	0°	8°	4°
θ_1	4°	12°	-
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.



Dimensions	Value (in mm)
C	0.950
X	0.700
Y	1.000
Y1	3.199

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.