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Kind regards,

Team Nexperia

# PEMH20; PUMH20

NPN/NPN resistor-equipped transistors;

R1 = 2.2 k $\Omega$ , R2 = 2.2 k $\Omega$

Rev. 04 — 15 November 2009

Product data sheet

## 1. Product profile

### 1.1 General description

NPN/NPN resistor-equipped transistors.

Table 1. Product overview

Type number	Package		NPN/PNP complement	PNP/PNP complement
	NXP	JEITA		
PEMH20	SOT666	-	PEMD20	PEMB20
PUMH20	SOT363	SC-88	PUMD20	PUMB20

### 1.2 Features

- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

### 1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

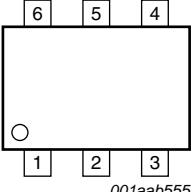
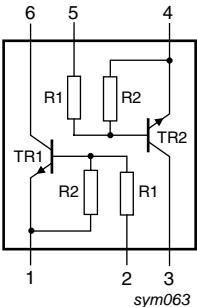
### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current (DC)		-	-	100	mA
R1	bias resistor 1 (input)		1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	

## 2. Pinning information

**Table 3. Pinning**

Pin	Description	Simplified outline	Symbol
1	GND (emitter) TR1	 <p>001aab555</p>	 <p>sym063</p>
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

## 3. Ordering information

**Table 4. Ordering information**

Type number	Package		Version
	Name	Description	
PEMH20	-	plastic surface mounted package; 6 leads	SOT666
PUMH20	SC-88	plastic surface mounted package; 6 leads	SOT363

## 4. Marking

**Table 5. Marking codes**

Type number	Marking code <sup>[1]</sup>
PEMH20	6K
PUMH20	H7*

[1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

## 5. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{CBO}$	collector-base voltage	open emitter	-	50	V	
$V_{CEO}$	collector-emitter voltage	open base	-	50	V	
$V_{EBO}$	emitter-base voltage	open collector	-	10	V	
$V_I$	input voltage					
	positive		-	+12	V	
	negative		-	-10	V	
$I_O$	output current (DC)		-	100	mA	
$I_{CM}$	peak collector current		-	100	mA	
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$				
	SOT363		[1]	-	200	mW
	SOT666		[1][2]	-	200	mW
$T_{stg}$	storage temperature		-65	+150	$^\circ\text{C}$	
$T_j$	junction temperature		-	150	$^\circ\text{C}$	
$T_{amb}$	ambient temperature		-65	+150	$^\circ\text{C}$	
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^\circ\text{C}$				
	SOT363		[1]	-	300	mW
	SOT666		[1][2]	-	300	mW

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	625	K/W
	SOT666		[1][2]	-	625	K/W
<b>Per device</b>						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air				
	SOT363		[1]	-	416	K/W
	SOT666		[1][2]	-	416	K/W

[1] Device mounted on a FR4 printed-circuit board, single-sided copper, tin-plated and standard footprint.

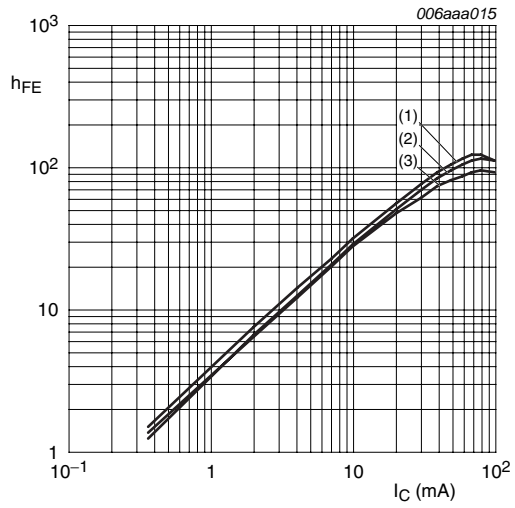
[2] Reflow soldering is the only recommended soldering method.

## 7. Characteristics

**Table 8. Characteristics**

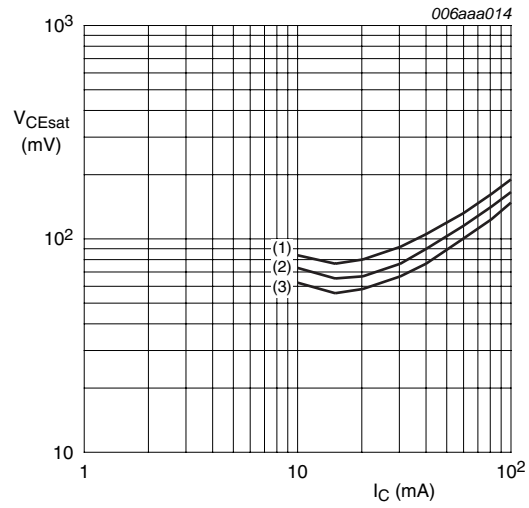
*T<sub>amb</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A	-	-	100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A	-	-	1	$\mu$ A
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = 5 V; I <sub>C</sub> = 0 A	-	-	2	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 20 mA	30	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 0.5 mA	-	-	150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 1 mA	-	1.2	0.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 20 mA	2	1.6	-	V
R1	bias resistor1 (input)		1.54	2.2	2.86	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = 10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A; f = 1 MHz	-	-	2.5	pF



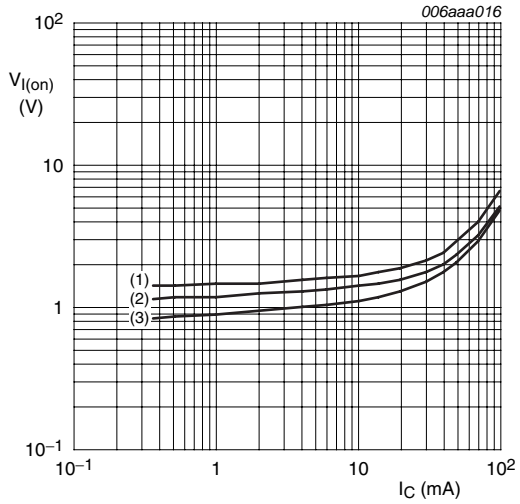
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = 150\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig. 1. DC current gain as a function of collector current; typical values**



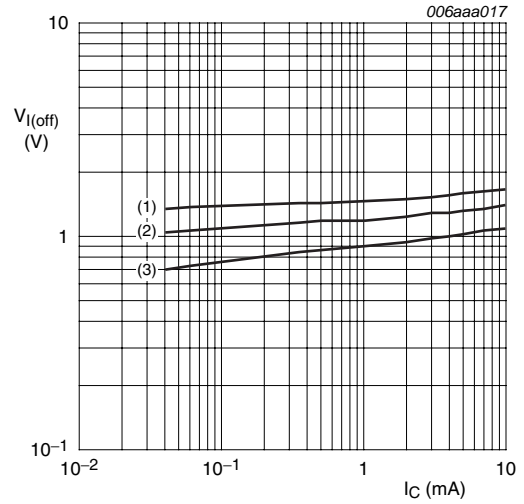
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40\text{ }^\circ\text{C}$

**Fig. 2. Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = 0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

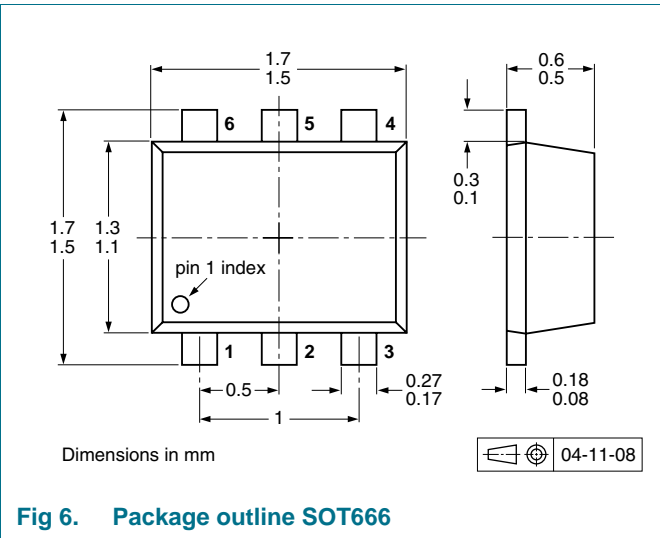
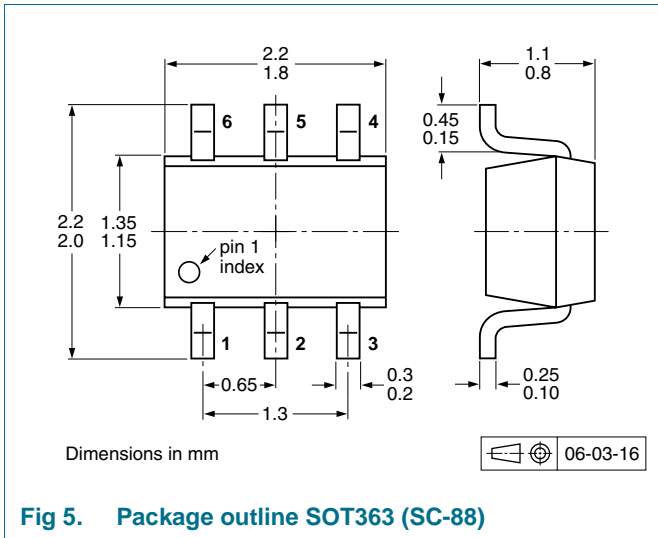
**Fig. 3. On-state input voltage as a function of collector current; typical values**



$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = -40\text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25\text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100\text{ }^\circ\text{C}$

**Fig. 4. Off-state input voltage as a function of collector current; typical values**

### 8. Package outline



### 9. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMH20	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMH20	SOT363	4 mm pitch, 8 mm tape and reel; T1 <sup>[2]</sup>	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 <sup>[3]</sup>	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 12](#).

[2] T1: normal taping

[3] T2: reverse taping

## 10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMH20_PUMH20_4	20091115	Product data sheet	-	PEMH20_PUMH20_3
Modifications:	<ul style="list-style-type: none"> <li>This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.</li> <li><a href="#">Figure 5 "Package outline SOT363 (SC-88)"; updated</a></li> </ul>			
PEMH20_PUMH20_3	20050214	Product data sheet	-	PUMH20_2
PUMH20_2	20040414	Product specification	-	PUMH20_1
PUMH20_1	20031016	Product specification	-	-



## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

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**13. Contents**

**1 Product profile . . . . . 1**

1.1 General description . . . . . 1

1.2 Features . . . . . 1

1.3 Applications . . . . . 1

1.4 Quick reference data . . . . . 1

**2 Pinning information . . . . . 2**

**3 Ordering information . . . . . 2**

**4 Marking . . . . . 2**

**5 Limiting values . . . . . 3**

**6 Thermal characteristics . . . . . 4**

**7 Characteristics . . . . . 4**

**8 Package outline . . . . . 6**

**9 Packing information . . . . . 6**

**10 Revision history . . . . . 7**

**11 Legal information . . . . . 8**

11.1 Data sheet status . . . . . 8

11.2 Definitions . . . . . 8

11.3 Disclaimers . . . . . 8

11.4 Trademarks . . . . . 8

**12 Contact information . . . . . 8**

**13 Contents . . . . . 9**

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