



BUK7K15-80E

Dual N-channel 80 V, 15 mΩ standard level MOSFET

11 May 2018

Product data sheet

1. General description

Dual Standard level N-channel MOSFET in an LFPK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with $V_{GS(th)}$ rating of greater than 1 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

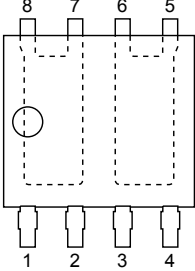
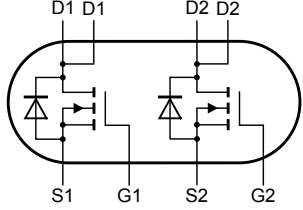
4. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-----|------|-----|------|
| Limiting values FET1 and FET2 | | | | | | |
| V_{DS} | drain-source voltage | $25\text{ °C} \leq T_j \leq 175\text{ °C}$ | - | - | 80 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2 | - | - | 23 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; Fig. 1 | - | - | 68 | W |
| Static characteristics FET1 and FET2 | | | | | | |
| R_{DSon} | drain-source on-state resistance | $V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | - | 11.2 | 15 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| Q_{GD} | gate-drain charge | $I_D = 10\text{ A}$; $V_{DS} = 64\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14 | - | 11.3 | - | nC |
| Source-drain diode FET1 and FET2 | | | | | | |
| Q_r | recovered charge | $I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $T_j = 25\text{ °C}$ | - | 37.7 | - | nC |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------|--|--|
| 1 | S1 | source1 |  <p>LFPAK56D (SOT1205)</p> |  <p><i>mbk725</i></p> |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | Version |
|-------------|----------|---|---------|
| | Name | Description | |
| BUK7K15-80E | LFPAK56D | plastic, single ended surface mounted package (LFPAK56D); 8 leads | SOT1205 |

7. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| BUK7K15-80E | 71580E |

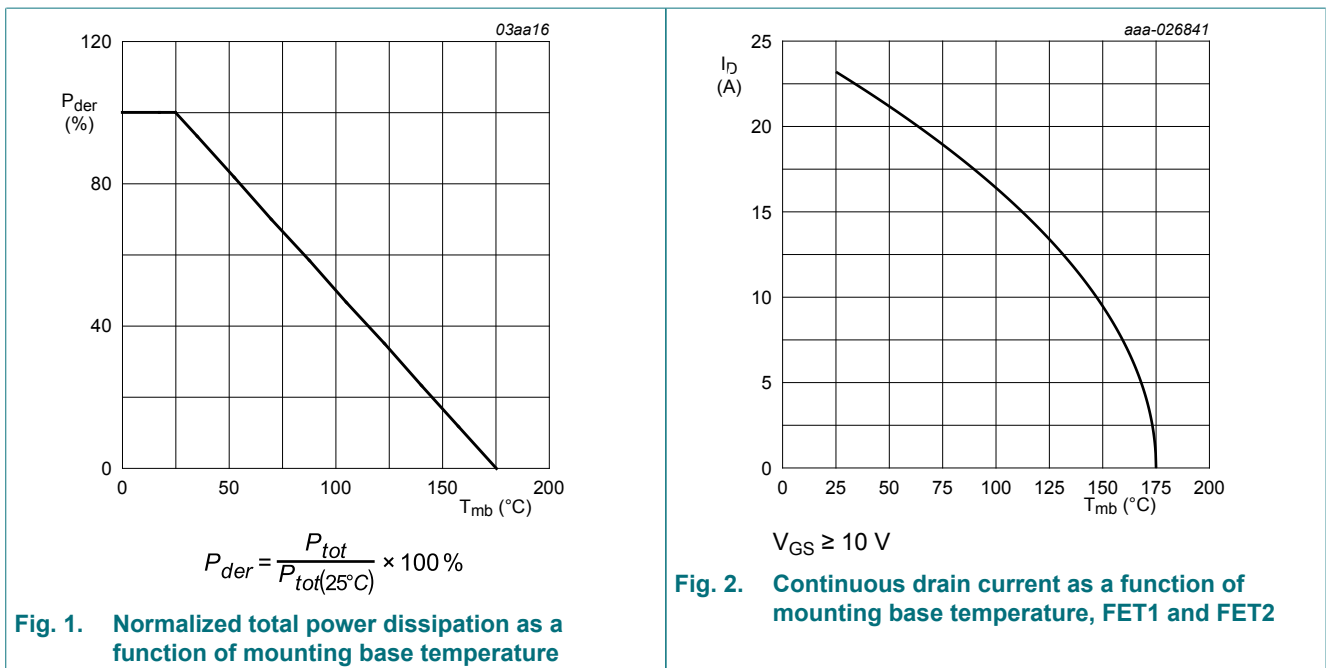
8. Limiting values

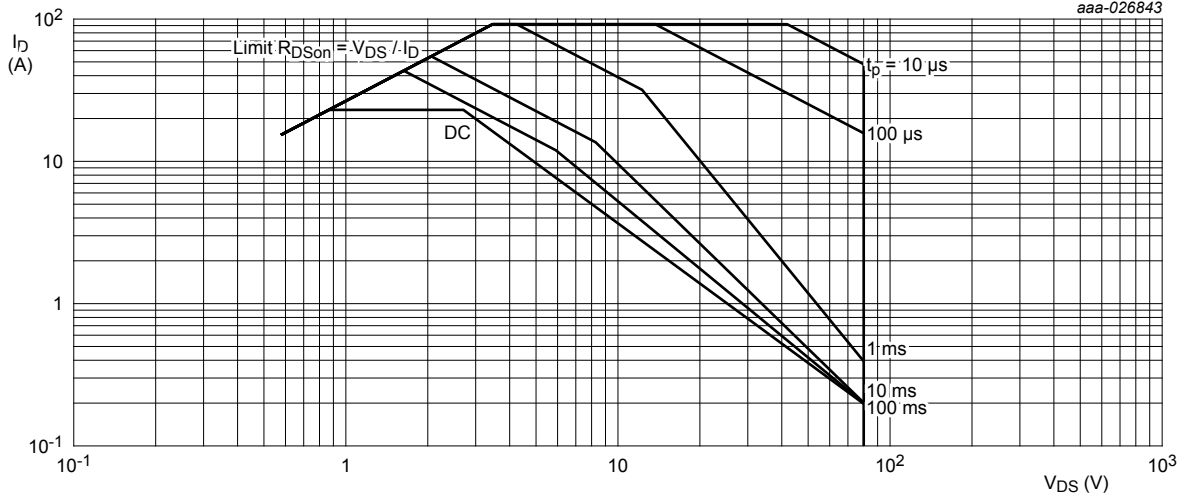
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|--|---|---------|-----|------|
| Limiting values FET1 and FET2 | | | | | |
| V _{DS} | drain-source voltage | 25 °C ≤ T _j ≤ 175 °C | - | 80 | V |
| V _{DGR} | drain-gate voltage | R _{GS} = 20 kΩ | - | 80 | V |
| V _{GS} | gate-source voltage | DC; T _j ≤ 175 °C | 20 | -20 | V |
| P _{tot} | total power dissipation | T _{mb} = 25 °C; Fig. 1 | - | 68 | W |
| I _D | drain current | V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2 | - | 23 | A |
| | | V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2 | - | 16 | A |
| I _{DM} | peak drain current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3 | - | 92 | A |
| T _{stg} | storage temperature | | -55 | 175 | °C |
| T _j | junction temperature | | -55 | 175 | °C |
| Source-drain diode FET1 and FET2 | | | | | |
| I _S | source current | T _{mb} = 25 °C | - | 23 | A |
| I _{SM} | peak source current | pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C | - | 92 | A |
| Avalanche ruggedness FET1 and FET2 | | | | | |
| E _{DS(AL)S} | non-repetitive drain-source avalanche energy | I _D = 23 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4 | [1] [2] | 133 | mJ |

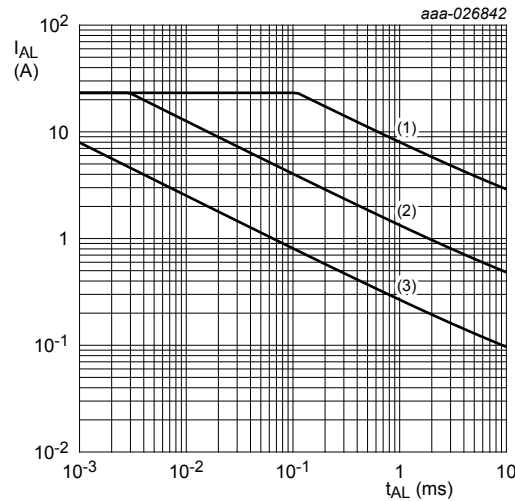
- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.





$T_{mb} = 25\text{ }^{\circ}\text{C}$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2



(1) $T_{j\text{ (init)}} = 25\text{ }^{\circ}\text{C}$; (2) $T_{j\text{ (init)}} = 150\text{ }^{\circ}\text{C}$; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|---|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | - | - | 2.21 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | Minimum footprint; mounted on a printed circuit board | - | 95 | - | K/W |

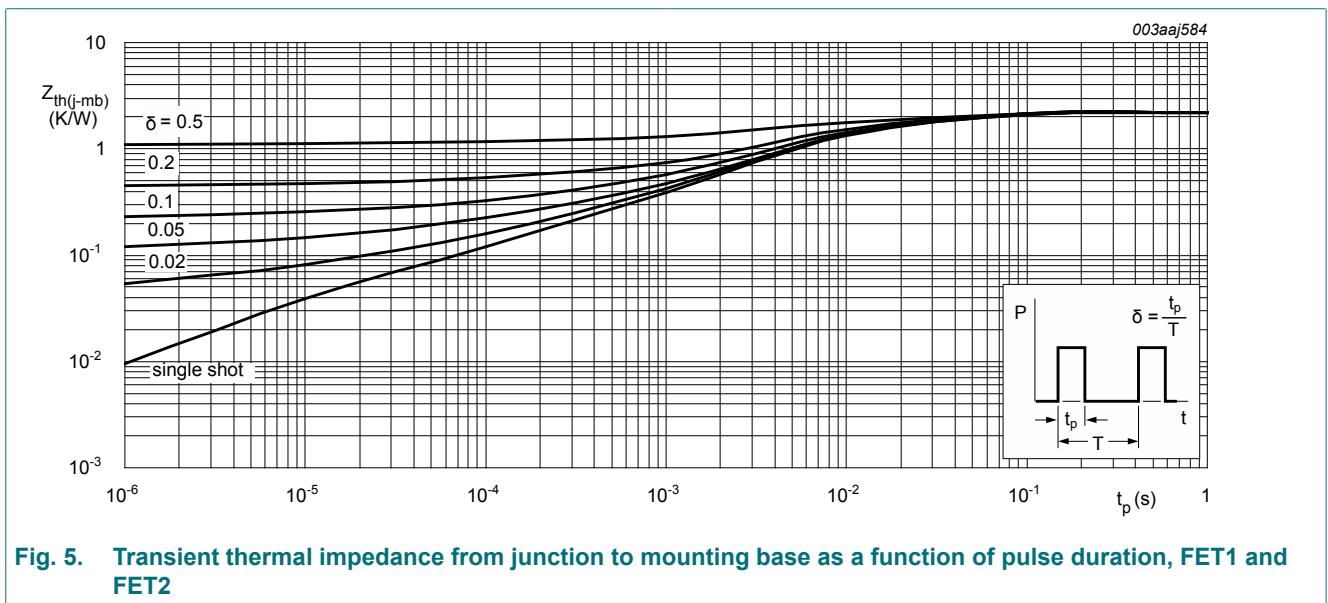


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------------|--|-----|------|------|---------------|
| Static characteristics FET1 and FET2 | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | 80 | - | - | V |
| | | $I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$ | 72 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 9 ; Fig. 10 | 2.4 | 3 | 4 | V |
| | | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ Fig. 10 | - | - | 4.5 | V |
| | | $I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 10 | 1 | - | - | V |
| I_{DSS} | drain leakage current | $V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 0.03 | 1 | μA |
| | | $V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ | - | - | 500 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| | | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 2 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 11 | - | 11.2 | 15 | mΩ |
| | | $V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 12 | - | - | 38 | mΩ |
| Dynamic characteristics FET1 and FET2 | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 10 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 13 ; Fig. 14 | - | 35.1 | - | nC |
| Q_{GS} | gate-source charge | | - | 7.4 | - | nC |
| Q_{GD} | gate-drain charge | | - | 11.3 | - | nC |
| C_{iss} | input capacitance | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 15 | - | 1847 | 2457 | pF |
| C_{oss} | output capacitance | | - | 194 | 233 | pF |
| C_{rss} | reverse transfer capacitance | | - | 115 | 158 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 60 \text{ V}; R_L = 5 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$ | - | 8.8 | - | ns |
| t_r | rise time | | - | 12.6 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 25.1 | - | ns |
| t_f | fall time | | - | 15.1 | - | ns |
| Source-drain diode FET1 and FET2 | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 16 | - | 0.8 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ | - | 30.5 | - | ns |
| Q_r | recovered charge | | - | 37.7 | - | nC |

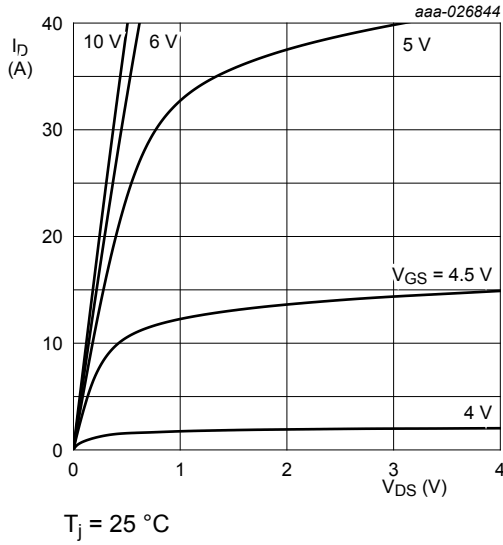


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

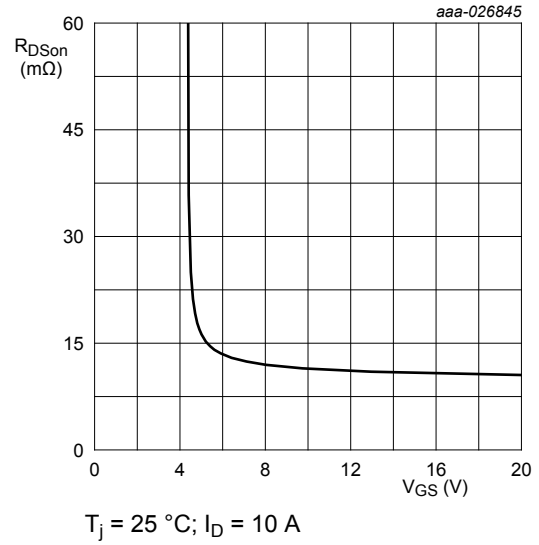


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2

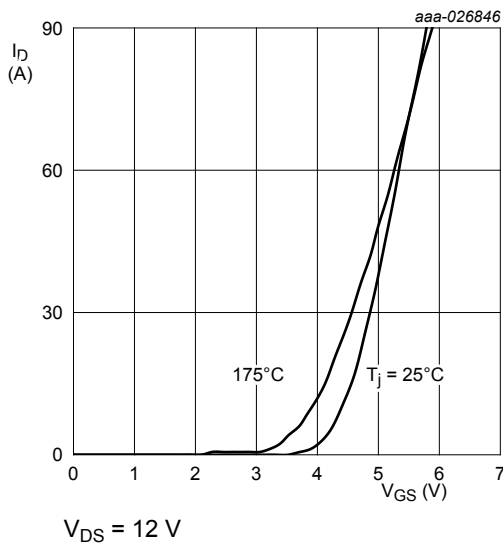


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

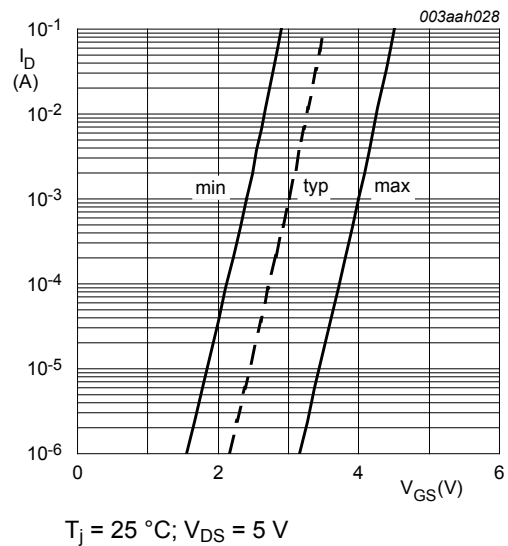


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

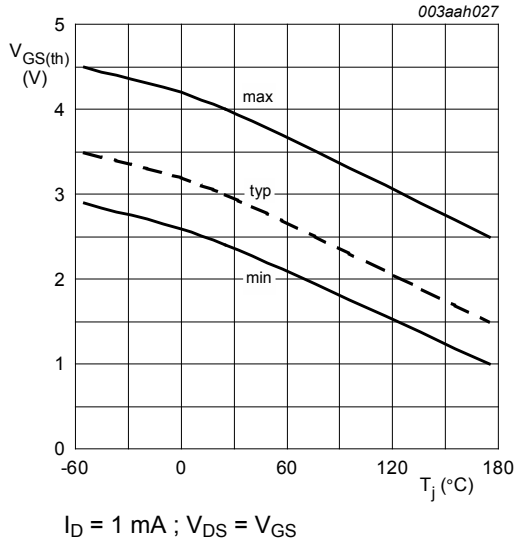


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

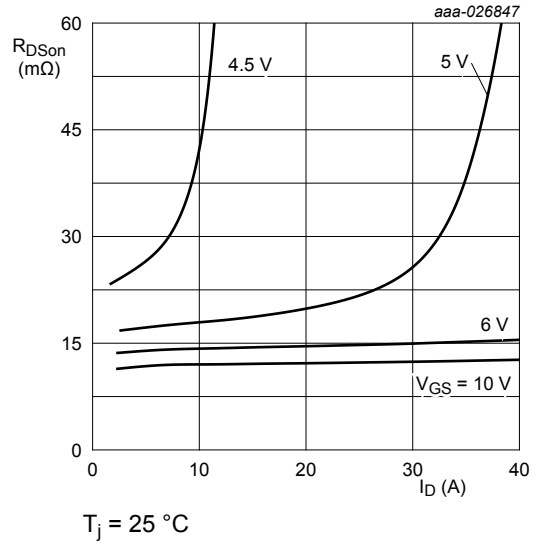


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

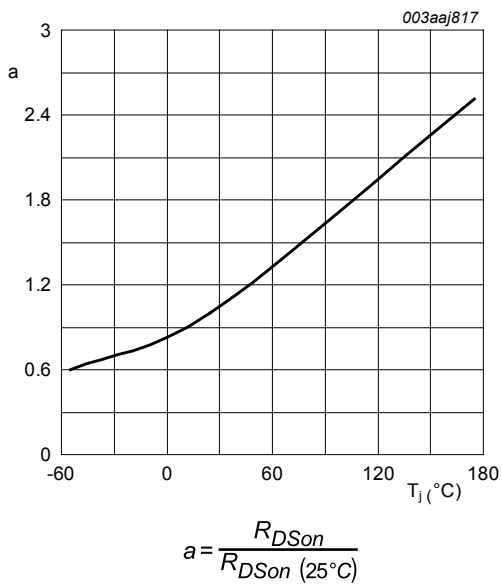


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

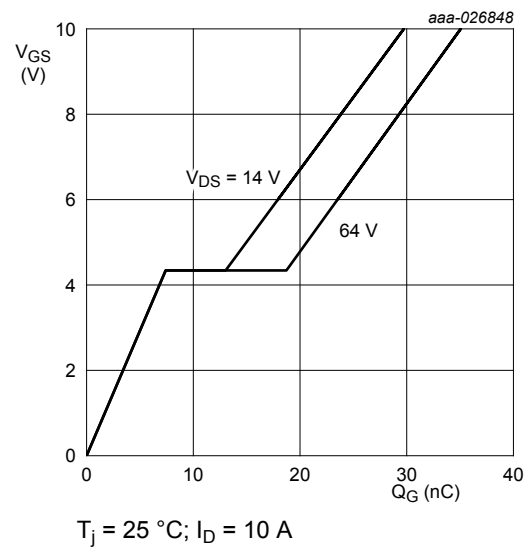


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

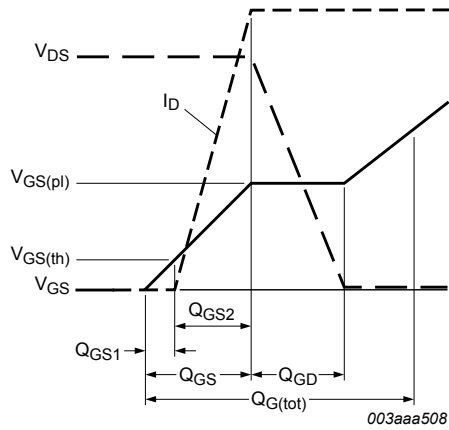
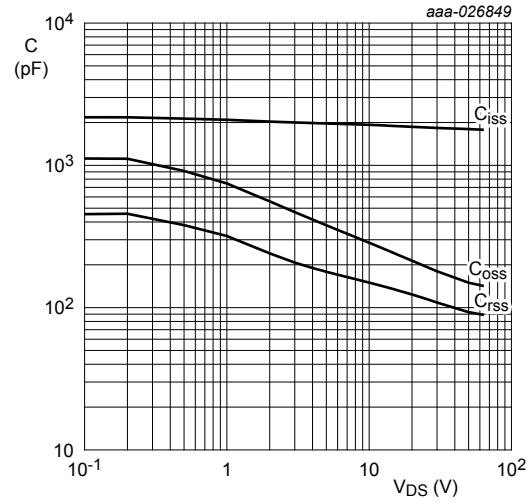
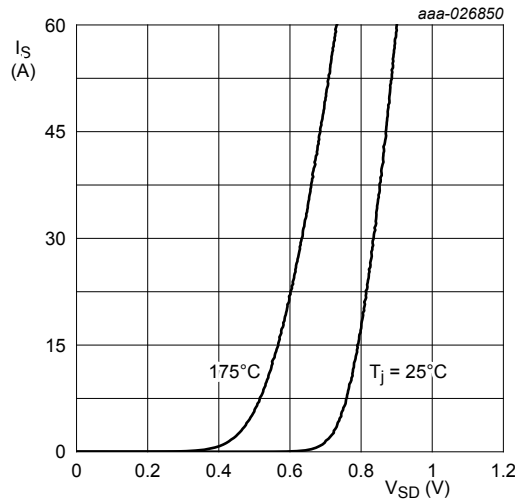


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0 \text{ V}$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2

11. Package outline

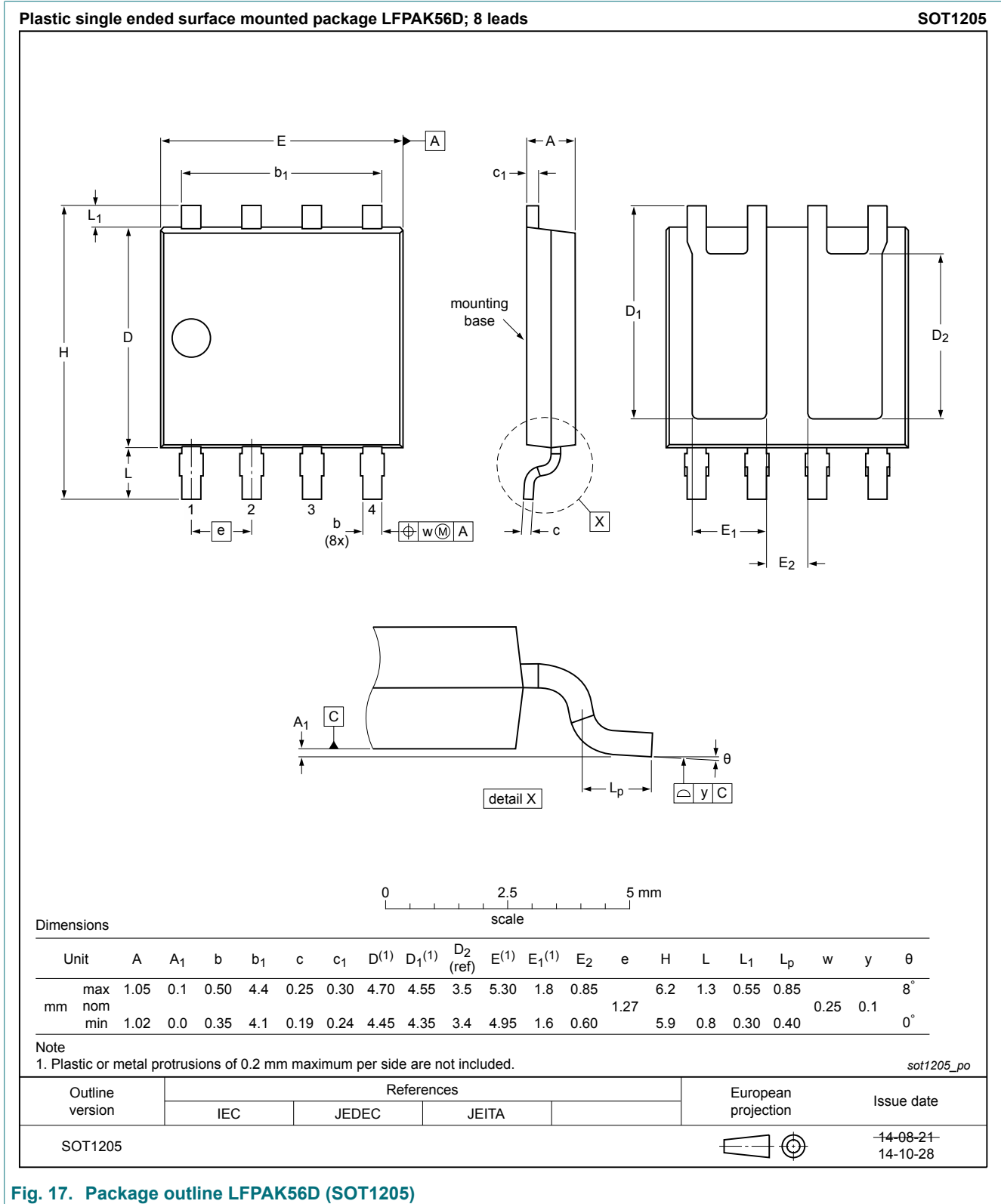


Fig. 17. Package outline LFAK56D (SOT1205)

12. Legal information

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Date of release: 11 May 2018



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