

Automotive 300mA Variable Output LDO Regulator



BDxxGA3MEFJ-M

General Description

BDxxGA3MEFJ-M is a LDO regulator with output current 0.3A. The output accuracy is $\pm 1\%$ of output voltage. With external resistance, it is available to set the output voltage at random (from 1.5V to 13.0V). It has package type: HTSOP-J8. Over current protection (for protecting the IC destruction by output short circuit), circuit current ON/OFF switch (for setting the circuit 0 μ A at shutdown mode), and thermal shutdown circuit (for protecting IC from heat destruction by over load condition) are all built in. It is usable for ceramic capacitor and enables to improve smaller set and long-life.

Features

- High accuracy reference voltage circuit
- Built-in Over Current Protection circuit (OCP)
- Built-in Thermal Shut Down circuit (TSD)
- With shut down switch
- AEC-Q100 Qualified

Key Specifications

- Input power supply voltage range: 4.5V to 14.0V
- Output voltage range(Variable type): 1.5V to 13.0V
- Output voltage(Fixed type): 1.5V/1.8V/2.5V/3

●Ordering Information

B	D	x	x	G	A	3	M	E	F	J	-	M	E	2
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Part Number	Output voltage	Voltage resistance	Output current	Automotive "M":M Series	Package	Packaging and forming specification
	00:Variable	G:15V	A3:0.3A		EFJ:HTSOP-J8	E2:Emboss tape reel
	15:1.5V					
	18:1.8V					
	25:2.5V					
	30:3.0V					
	33:3.3V					
	50:5.0V					
	60:6.0V					
	70:7.0V					
	80:8.0V					
	90:9.0V					
	J0:10.0V					
	J2:12.0V					

●Block Diagram

BDxxGA3MEFJ-M

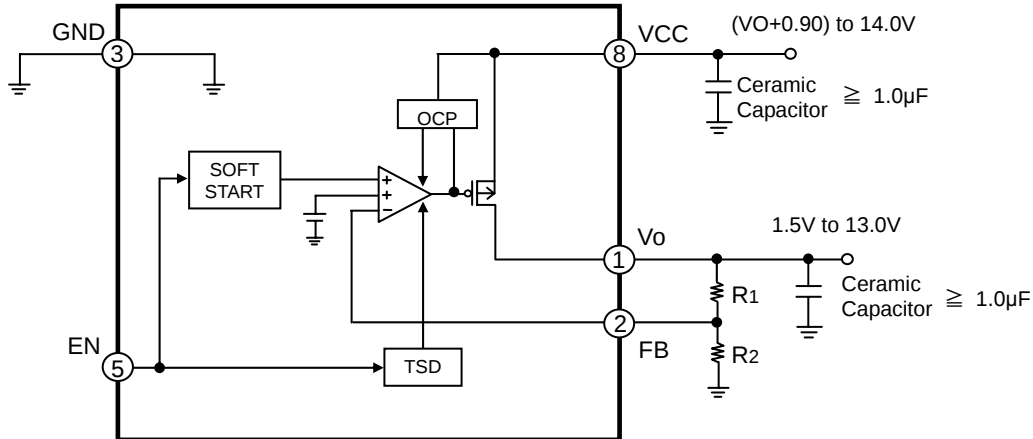


Figure 1. Block Diagram

BDxxGA3MEFJ-M (Fixed type)

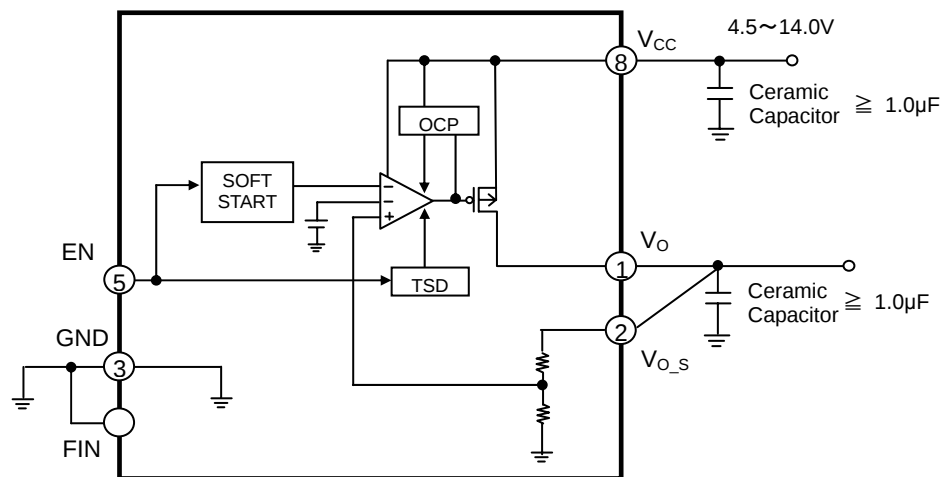
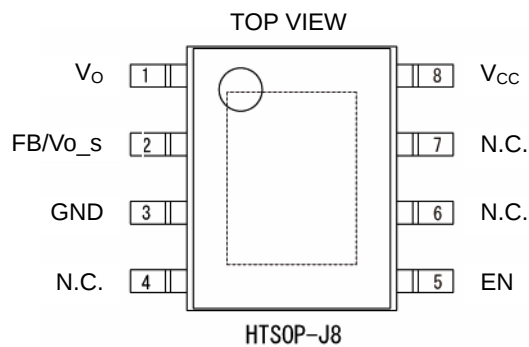


Figure 2. Block Diagram (Fixed type)

●Pin Configuration



●Absolute Maximum Ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Power supply voltage		V _{CC}	15.0 ^{*1}	V
EN voltage		V _{EN}	15.0	V
Power dissipation	HTSOP-J8	Pd ^{*2}	2110 ^{*2}	mW
Operating Temperature Range		Topr	-40 to +105	°C
Storage Temperature Range		Tstg	-55 to +150	°C
Junction Temperature		Tjmax	+150	°C

^{*1} Not to exceed Pd

^{*2} Reduced by 16.9mW/°C for each increase in Ta of 1°C over 25°C. (when mounted on a board 70mm × 70mm × 1.6mm glass-epoxy board, two layer)

●Recommended Operating Ratings (Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit
Input power supply voltage	V _{CC}	4.5	14.0	V
EN voltage				

●Typical Performance Curves

(Unless otherwise noted, EN=3V, V_{CC}=6V, R₁=43k Ω , R₂=8.2k Ω)

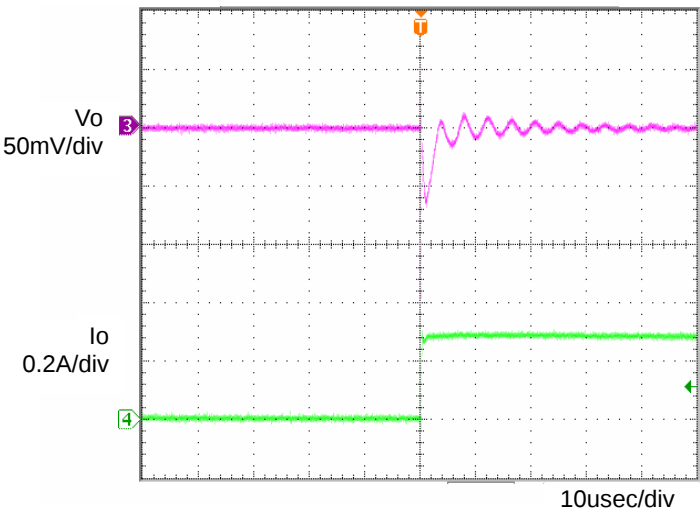


Figure 3.
Transient Response
(0→0.3A)
Co=1 μ F, Ta=-40°C

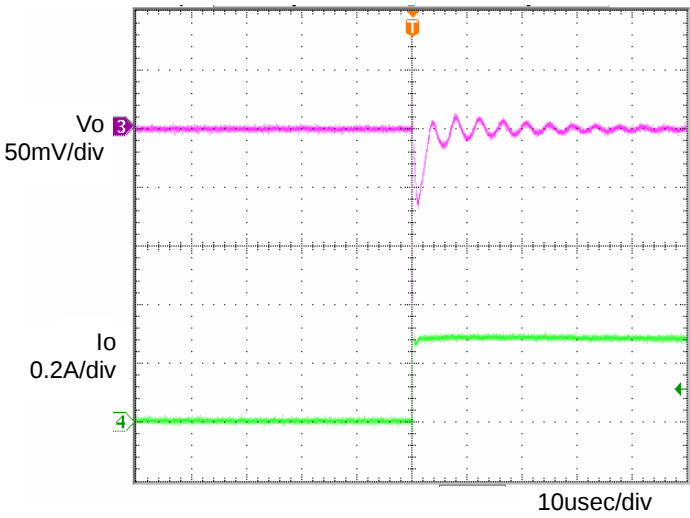


Figure 4.
Transient Response
(0→0.3A)
Co=1 μ F, Ta=25°C

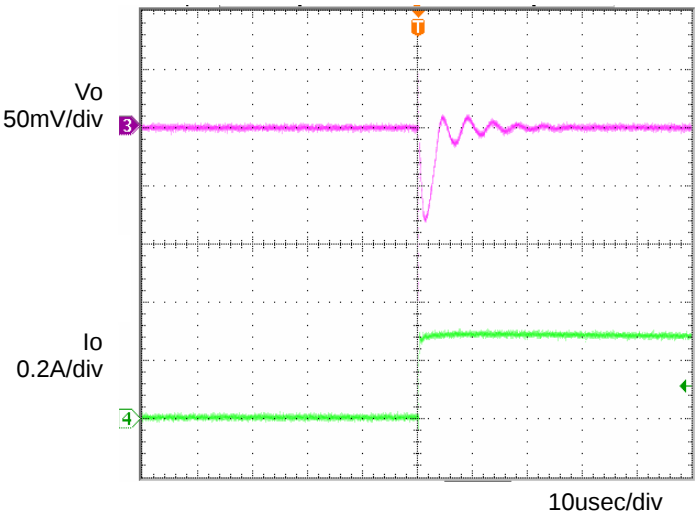


Figure 5.
Transient Response
(0→0.3A)
Co=1 μ F, Ta=105°C

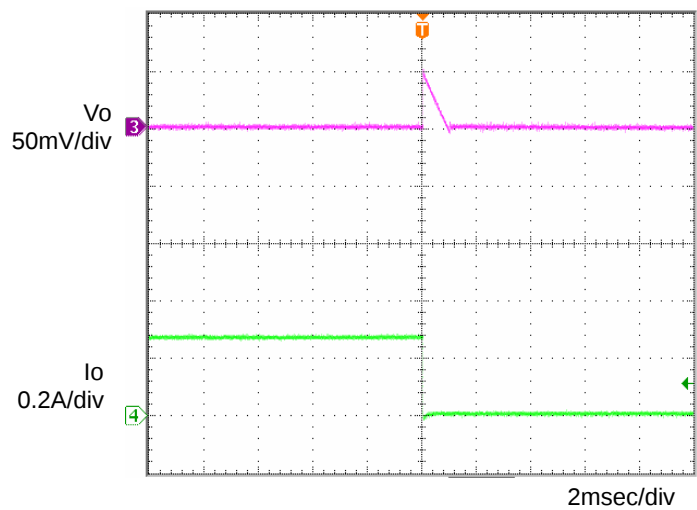


Figure 7.
Transient Response
(0.3→0A)
Co=1μF, Ta=25°C

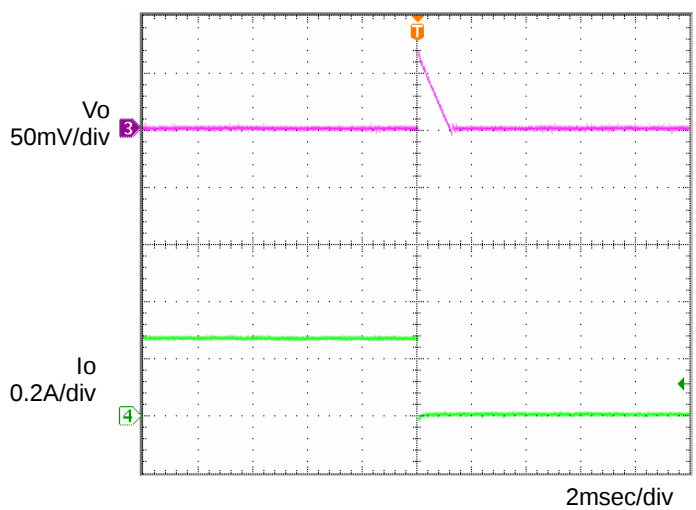


Figure 8.
Transient Response
(0.3→0A)
Co=1μF, Ta=105°C

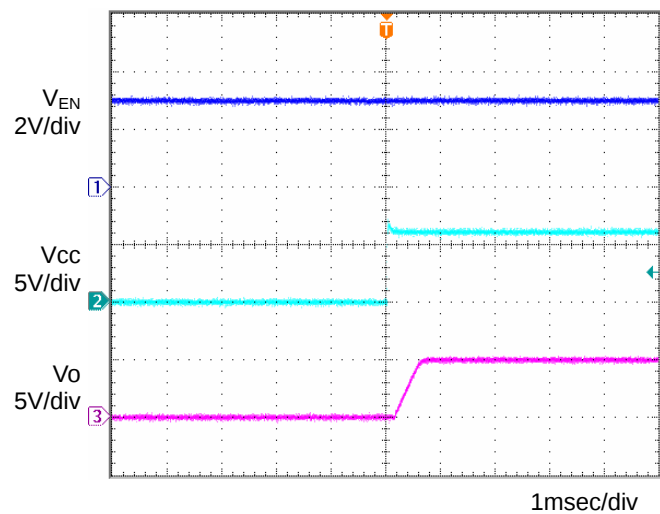
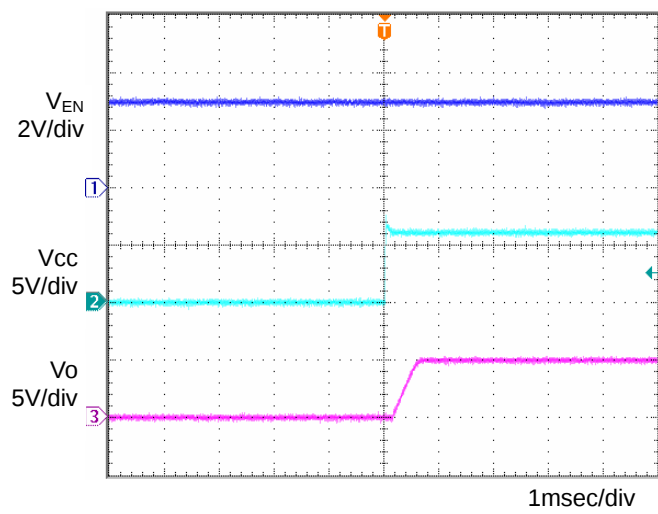


Figure 9.
Input sequence 1
Co=1μF, Ta=-40°C



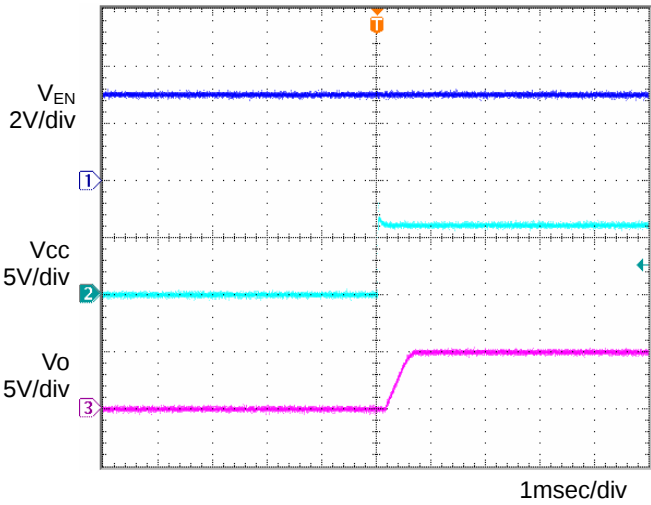


Figure 11.
Input sequence 1
 $C_o=1\mu F, T_a=105^{\circ}C$

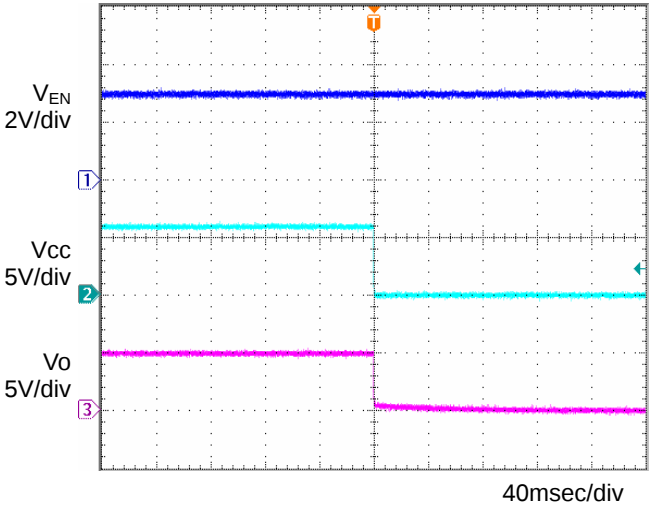
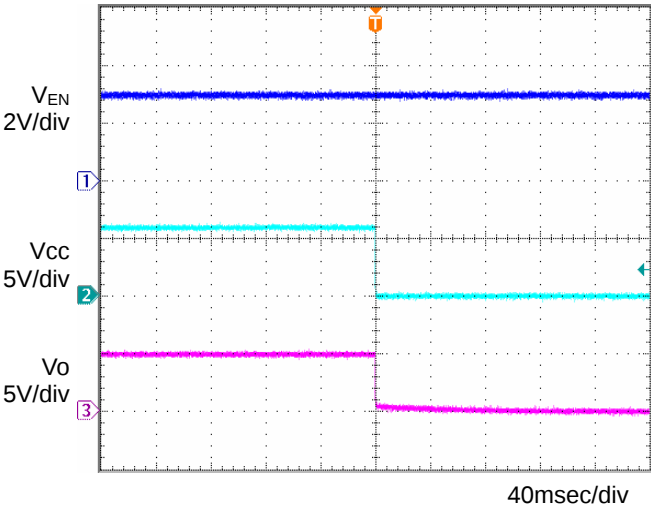


Figure 12.
OFF sequence 1
 $C_o=1\mu F, T_a=-40^{\circ}C$



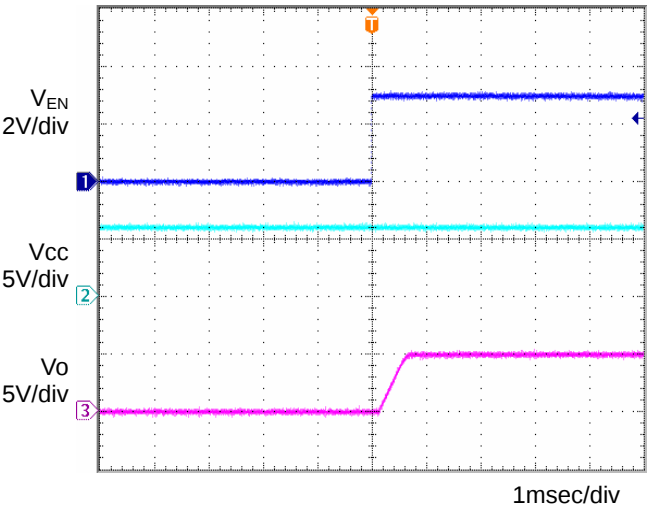


Figure 15.
Input sequence 2
 $C_o=1\mu F, T_a=-40^{\circ}C$

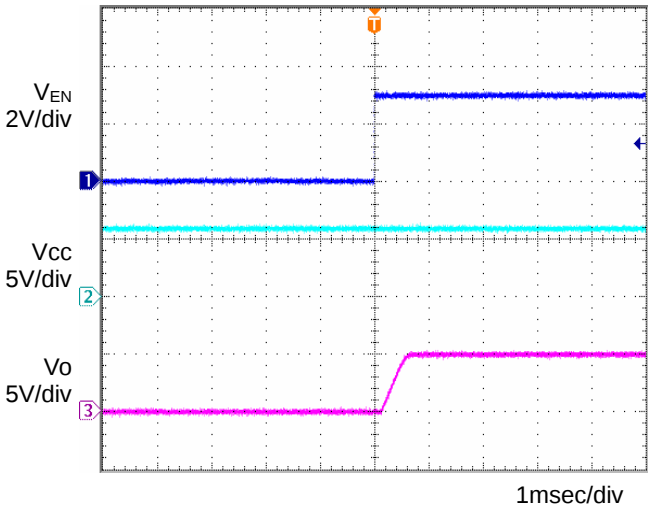
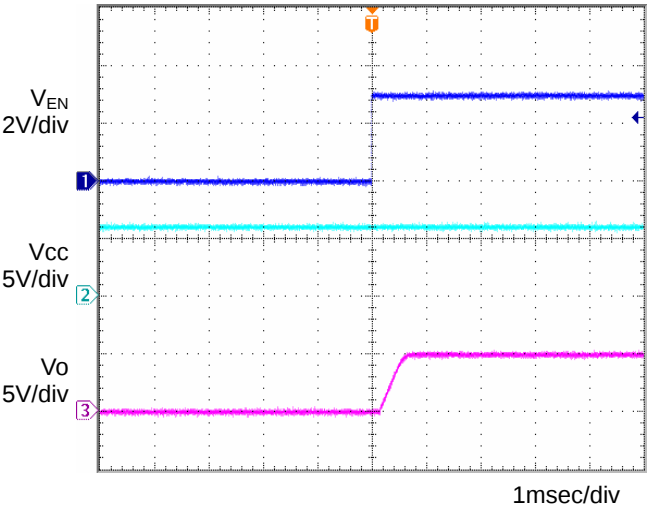


Figure 16.
Input sequence 2
 $C_o=1\mu F, T_a=25^{\circ}C$



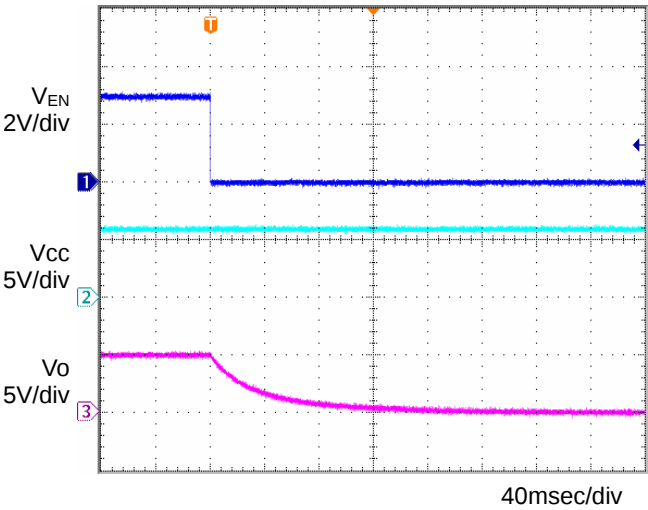


Figure 19.
OFF sequence 2
 $C_o = 1\mu\text{F}$, $T_a = 25^\circ\text{C}$

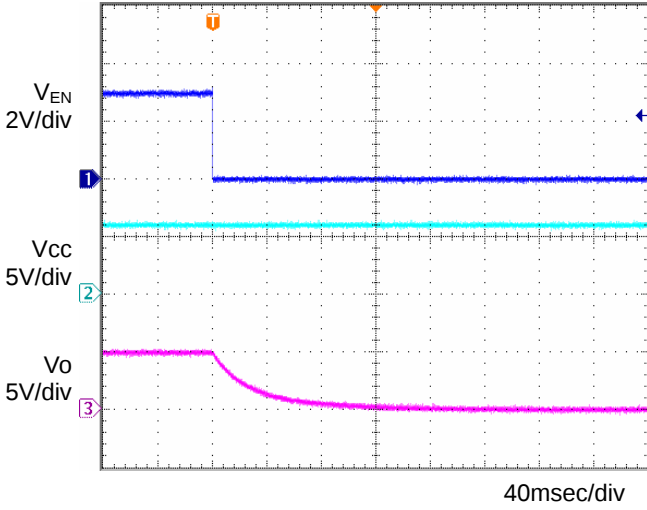
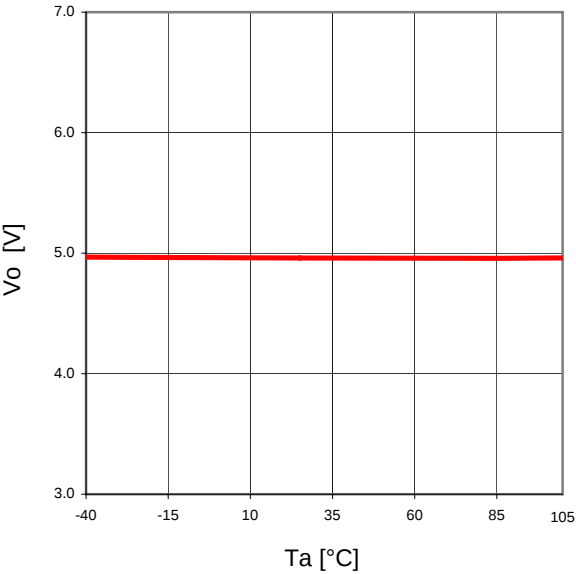


Figure 20.
OFF sequence 2
 $C_o = 1\mu\text{F}$, $T_a = 105^\circ\text{C}$



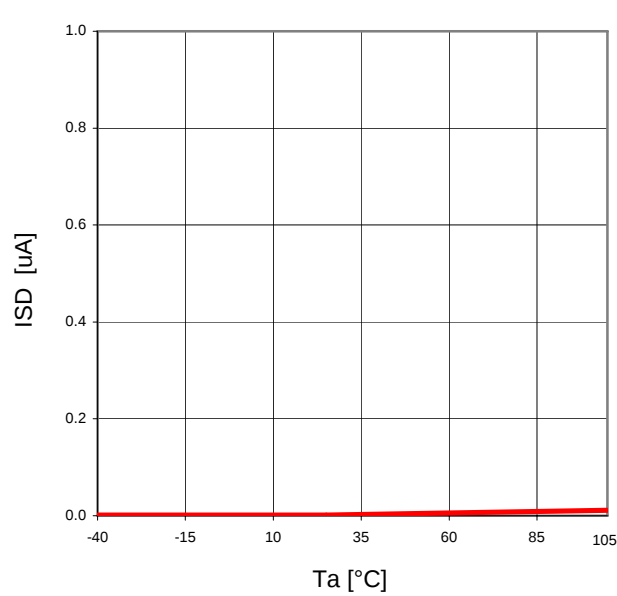
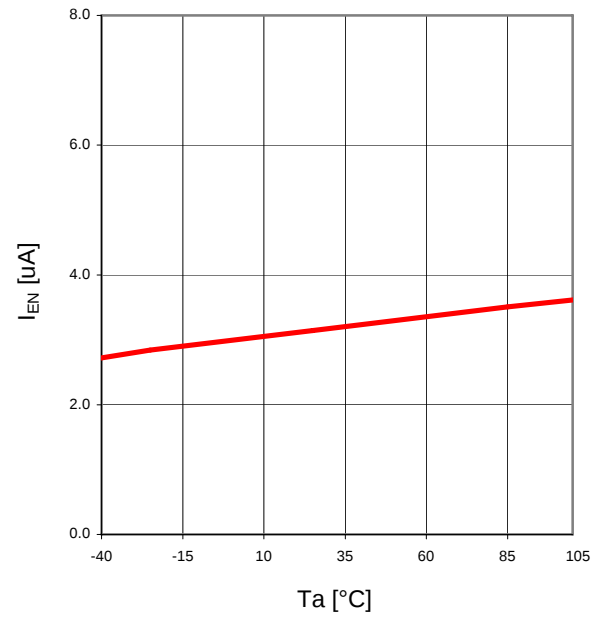


Figure 23.
Ta-ISD
(VEN=0V)



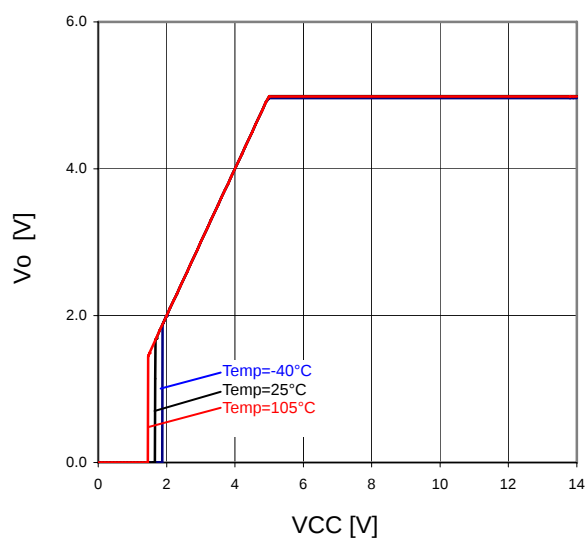
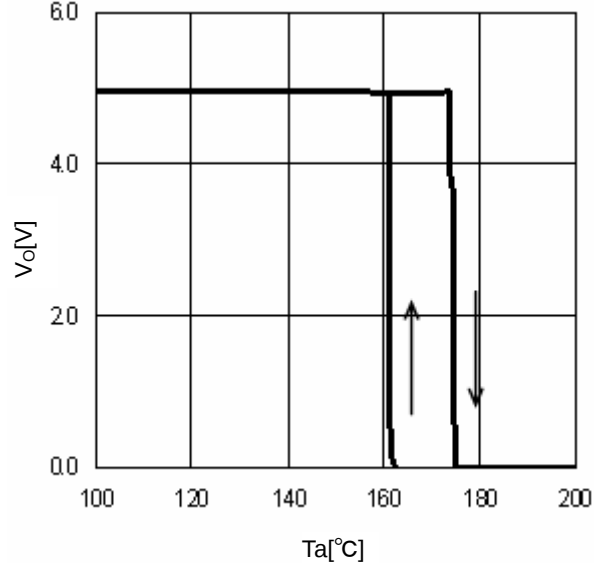


Figure 27.
Vcc-Vo
($I_o=0\text{mA}$)



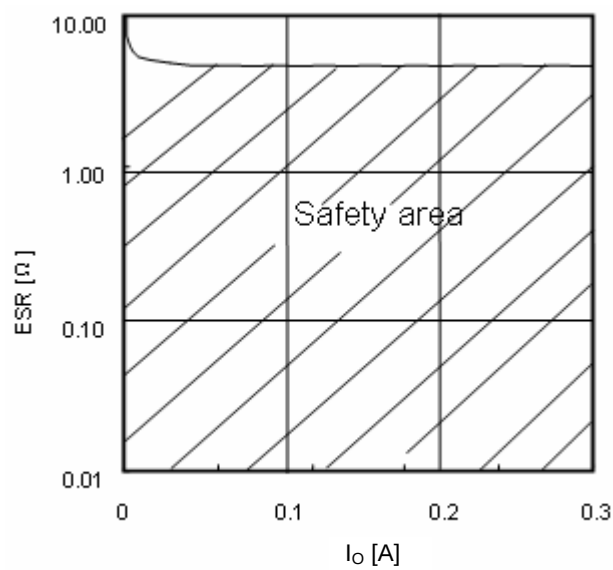


Figure 31.
Operation Safety area

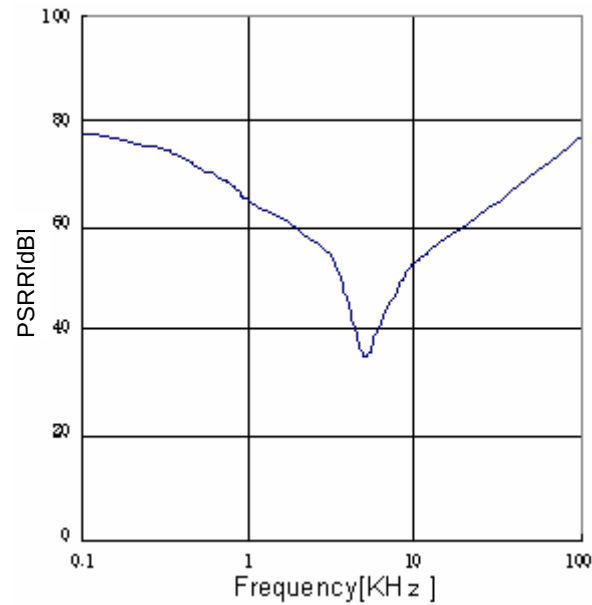
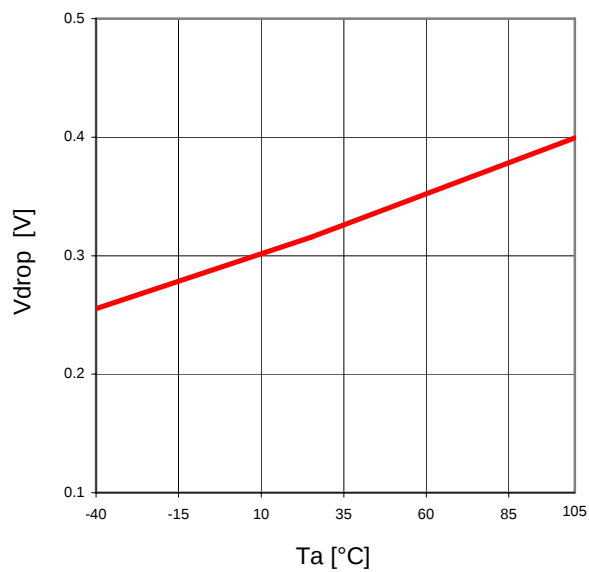


Figure 32.
PSRR(Io=0mA)



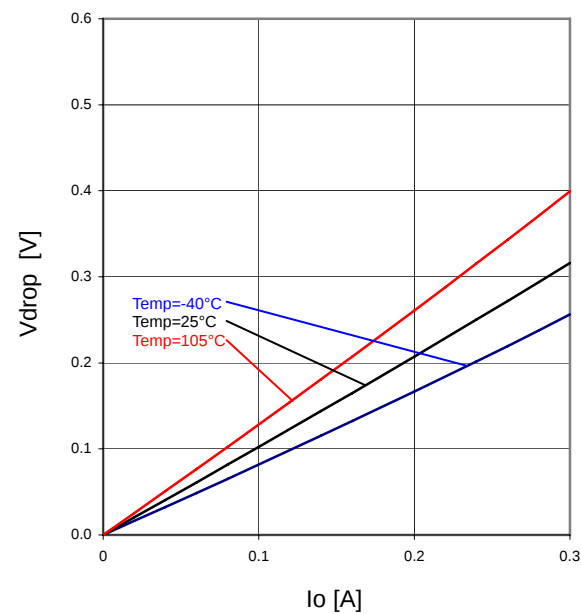
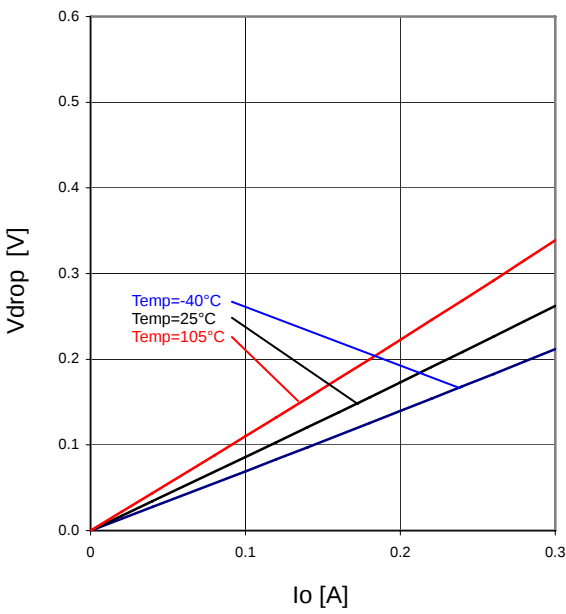
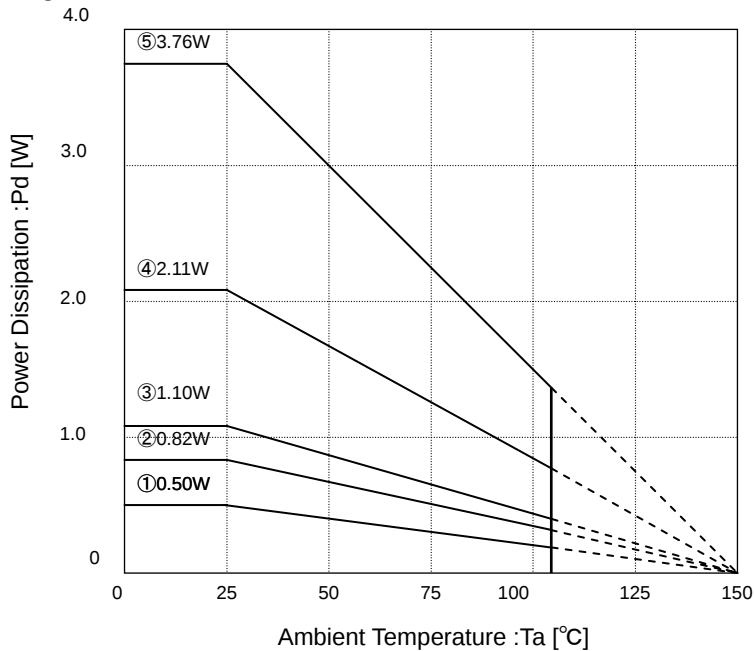


Figure 35.
Minimum dropout Voltage 2
(V_{CC}=6.0V)



●Power Dissipation

◎HTSOP-J8



Measure condition: mounted on a ROHM board, and IC

Substrate size: 70mm × 70mm × 1.6mm
(Substrate with thermal via)

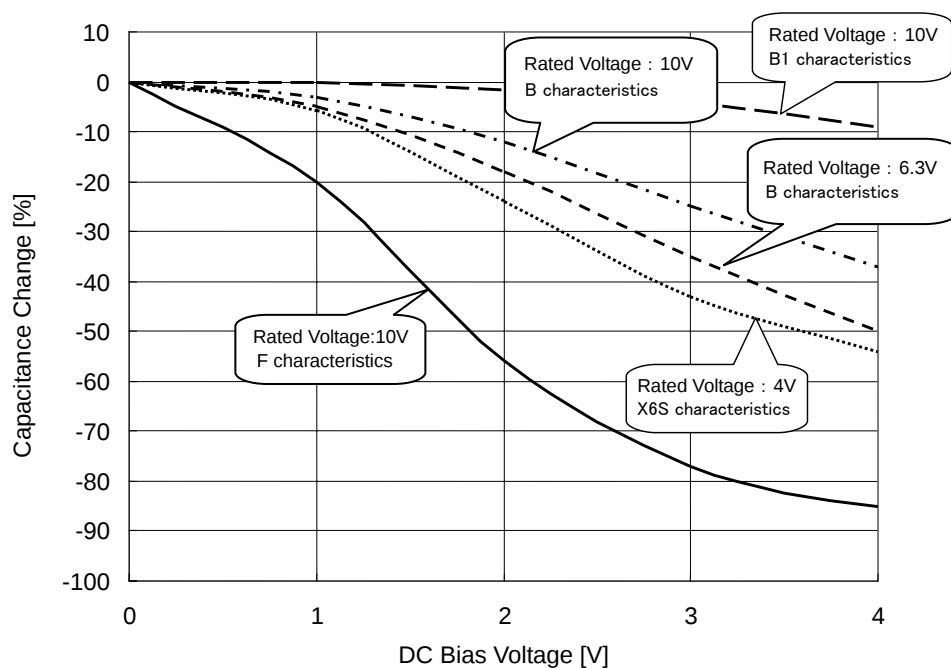
• Solder the substrate and package reverse exposure heat radiation part

●Input-to-Output Capacitor

It is recommended that a capacitor is placed nearby pin between Input pin and GND, output pin and GND.

A capacitor, between input pin and GND, is valid when the power supply impedance is high or drawing is long. Also as for a capacitor, between output pin and GND, the greater the capacity, more sustainable the line regulation and it makes improvement of characteristics by load change. However, please check by mounted on a board for the actual application. Ceramic capacitor usually has difference, thermal characteristics and series bias characteristics, and moreover capacity decreases gradually by using conditions.

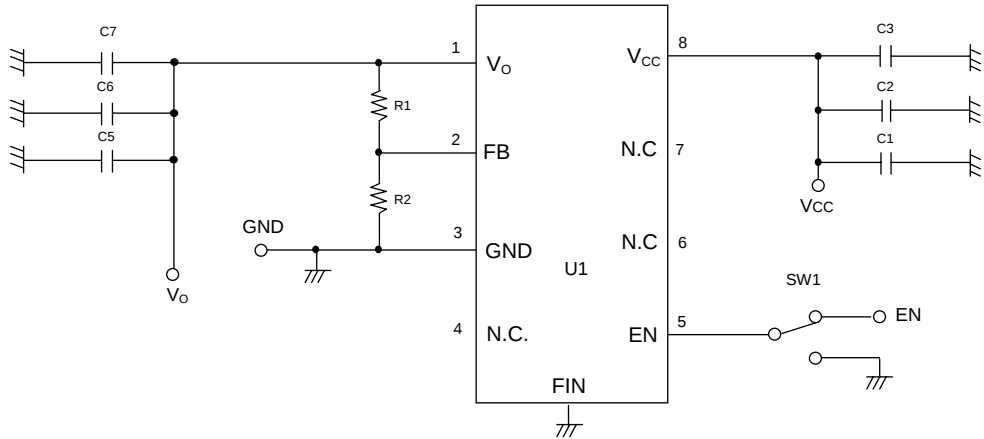
For more detail, please be sure to inquire the manufacturer, and select the best ceramic capacitor.



Ceramic capacitor capacity – DC bias characteristics
(Characteristics example)

●Equivalent Series Resistance ESR (ceramic capacitor etc.)

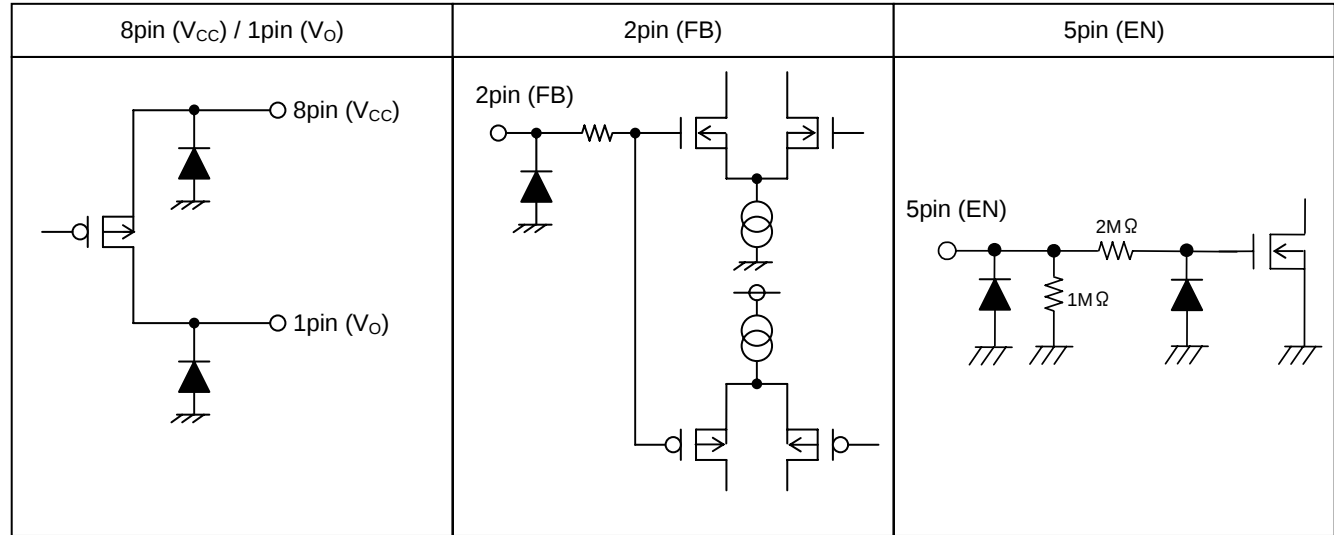
●Evaluation Board Circuit



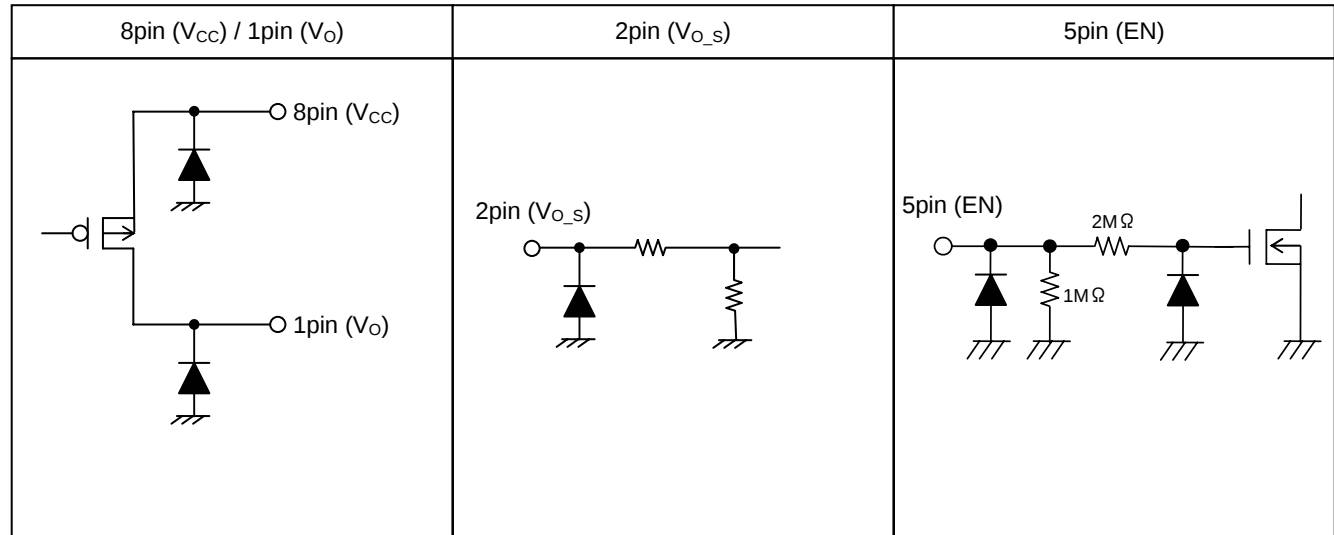
●Evaluation Board Parts List

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1	43kΩ	MCR01PZPZF4302	ROHM	C4	-	-	-
R2	8.2kΩ	MCR01PZPZF8201	ROHM	C5	1μF	CM105X7R105K16AB	KYOCERA
R3	-	-	-	C6			
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	1μF	CM105B105K16A	KYOCERA				

●I/O Equivalent Circuits (Output Voltage Vairable type)



●I/O Equivalent Circuits (Output Voltage Fixed type)



●Operational Notes

(1). Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2). Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3). Power supply lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4). GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

(5). Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(6). Inter-pin shorts and mounting errors

(11). Regarding input pin of the IC

This monolithic IC contains P⁺ isolation and P substrate layers between adjacent elements in order to keep them isolated.

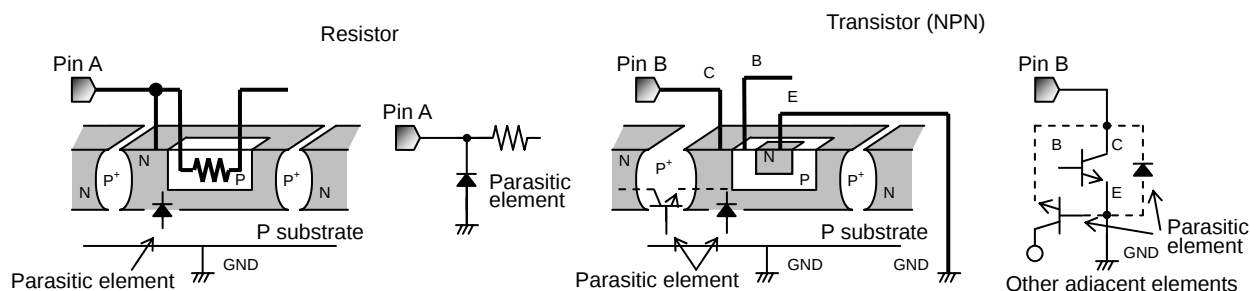
P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

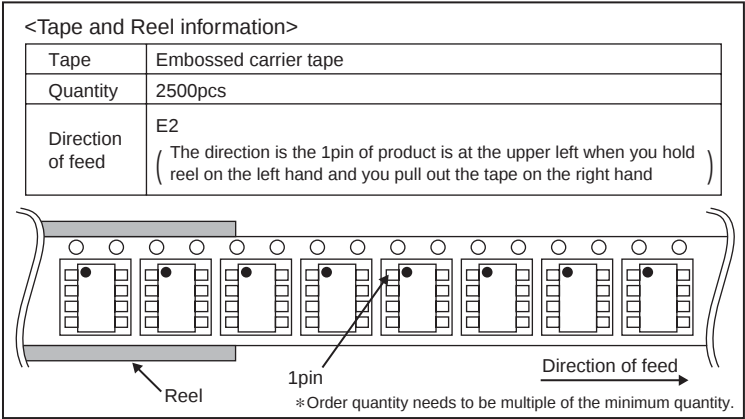
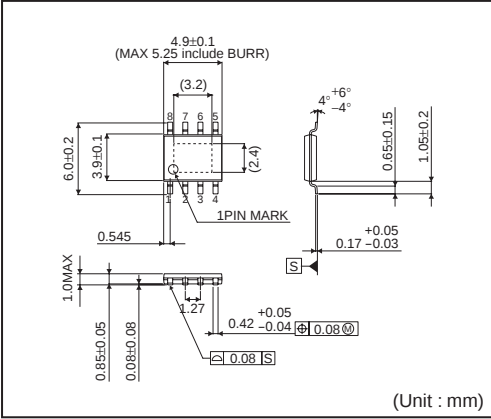
Parasitic diodes can occur inevitable in the structure of the IC.

The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND(P substrate) voltage to an input pin, should not be used.



●Physical Dimension Tape and Reel Information

HTSOP-J8



●Revision History

Date	Revision	Changes
31.Aug.2012	001	New Release

Notice

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1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive

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- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

