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CY39C603

Phase Dimmable PSR LED Driver IC for LED Lighting

Description

CY39C603 is a Primary Side Regulation (PSR) LED driver IC for LED lighting. Using the information of the primary peak current and the transformer-energy-zero time, it is able to deliver a well regulated current to the secondary side without using an opto-coupler in an isolated flyback topology. Operating in critical conduction mode, a smaller transformer is required. In addition, CY39C603 has a built-in phase dimmable circuit and can constitute flicker less lighting systems for phase dimming with low-component count. It is most suitable for the general lighting applications, for example replacement of commercial and residential incandescent lamps.

Features

- PSR topology in an isolated flyback circuit
- High power factor (>0.9 : without dimmer) in Single Conversion
- High efficiency (>80 % : without dimmer) and low EMI by detecting transformer zero energy
- Built-in phase dimmable circuit
  - Dimming curve based on conduction angle
  - Dimmer hold current control
- Highly reliable protection functions
  - Under voltage lock out (UVLO)
  - Over voltage protection (OVP)
  - Over current protection (OCP)
  - Over temperature protection (OTP)
- Switching frequency setting : 30 kHz to 133 kHz
- Input voltage range VDD : 9 V to 20 V
- Input voltage for LED lighting applications : AC110V_{RMS}
- Output power range for LED lighting applications : 15 W to 50 W
- Package : SOP-14 (5.30 mm × 10.15 mm × 2.25 mm [Max])

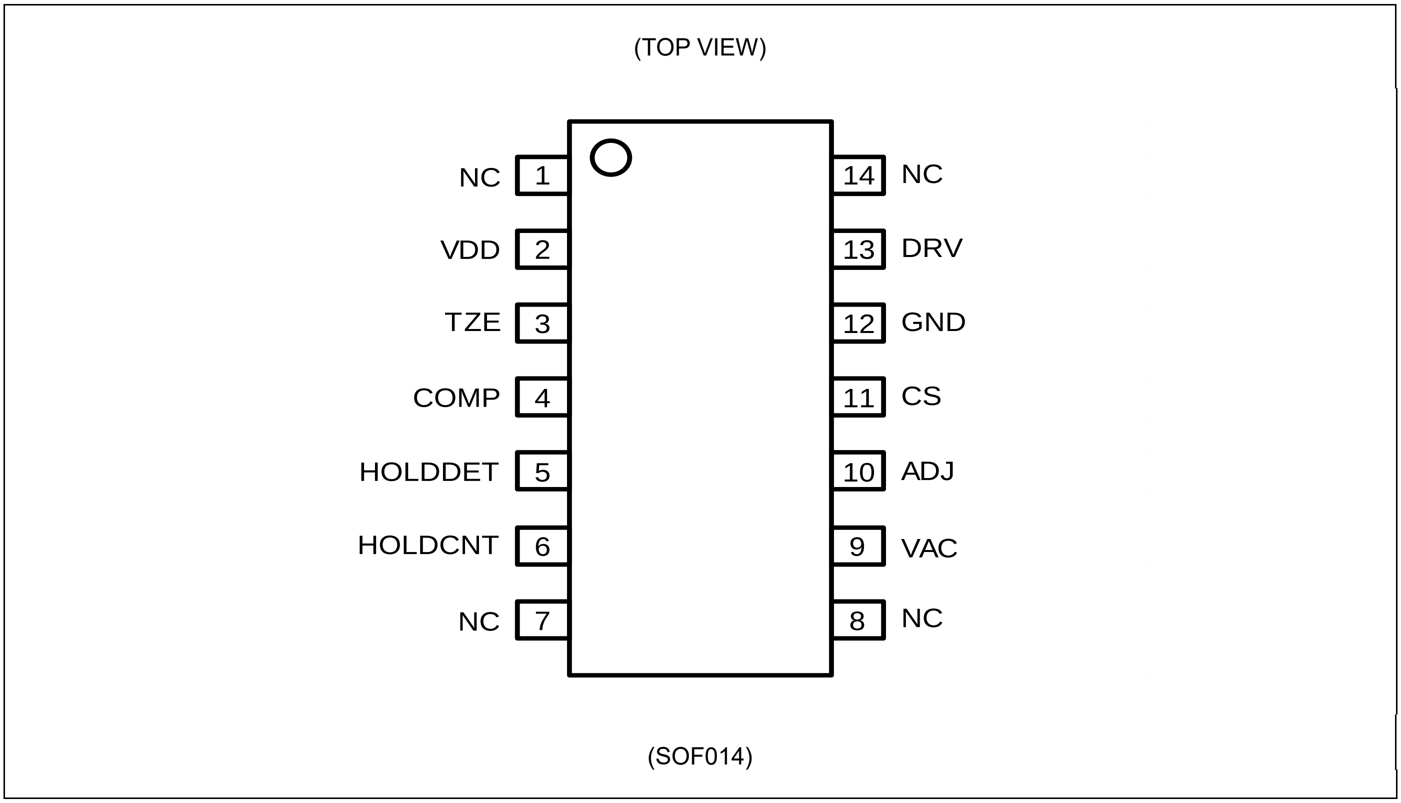
Applications

- Phase dimmable (Leading/Trailing) LED lighting
- LED lighting

Contents

1. Pin Assignment

Figure 1-1 Pin Assignment



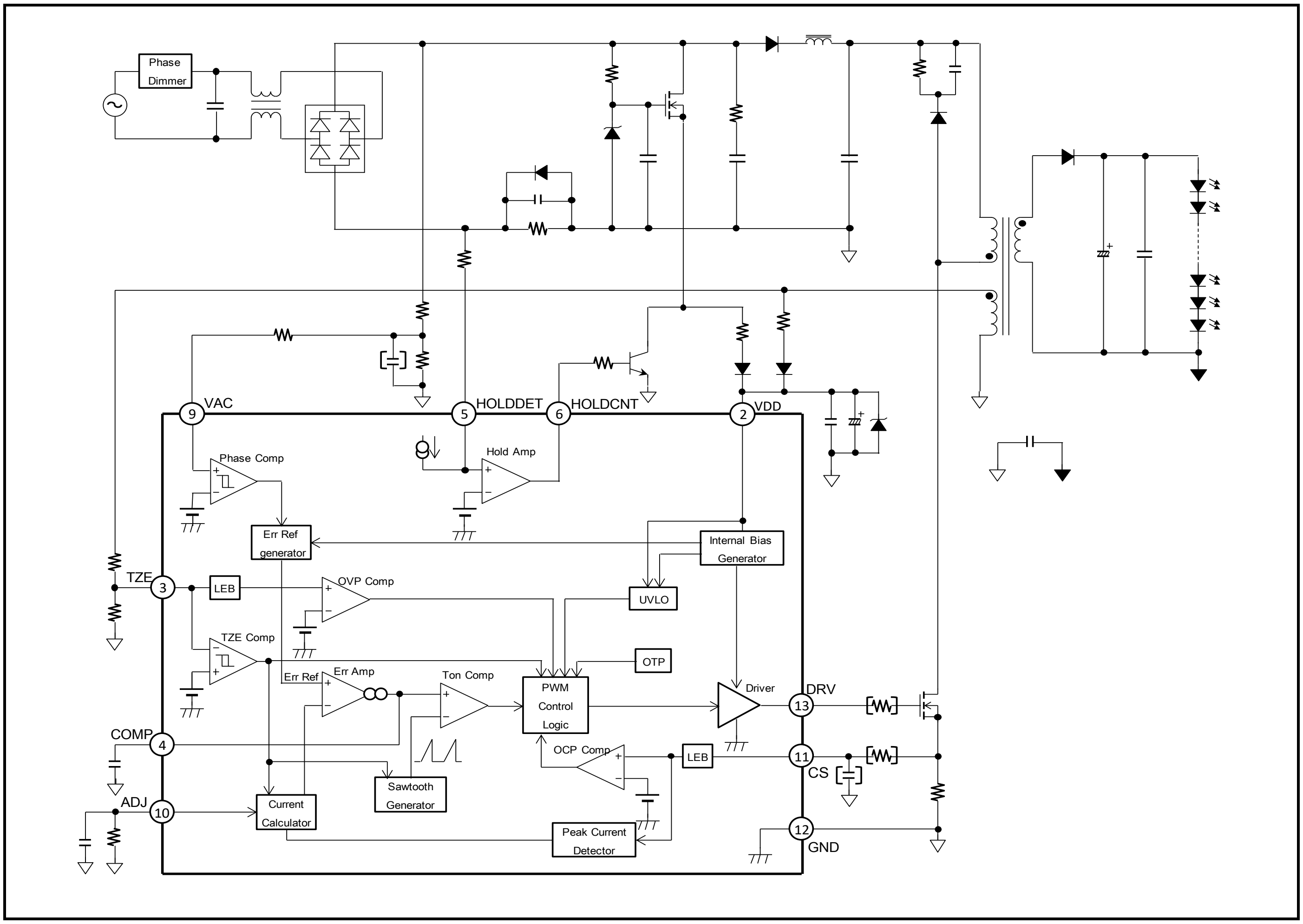
2. Pin Descriptions

Table 2-1 Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	NC	-	Not used. Leave this pin open.
2	VDD	-	Power supply pin.
3	TZE	I	Transformer Zero Energy detecting pin.
4	COMP	O	External Capacitor connection pin for the compensation.
5	HOLDDET	I	Phase Dimmer current detecting pin.
6	HOLDCNT	O	External BIP base current control pin.
7	NC	-	Not used. Leave this pin open.
8	NC	-	Not used. Leave this pin open.
9	VAC	I	Phase Dimmer conduction angle detecting pin.
10	ADJ	O	Pin for adjusting the switch-on timing.
11	CS	I	Pin for detecting peak current of transformer primary winding.
12	GND	-	Ground pin.
13	DRV	O	External MOSFET gate connection pin.
14	NC	-	Not used. Leave this pin open.

3. Block Diagram

Figure 3-1 Block Diagram (Isolated Flyback Application)



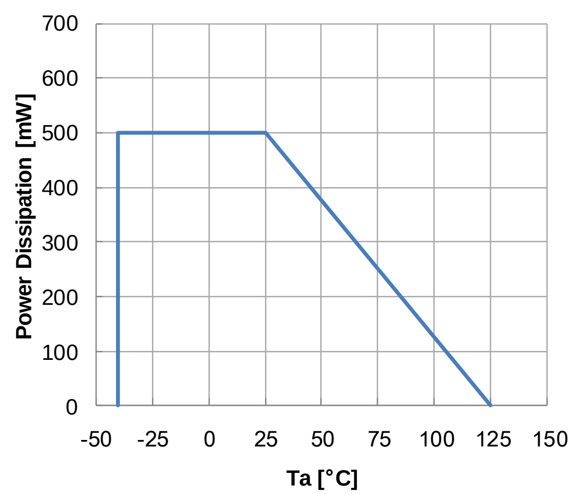
4. Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power Supply Voltage	V_{VDD}	VDD pin	-0.3	+25	V
Input Voltage	V_{CS}	CS pin	-0.3	+6.0	V
	V_{TZE}	TZE pin	-0.3	+6.0	V
	$V_{HOLDDET}$	HOLDDET pin	-0.3	+6.0	V
	V_{VAC}	VAC pin	-0.3	+6.0	V
Output Voltage	V_{DRV}	DRV pin	-0.3	+25	V
	$V_{HOLDCNT}$	HOLDCNT pin	-0.3	+6.0	V
Output Current	I_{ADJ}	ADJ pin	-1	-	mA
	I_{DRV}	DRV pin DC level	-50	+50	mA
	$I_{HOLDCNT}$	HOLDCNT pin	-400	-	μA
Power Dissipation	P_D	Ta ≤ +25°C	-	500(*1)	mW
Storage Temperature	T_{STG}	-	-55	+125	°C
ESD Voltage 1	V_{ESDH}	Human Body Model	-2000	+2000	V
ESD Voltage 2	V_{ESDC}	Charged Device Model	-1000	+1000	V

*1: The value when using two layers PCB.
Reference: θja (wind speed 0m/s): 200°C/W

Figure 4-1 Power Dissipation



WARNING:

1. Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

5. Recommended Operating Conditions

Table 5-1 Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
VDD pin Input Voltage	V_{VDD}	VDD pin	9	-	20	V
VAC pin Resistance	R_{VAC}	VAC pin	-	510	-	kΩ
TZE pin Resistance	R_{TZE}	TZE pin	50	-	200	kΩ
ADJ pin Resistance	R_{ADJ}	ADJ pin	9.3	-	185.5	kΩ
COMP pin Capacitance	C_{COMP}	COMP pin	-	4.7	-	µF
VDD pin Capacitance	C_{BP}	Set between VDD pin and GND pin	-	100	-	µF
Operating Junction Temperature	Tj	-	-40	-	+125	°C

WARNING:

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.
2. Any use of semiconductor devices will be under their recommended operating condition.
3. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
4. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

6. Electrical Characteristics

Table 6-1 Electrical Characteristics

(Ta = +25°C, V_{VDD} = 12V)

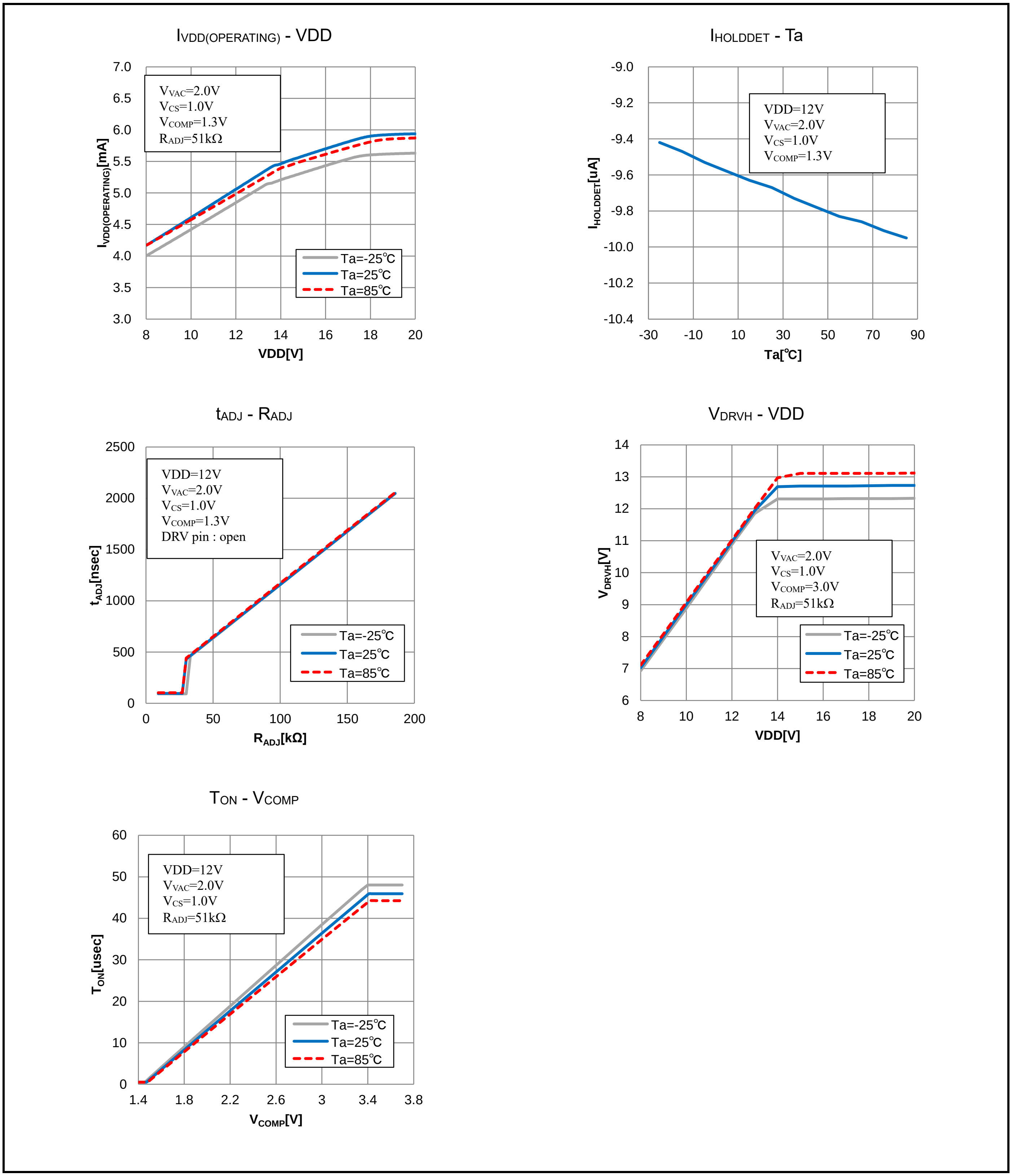
Parameter		Symbol	Pin	Condition	Value			Unit
					Min	Typ	Max	
UVLO	UVLO Turn-on threshold voltage	V_{TH}	VDD	-	9.6	10.2	10.8	V
	UVLO Turn-off threshold voltage	V_{TL}	VDD	-	7.55	8	8.5	V
	Startup current	I_{START}	VDD	V_{VDD} = 7V	-	65	160	μA
TRANSFORMER ZERO ENERGY DETECTION	Zero energy threshold voltage	V_{TZETL}	TZE	TZE = “H” to “L”	-	20	-	mV
	Zero energy threshold voltage	V_{TZETH}	TZE	TZE = “L” to “H”	0.6	0.7	0.8	V
	TZE clamp voltage	$V_{TZECLAMP}$	TZE	I_{TZE} = -10 μA	-200	-160	-100	mV
	OVP threshold voltage	V_{TZEOVP}	TZE	-	4.15	4.3	4.45	V
	OVP blanking time	$t_{OVPBLANK}$	TZE	-	0.6	1	1.7	μs
	TZE input current	I_{TZE}	TZE	V_{TZE} = 5V	-1	-	+1	μA
COMPENSATION	Source current	I_{SO}	COMP	V_{COMP} = 2V, V_{CS} = 0V, Conduction Angle = 165deg	-	-27	-	μA
	Trans conductance	gm	COMP	V_{COMP} = 2.5V, V_{CS} = 1V	-	96	-	μA/V
ADJUSTMENT	ADJ voltage	V_{ADJ}	ADJ	-	1.81	1.85	1.89	V
	ADJ source current	I_{ADJ}	ADJ	V_{ADJ} = 0V	-650	-450	-250	μA
	ADJ time	t_{ADJ}	TZE DRV	t_{ADJ} (R_{ADJ} = 51 kΩ) - t_{ADJ} (R_{ADJ} = 9.1 kΩ)	490	550	610	ns
	Minimum switching period	T_{SW}	TZE DRV	-	6.75	7.5	8.25	μs
CURRENT SENSE	OCP threshold voltage	V_{OCPTH}	CS	-	1.9	2	2.1	V
	OCP delay time	t_{OCPDLY}	CS	-	-	400	500	ns
	CS input current	I_{CS}	CS	V_{CS} = 5V	-1	-	+1	μA

(Ta = +25°C, V_{VDD} = 12V)

Parameter		Symbol	Pin	Condition	Value Min	Value Typ	Value Max	Unit
DRV	DRV high voltage	V_{DRVH}	DRV	VDD = 18V, I_{DRV} = -30 mA	7.6	9.4	-	V
	DRV low voltage	V_{DRVL}	DRV	VDD = 18V, I_{DRV} = 30 mA	-	130	260	mV
	Rise time	t_{RISE}	DRV	VDD = 18V, CLOAD = 1 nF	-	94	-	ns
	Fall time	t_{FALL}	DRV	VDD = 18V, CLOAD = 1 nF	-	16	-	ns
	Minimum on time	t_{ONMIN}	DRV	TZE trigger	300	500	700	ns
	Maximum on time	t_{ONMAX}	DRV	-	27	44	60	µs
	Minimum off time	t_{OFFMIN}	DRV	-	1	1.5	1.93	µs
	Maximum off time	t_{OFFMAX}	DRV	TZE = GND	37	46	55	µs
OTP	OTP threshold	T_{OTP}	-	Tj, temperature rising	-	150	-	°C
	OTP hysteresis	T_{OTPHYS}	-	Tj, temperature falling, degrees below T_{OTP}	-	25	-	°C
DIMMER CONDUCTION ANGLE DETECTION	Phase Comp threshold voltage	V_{PHTH1}	VAC	VAC = “L” to “H”	0.9	1.0	1.1	V
	Phase Comp threshold voltage	V_{PHTH2}	VAC	VAC = “H” to “L”	0.45	0.5	0.55	V
	Phase Comp hysteresis	V_{PHHYS}	VAC	-	-	0.5	-	V
TRIAC HOLD CURRENT CONTROL	HOLDDET input current	$I_{HOLDDET}$	HOLD DET	-	-10.09	-9.7	-9.32	µA
	Hold Amp threshold voltage	V_{HOLDTH}	HOLD CNT	-	375	400	425	mV
	HOLDCNT Maximum output voltage	V_{CNTOH}	HOLD CNT	$V_{HOLDDET}$ = 0.6V, R_{BASE} = 16 kΩ, V_{BASE} = 0.7V	3.4	-	-	V
	HOLDCNT Minimum output voltage	V_{CNTOL}	HOLD CNT	$V_{HOLDDET}$ = 0.2V, R_{BASE} = 16 kΩ, V_{BASE} = 0.7V			0.8	V
	HOLDCNT source current	I_{CNTSO}	HOLD CNT	$V_{HOLDDET}$ = 0.6V, R_{BASE} = 16 kΩ, V_{BASE} = 0.7V	-250	-200	-167	µA
POWER SUPPLY CURRENT	Power supply current	$I_{VDD(STATIC)}$	VDD	V_{VDD} = 20V, V_{TZE} = 1V	-	3.3	4	mA
		$I_{VDD(OPERATING)}$	VDD	V_{VDD} = 20V, Qg = 20 nC, f_{SW} = 133 kHz	-	5.9	-	mA

7. Standard Characteristics

Figure 7-1 Standard Characteristics



8. Function Explanations

8.1 LED Current Control by PSR(Primary Side Regulation)

CY39C603 regulates the average LED current (I_{LED}) by feeding back the information based on Primary Winding peak current (I_{P_PEAK}), Secondary Winding energy discharge time (T_{DIS}) and switching period (T_{SW}). Figure 8-1 shows the operating waveform in steady state. I_P is Primary Winding current and I_S is Secondary Winding current. I_{LED} as an average current of the Secondary Winding is described by the following equation.

$$I_{LED} = \frac{1}{2} \times I_{S\_PEAK} \times \frac{T_{DIS}}{T_{SW}}$$

Using I_{P_PEAK} and the transformer Secondary to Primary turns ratio (N_P/N_S), Secondary Winding peak current (I_{S_PEAK}) is described by the following equation.

$$I_{S\_PEAK} = \frac{N_P}{N_S} \times I_{P\_PEAK}$$

Therefore,

$$I_{LED} = \frac{1}{2} \times \frac{N_P}{N_S} \times I_{P\_PEAK} \times \frac{T_{DIS}}{T_{SW}}$$

CY39C603 detects T_{DIS} by monitoring the TZE pin and I_{P_PEAK} by monitoring the CS pin and then controls I_{LED}. An internal Err Amp sinks gm current proportional to I_{P_PEAK} from the COMP pin during T_{DIS} period. In steady state, since the average of the gm current is equal to internal reference current (I_{SO}), the voltage on the COMP pin (V_{COMP}) is nearly constant.

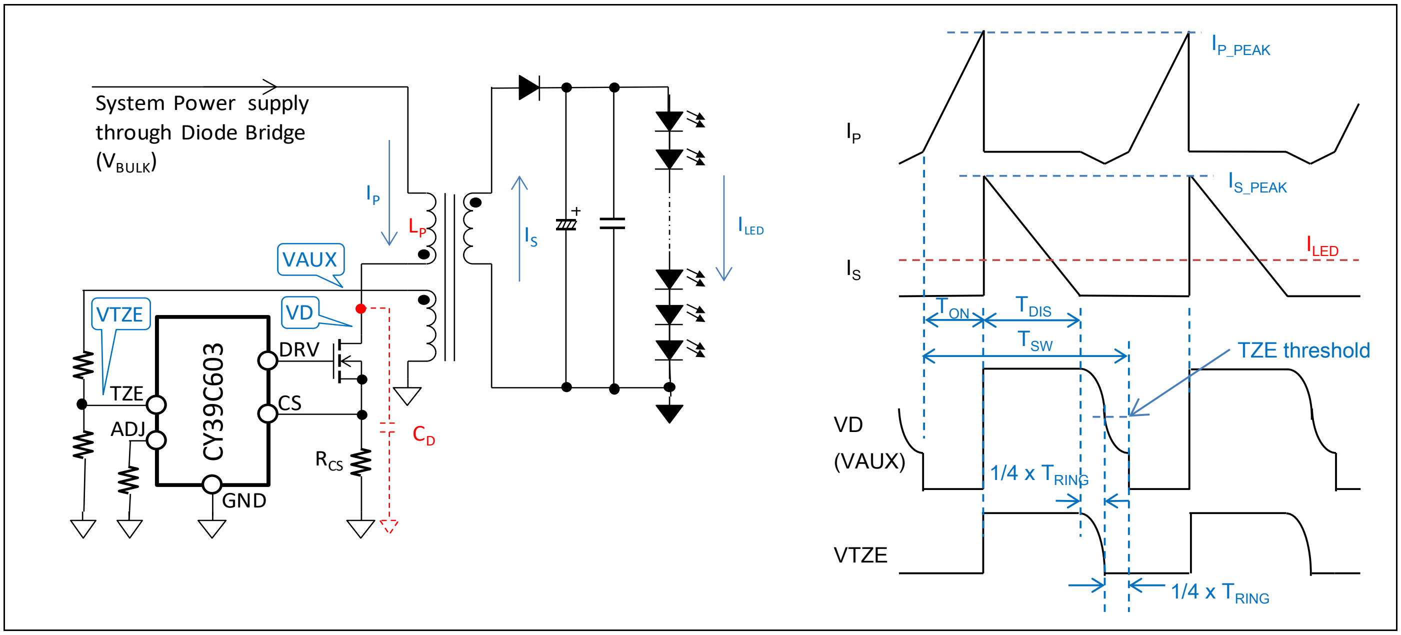
$$I_{P\_PEAK} \times R_{CS} \times gm \times T_{DIS} = I_{SO} \times T_{SW}$$

In above equation, gm is transconductance of the Err Amp and R_{CS} is a sense resistance.

Eventually, I_{LED} can be calculated by the following equation.

$$I_{LED} = \frac{1}{2} \times \frac{N_P}{N_S} \times \frac{I_{SO}}{gm} \times \frac{1}{R_{CS}}$$

Figure 8-1 LED Current Control Waveform



8.2 PFC (Power Factor Correction) Function

Switching on time (T_{ON}) is generated by comparing V_{COMP} with an internal sawtooth waveform (refer to Figure 3-1). Since V_{COMP} is slow varying with connecting an external capacitor (C_{COMP}) from the COMP pin to the GND pin, T_{ON} is nearly constant within an AC line cycle. In this state, I_{P_PEAK} is nearly proportional to the AC line voltage (V_{BULK}). It can bring the phase differences between the input voltage and the input current close to zero, so that high Power Factor can be achieved.

8.3 Phase Dimming Function

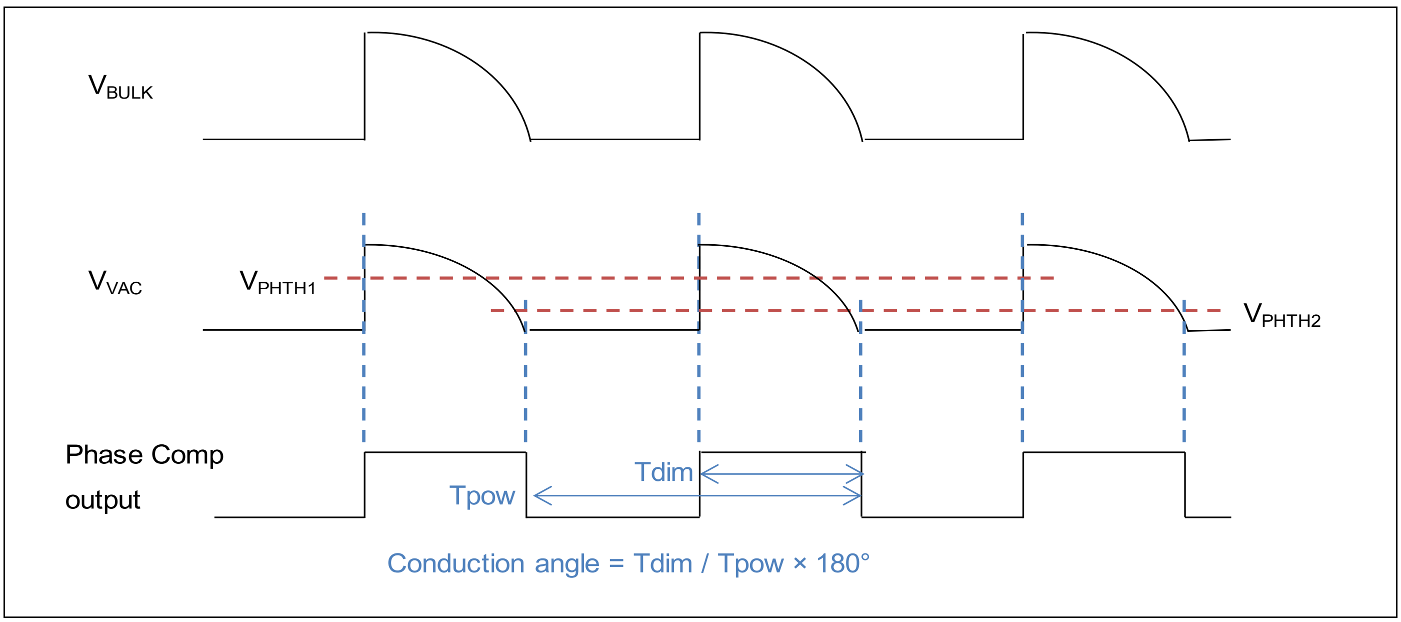
CY39C603 is compatible with both leading-edge dimmers (TRIAC dimming) and trailing-edge dimmers.

To realize the phase dimming, this device has two functions, dimmer conduction angle detect function for LED current control and TRIAC dimmer hold current control function.

Figure 8-2 shows how CY39C603 detects the conduction angle. V_{BULK} is scaled via a resistor divider connected to the VAC pin. The conduction angle is detected by monitoring the voltage on the VAC pin (V_{VAC}).

CY39C603 measures a half of power cycle period (Tpow) as duration between negative crossings of V_{VAC} and a Phase Comp threshold voltage (V_{PHTH2}). Dimmer-ON period (Tdim) is measured as duration between a positive crossing of V_{VAC} and another Phase Comp threshold voltage (V_{PHTH1}) and the following negative crossing. Conduction angle is defined as Tdim/Tpow × 180°.

Figure 8-2 Conduction Angle Detection Waveform



CY39C603 regulates LED current by changing a reference of Err Amp as a function of the conduction angle. Table 8-1 shows I_{LED} dimming ratio based on the conduction angle.

In addition, the initial I_{LED} ratio in Power–On state is 5%.

Table 8-1 I_{LED} Ratio Based on Conduction Angles

Conduction Angle	I_{LED} Ratio [%]
θ < 45deg	5
45deg ≤ θ < 90deg	(25/45) × θ -20
90deg ≤ θ < 135deg	(70/45) × θ -110
135deg ≤ θ	100

8.4 HOLD Current Control Function

The hold current control function prevents LEDs from flickering caused by shortage of hold current. The hold current (I_{HOLD}) is the minimum current required to flow through TRIAC dimmer in order to keep the TRIAC on (refer to Figure 8-3). In small conduction angle, since I_{LED} can be low, AC/DC Converter current (I_{BULK}) and TRIAC dimmer current (I_{TRIAC}) are reduced. Once I_{TRIAC} falls below I_{HOLD}, TRIAC goes off and this results in LED flickering. CY39C603 controls I_{TRIAC} larger than I_{HOLD} by adding the current (I_{BIP}) via a BIP transistor (M1) with sensing I_{TRIAC} and keeps the TRIAC on.

I_{TRIAC} is sensed with a resistor (R_S). A bypass diode (D_{BYPASS}) is used to clamp the voltage between R_S terminals (V_{RS}) and prevent the voltage on the HOLDDET pin ($V_{HOLDDET}$) from exceeding absolute maximum ratings. An offset resistor (R_{OFFSET}) is used to add an offset voltage to $V_{HOLDDET}$ and prevent $V_{HOLDDET}$ from the above ratings.

R_S is set as the following equation.

$$R_S = \frac{R_{OFFSET} \times I_{HOLDDET} - V_{HOLDTH}}{I_{TRIACMIN}}$$

where $I_{HOLDDET}$ is the current of the HOLDDET pin, V_{HOLDTH} is Hold Amp threshold voltage, and $I_{TRIACMIN}$ is minimum TRIAC current chosen by designers.

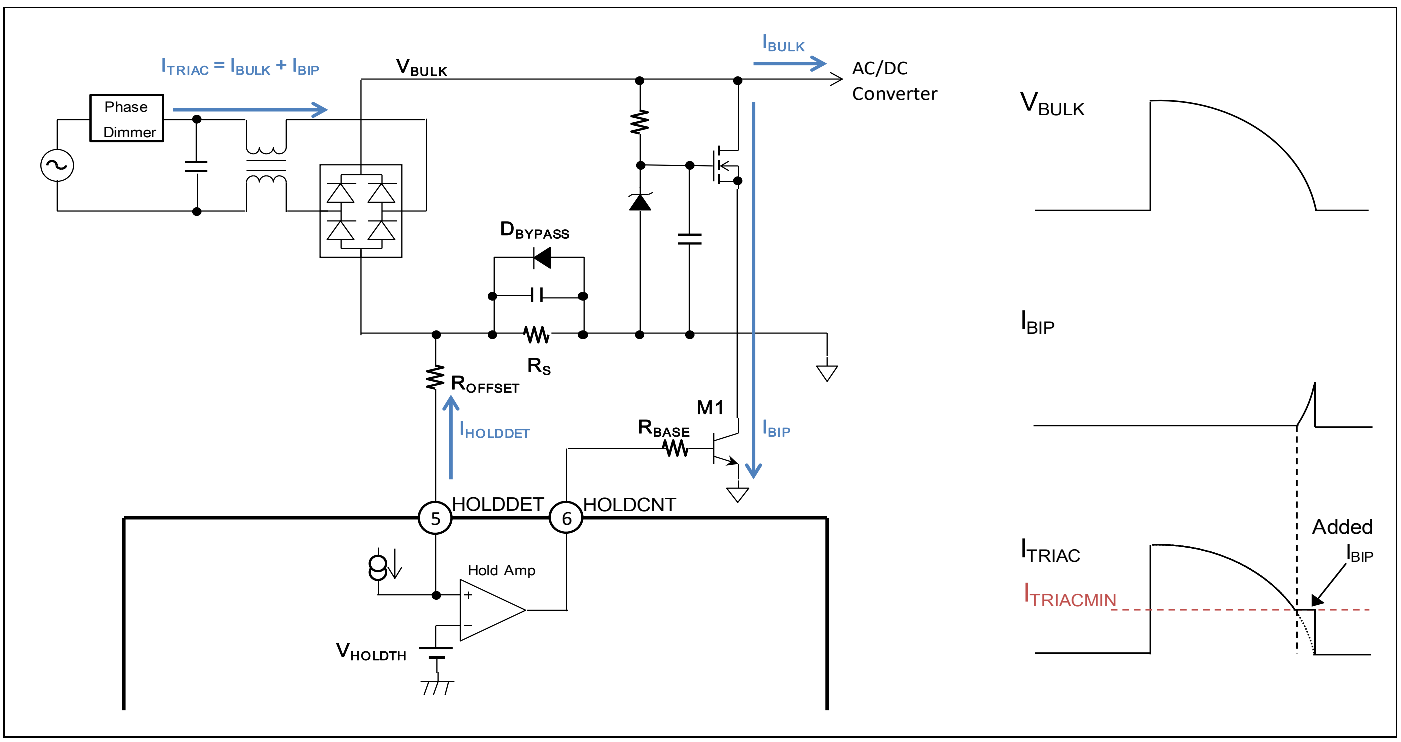
R_{OFFSET} is set as the following equation.

$$R_{OFFSET} > \frac{V_{BYPASSMAX} - 0.3V}{I_{HOLDDET}}$$

where $V_{BYPASSMAX}$ is the maximum forward voltage of D_{BYPASS}.

Hold Amp is designed only for driving BIP transistors. Connecting a resistor (R_{BASE}) between the HOLDCNT pin and M1 base terminal limits the maximum I_{BIP} value and clamp the rush current at TRIAC dimmer-on timing.

Figure 8-3 HOLD Current Control Waveform



8.5 Power-On Sequence

When the AC line voltage is supplied, V_{BULK} is powered from the AC line through a diode bridge, and the VDD pin is charged from V_{BULK} through an external source-follower BiasMOS.(Figure 8-4 red path)

When the VDD pin is charged up and the voltage on the VDD pin (V_{VDD}) rises above the UVLO threshold voltage, an internal Bias circuit starts operating, and CY39C603 starts the conduction angle detection (refer to 8.3). After the UVLO is released, this device enables switching and is operating in a forced switching mode (T_{ON} = 1.5 μs, T_{OFF} = 78 μs to 320 μs). When the voltage on the TZE pin reaches the Zero energy threshold voltage (V_{TZETH} = 0.7V), CY39C603 enters normal operation mode. After the switching begins, the VDD pin is also charged from Auxiliary Winding through an external diode (DBIAS).(Figure 8-4 blue path)

During non-conduction period V_{VDD} is not supplied from V_{BULK} or Auxiliary Winding. It is necessary to set an appropriate capacitor of the VDD pin in order to keep V_{VDD} above the UVLO threshold voltage in this period. An external diode (D1) between BiasMOS and the VDD pin is used to prevent discharge from the VDD pin to V_{BULK} at zero cross points of the AC line voltage.

Figure 8-4 VDD Supply Path at Power-On

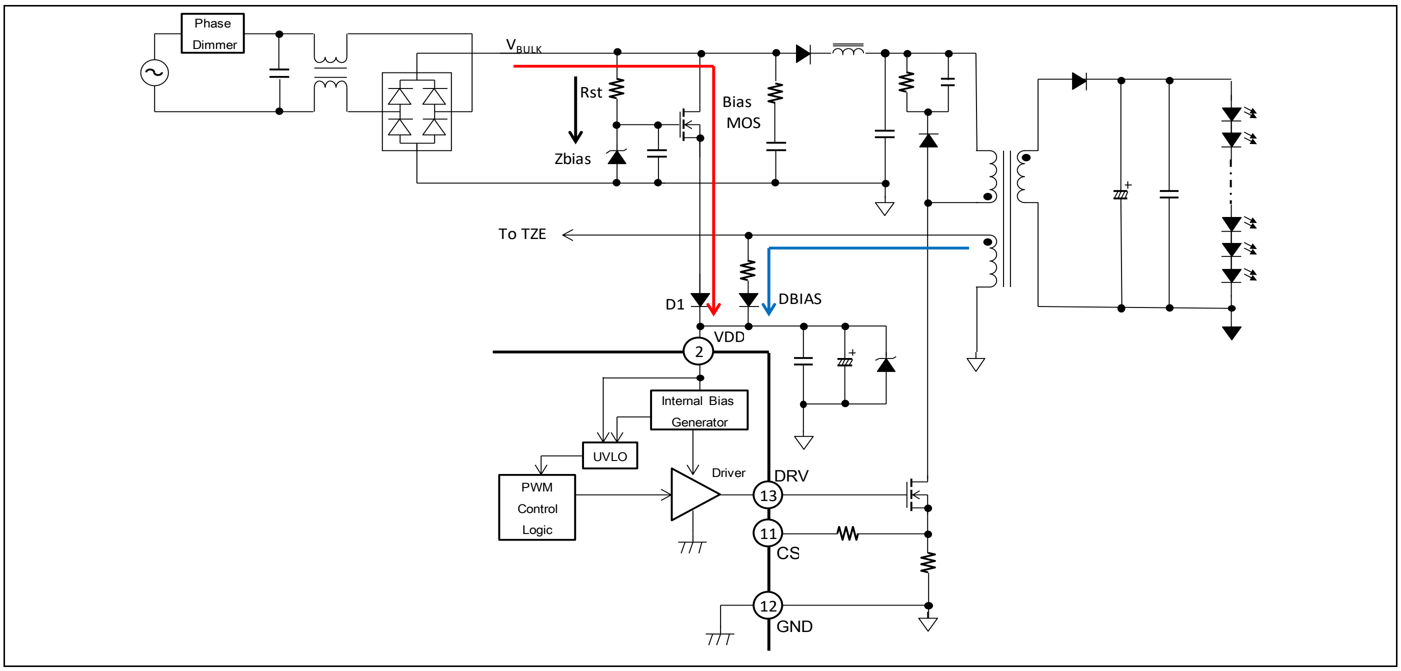
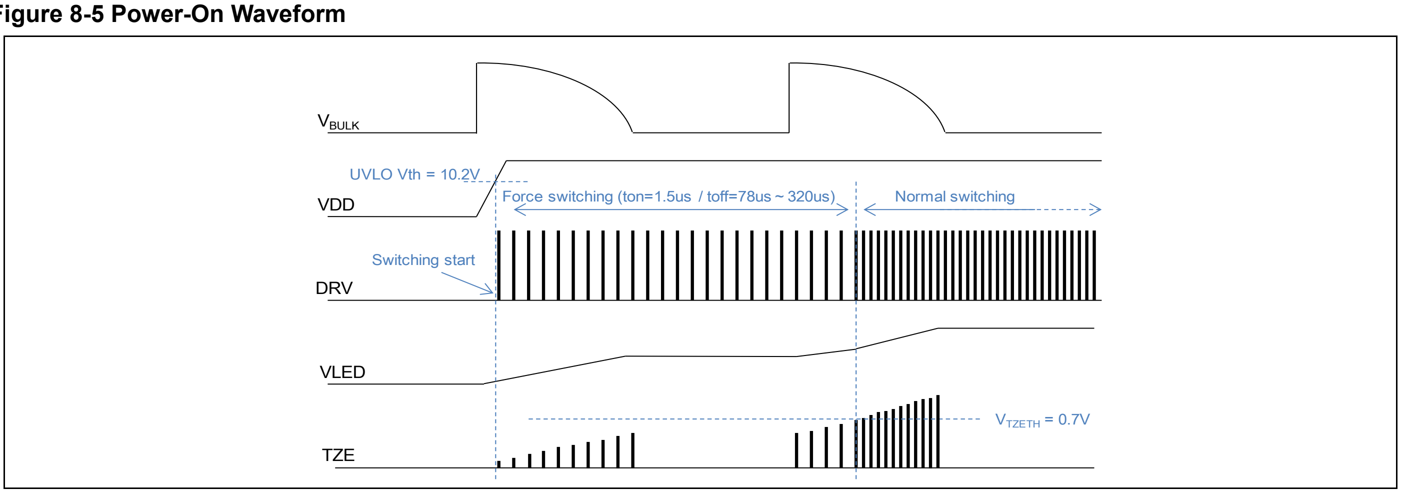


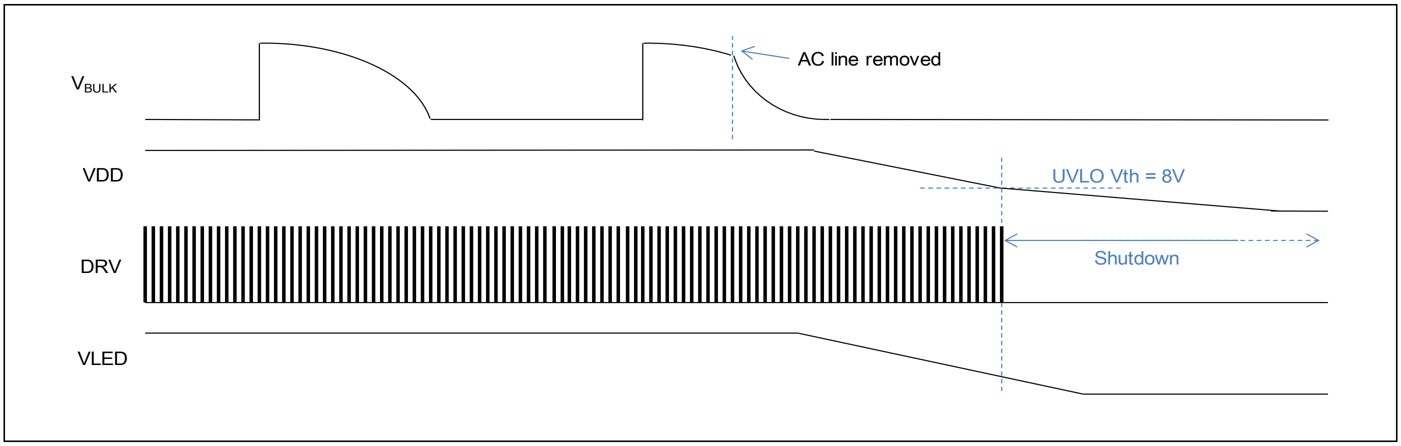
Figure 8-5 Power-On Waveform



8.6 Power-Off Sequence

After the AC line voltage is removed, V_{BULK} is discharged by switching operation and the Hold current circuit. Since any Secondary Winding current does not flow, I_{LED} is supplied only from output capacitors and decreases gradually. V_{VDD} also decreases because there is no current supply from both Auxiliary Winding and V_{BULK}. When V_{VDD} falls below the UVLO threshold voltage, CY39C603 shuts down.

Figure 8-6 Power-Off Waveform



8.7 I_{P_PEAK} Detection Function

CY39C603 detects Primary Winding peak current (I_{P_PEAK}) of Transformer. I_{LED} is set by connecting a sense resistance (R_{CS}) between the CS pin and the GND pin. Maximum I_{P_PEAK} ($I_{P\_PEAKMAX}$) limited by Over Current Protection (OCP) can also be set with the resistance.

Using the Secondary to Primary turns ratio (N_P/N_S) and I_{LED}, R_{CS} is set as the following equation (refer to 8.1).

$$R_{CS} = \frac{N_P}{N_S} \times \frac{0.132}{I_{LED}}$$

In addition, using the OCP threshold voltage (V_{OCPTH}) and R_{CS}, $I_{P\_PEAKMAX}$ is calculated with the following equation.

$$I_{P\_PEAKMAX} = \frac{V_{OCPTH}}{R_{CS}}$$

8.8 Zero Voltage Switching Function

CY39C603 has built-in zero voltage switching function to minimize switching loss of the external switching MOSFET. This device detects a zero crossing point through a resistor divider connected from the TZE pin to Auxiliary Winding. A zero energy detection circuit detects a negative crossing point of the voltage on the TZE pin to Zero energy threshold voltage (V_{TZETL}). On-timing of switching MOSFET is decided with waiting an adjustment time (t_{ADJ}) after the negative crossing occurs.

t_{ADJ} is set by connecting an external resistance (R_{ADJ}) between the ADJ pin and the GND pin. Using Primary Winding inductance (L_P) and the parasitic drain capacitor of switching MOSFET (C_D), t_{ADJ} is calculated with the following equation.

$$t_{ADJ} = \frac{\pi\sqrt{L_P \times C_D}}{2}$$

Using t_{ADJ}, R_{ADJ} is set as the following equation.

$$R_{ADJ}[k\Omega] = 0.0927 \times t_{ADJ}[ns]$$

8.9 Protection Functions

Under Voltage Lockout Protection (UVLO)

The under voltage lockout protection (UVLO) prevents IC from a malfunction in the transient state during V_{VDD} startup and a malfunction caused by a momentary drop of V_{VDD}, and protects the system from destruction/deterioration. An UVLO comparator detects the voltage decrease below the UVLO threshold voltage on the VDD pin, and then the DRV pin is turned to “L” and the switching stops. CY39C603 automatically returns to normal operation mode when V_{VDD} increases above the UVLO threshold voltage.

Over Voltage Protection (OVP)

The over voltage protection (OVP) protects Secondary side components from an excessive stress voltage. If the LED is disconnected, the output voltage of Secondary Winding rises up. The output overvoltage can be detected by monitoring the TZE pin. During Secondary Winding energy discharge time, V_{TZE} is proportional to V_{AUX} and the voltage of Secondary Winding (refer to 8.1). When V_{TZE} rises higher than the OVP threshold voltage for 3 continues switching cycles, the DRV pin is turned to “L”, and the switching stops (latch off). When V_{VDD} drops below the UVLO threshold voltage, the latch is removed.

Over Current Protection (OCP)

The over current protection (OCP) prevents inductor or transformer from saturation. The drain current of the external switching MOSFET is limited by OCP. When the voltage on the CS pin reaches the OCP threshold voltage, the DRV pin is turned to “L” and the switching cycle ends. After zero crossing is detected on the TZE pin again, the DRV pin is turned to “H” and the next switching cycle begins.

Over Temperature Protection (OTP)

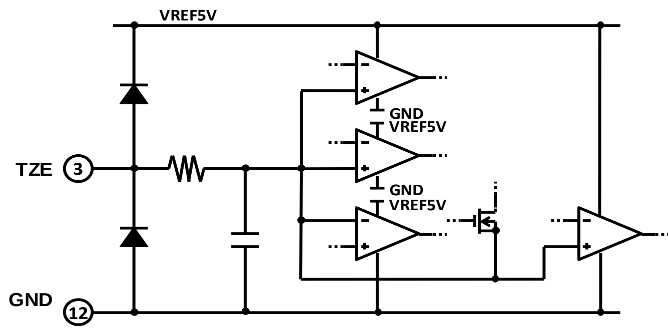
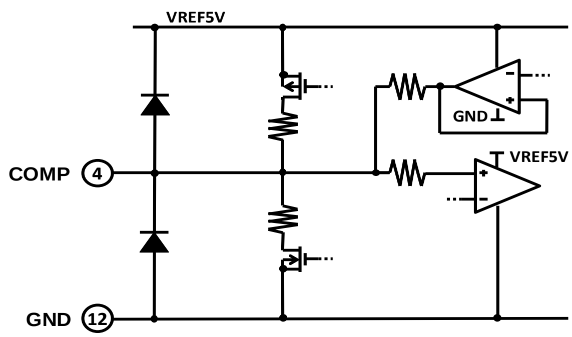
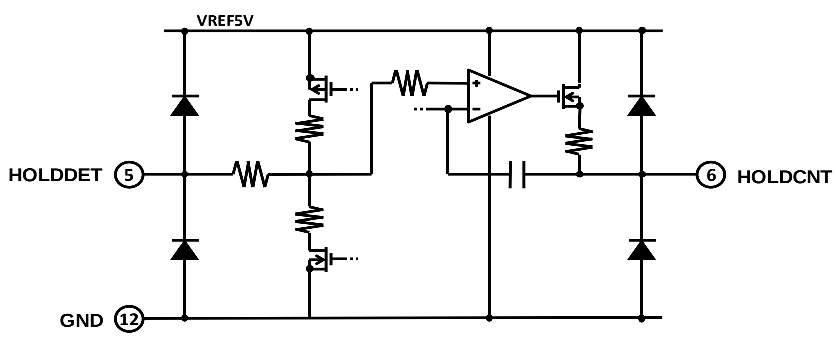
The over temperature protection (OTP) protects IC from thermal destruction. When the junction temperature reaches +150°C, the DRV pin is turned to “L”, and the switching stops. It automatically returns to normal operation mode if the junction temperature falls back below +125°C.

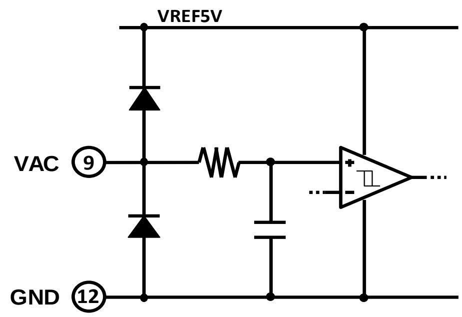
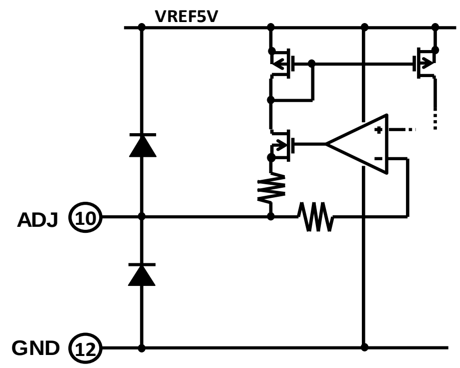
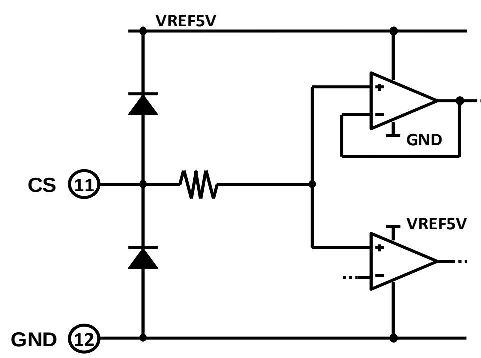
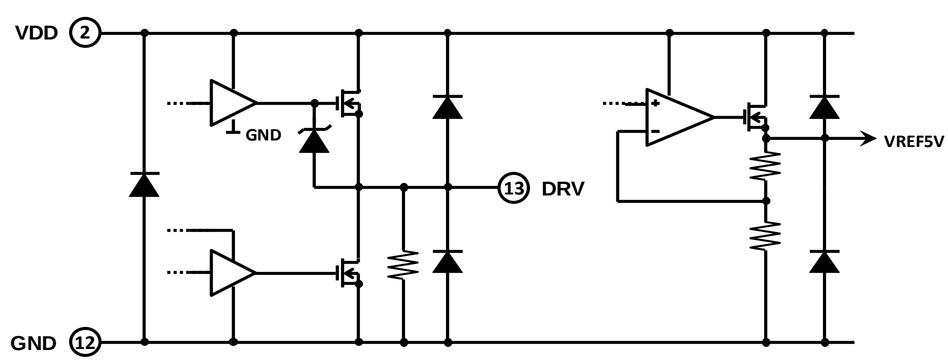
Table 8-2 Protection Functions Table

Function	PIN Operation				Detection Condition	Return Condition	Remarks
	DRV	HOLD CNT	COMP	ADJ			
Normal Operation	Active	Active	Active	Active	-	-	-
Under Voltage Lockout Protection (UVLO)	L	L	L	L	VDD < 8V	VDD > 10.2V	Auto Restart
Over Voltage Protection (OVP)	L	L	1.5V fixed	Active	TZE > 4.3V	VDD < 8V → VDD > 10.2V	Latch off
Over Current Protection (OCP)	L	Active	Active	Active	CS > 2V	Cycle by cycle	Auto Restart
Over Temperature Protection (OTP)	L	L	1.5V fixed	Active	Tj > +150°C	Tj < +125°C	Auto Restart

9. I/O Pin Equivalent Circuit Diagram

Figure 9-1 I/O Pin Equivalent Circuit Diagram

Pin No.	Pin Name	Equivalent Circuit Diagram
3	TZE	
4	COMP	
5, 6	HOLDDET, HOLDCNT	

Pin No.	Pin Name	Equivalent Circuit Diagram
9	VAC	
10	ADJ	
11	CS	
13	DRV	

10. Application Examples

10.1 17W Isolated and Phase Dimming Application

Input: AC85V$_{RMS}$ to 145V$_{RMS}$, Output: 470mA/32V to 42V, Ta = +25°C

Figure 10-1 17W EVB Schematic

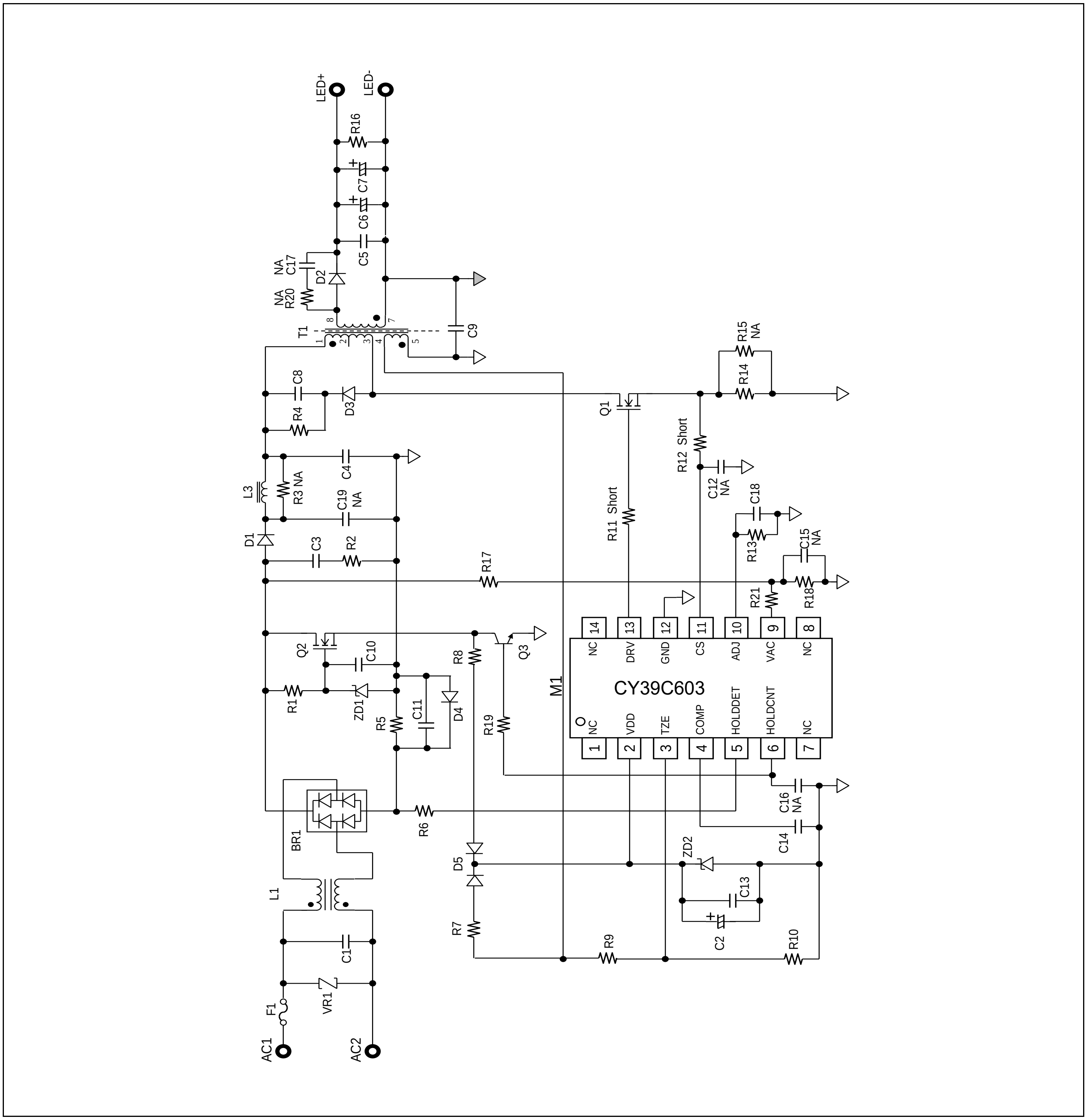
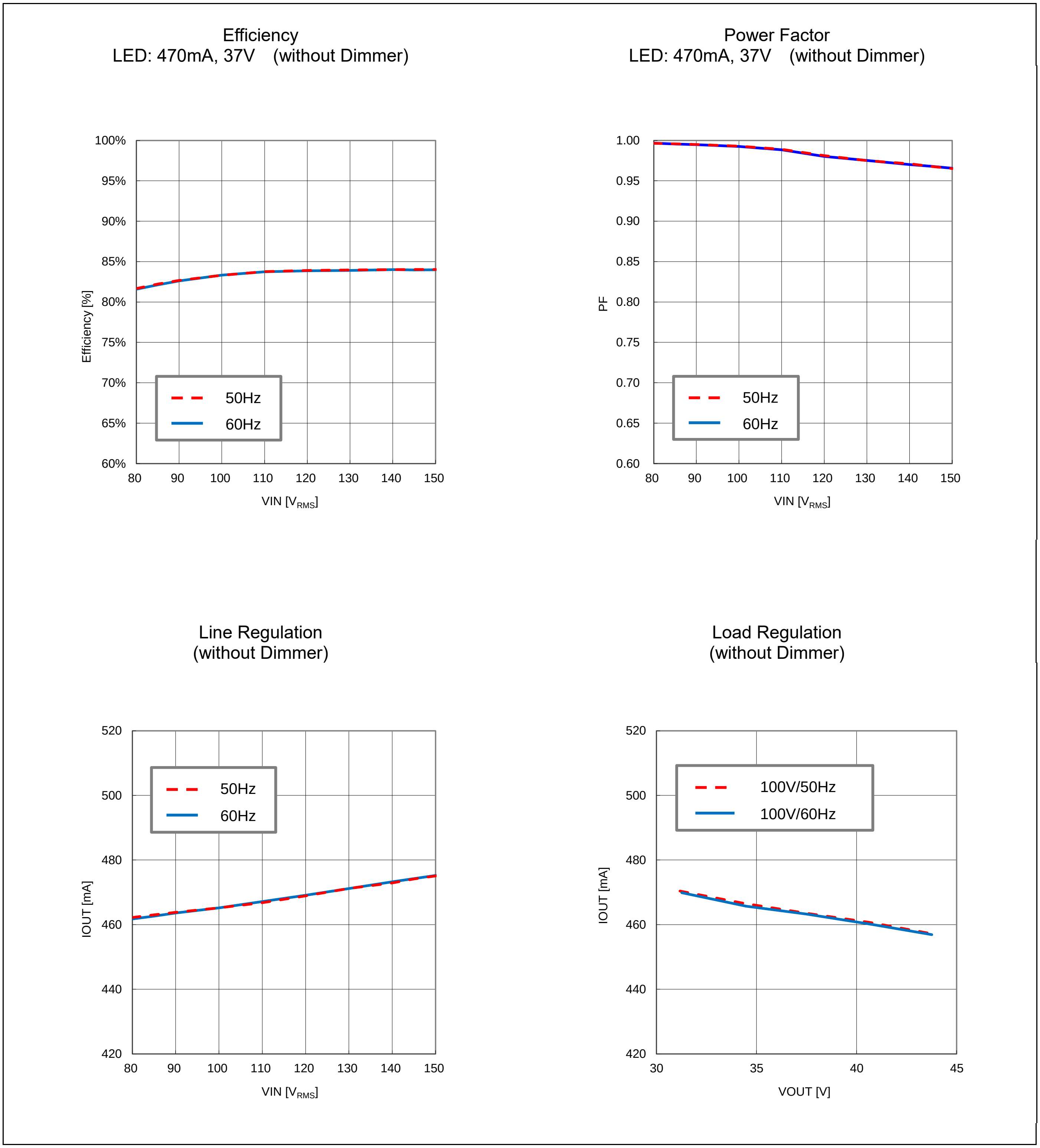


Table 10-1 17W BOM List

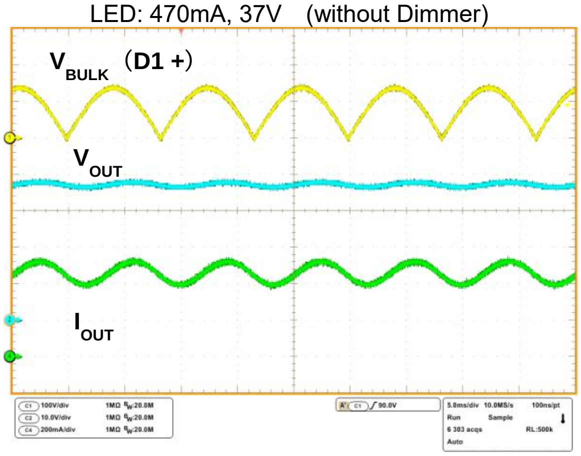
No.	Component	Description	Part No.	Vendor
1	M1	LED driver IC, SOP-14	CY39C603	Cypress
2	Q1	MOSFET, N-channel, 800V, 5.5A, TO-220F	FQPF8N80C	Fairchild
3	Q2	MOSFET, N-channel, 650V, 7.3A, TO-220	FDPF10N60NZ	Fairchild
4	Q3	Bipolar transistor, NPN, 60V, 3A, hfe = 250min, SOT-223	NZT560A	Fairchild
5	BR1	Bridge rectifier, 1A, 600V, Micro-DIP	MDB6S	Fairchild
6	D1	Diode, ultra fast rectifier, 1A, 600V, SMA	ES1J	Fairchild
7	D2	Diode, ultra fast rectifier, 3A, 200V, SMC	ES3D	Fairchild
8	D3	Diode, fast rectifier, 1A, 800V, SMA	RS1K	Fairchild
9	D4	Diode, ultra fast rectifier, 1A, 200V, SMA	ES1D	Fairchild
10	D5	Diode, 200 mA, 200V, SOT-23	MMBD1404	Fairchild
11	ZD1, ZD2	Diode, Zener, 18V, 500 mW, SOD-123	MMSZ18T1G	ON Semi
12	T1	Transformer, 600 μH	EI-2520	-
13	L1	Common mode inductor, 20 mH, 0.5A	744821120	Wurth Electronic
14	L3	Inductor, 3.3 mH, 0.27A, 5.0Ω, ϕ10×14.4	RCH114NP-332KB	Sumida
15	C1	Capacitor, X2, 305VAC, 0.1 μF	B32921C3104M	EPCOS
16	C2	Capacitor, aluminum electrolytic, 100 μF, 25V, ϕ6.3×11	EKMG250ELL101MF11D	NIPPON-CHEMI-CON
17	C3	Capacitor,polyester film, 220 nF, 400V, 18.5×5.9	ECQ-E4224KF	Panasonic
18	C4	Capacitor,polyester film, 100 nF, 400V, 12×6.3	ECQ-E4104KF	Panasonic
19	C5	Capacitor, ceramic, 10 μF, 50V, X7S, 1210	-	-
20	C6, C7	Capacitor, aluminum electrolytic, 470 μF 50V, ϕ10.0×20	EKMG500ELL471MJ20S	NIPPON-CHEMI-CON
21	C8	Capacitor, ceramic, 15 nF, 250V, X7R, 1206	-	-
22	C9	Capacitor, ceramic, 2.2 nF, X1/Y1 radial	DE1E3KX222M	muRata
23	C10, C11	Capacitor, ceramic, 0.1 μF, 50V, X5R, 0603	-	-
24	C12, C15, C16	NA (Open), 0603	-	-
25	C13	Capacitor, ceramic, 10 μF, 35V, X5R, 0805	-	-
26	C14	Capacitor, ceramic, 4.7 μF, 16V, JB, 0805	-	-
27	C17	NA (Open), 1206	-	-
28	C18	Capacitor, ceramic, 100 pF, 50V, CH, 0603	-	-
29	C19	NA (Open)	-	-
30	R1, R17	Resistor, chip, 1 MΩ, 1/4W, 1206	-	-
31	R2	Resistor, metal film, 510Ω, 2W,	-	-
32	R3	NA (Open), 1206	-	-
33	R4	Resistor, metal oxide film, 68 kΩ, 3W	-	-
34	R5	Resistor, chip, 5.1Ω, 1W, 2512	-	-
35	R6	Resistor, chip, 62 kΩ, 1/10W, 0603	-	-
36	R7	Resistor, chip, 10Ω, 1/8W, 0805	-	-
37	R8	Resistor, chip, 22Ω, 1/10W, 0603	-	-
38	R9	Resistor, chip, 91 kΩ, 1/10W, 0603	-	-
39	R10	Resistor, chip, 24 kΩ, 1/10W, 0603	-	-
40	R11, R12	NA (Short), 0603	-	-
41	R13	Resistor, chip, 39 kΩ, 1/10W, 0603	-	-
42	R14	Resistor, chip, 1.1Ω, 1/4W, 1206	-	-
43	R16	Resistor, chip, 51 kΩ, 1/10W, 0603	-	-
44	R18	Resistor, chip, 33 kΩ, 1/10W, 0603	-	-
45	R19	Resistor, chip, 12 kΩ, 1/10W, 0603	-	-
46	R20, R15	NA (Open), 1206	-	-
47	R21	Resistor, chip, 510 kΩ, 1/10W, 0603	-	-
48	VR1	Varistor, 275VAC, 7 mm DISK	ERZ-V07D431	Panasonic
49	F1	Fuse, 1A, 300VAC	3691100000	Littelfuse

Fairchild	:	Fairchild Semiconductor International, Inc.
On Semi	:	ON Semiconductor
Wurth Electronic	:	Wurth Electronics Midcom Inc.
Sumida	:	SUMIDA CORPORATION
EPCOS	:	EPCOS AG
NIPPON-CHEMI-CON	:	Nippon Chemi-Con Corporation
Panasonic	:	Panasonic Corporation
muRata	:	Murata Manufacturing Co., Ltd.
Littelfuse	:	Littelfuse, Inc.

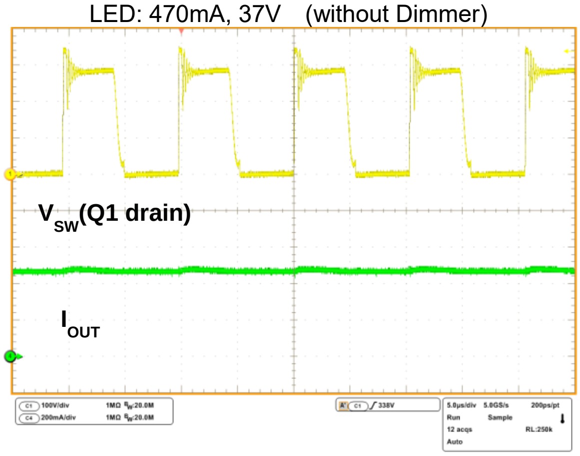
Figure 10-2 17W Reference Data



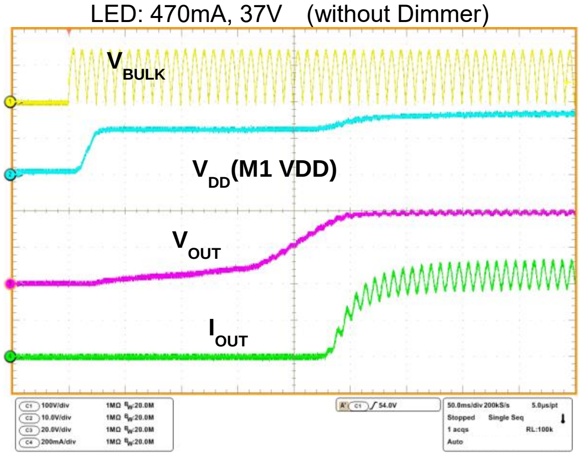
Output Ripple Waveform
V_{IN}=100V_{RMS} / 60Hz
LED: 470mA, 37V (without Dimmer)



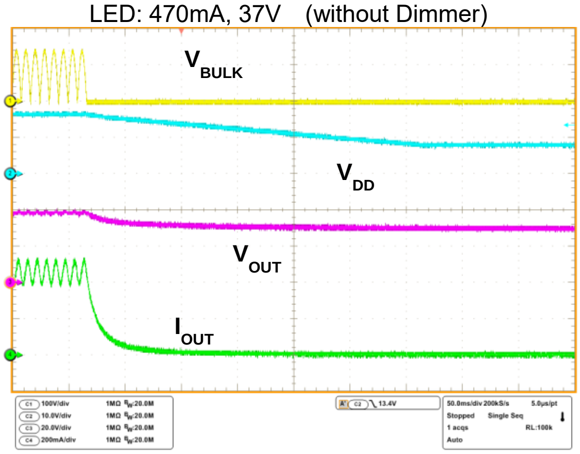
Switching Waveform
V_{IN}=100V_{RMS} / 60Hz
LED: 470mA, 37V (without Dimmer)



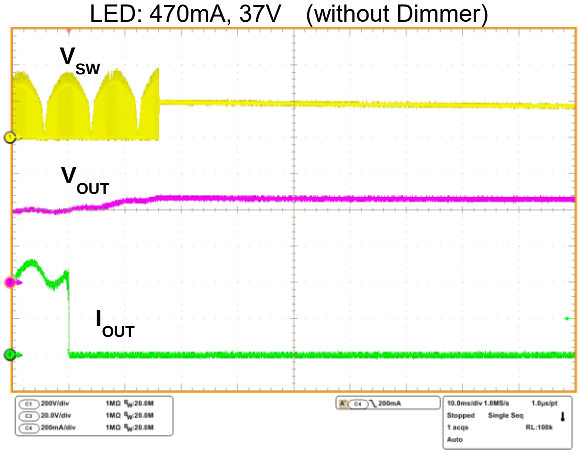
Turn-On Waveform
V_{IN}=100V_{RMS} / 60Hz
LED: 470mA, 37V (without Dimmer)



Turn-Off Waveform
V_{IN}=100V_{RMS} / 60Hz
LED: 470mA, 37V (without Dimmer)



LED Open Waveform
V_{IN}=100V_{RMS} / 60Hz
LED: 470mA, 37V (without Dimmer)



Total Harmonic Distortion(THD)
LED: 470mA, 37V (without Dimmer)

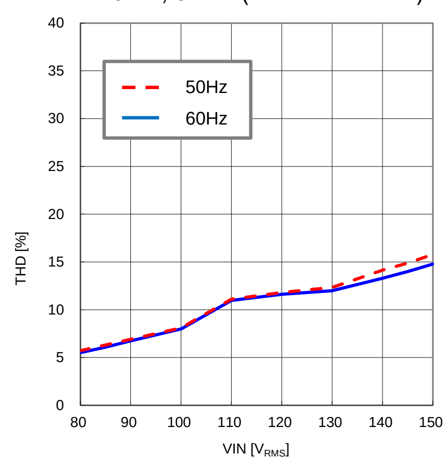


Figure 10-3 17W Japan Dimmer Performance Data

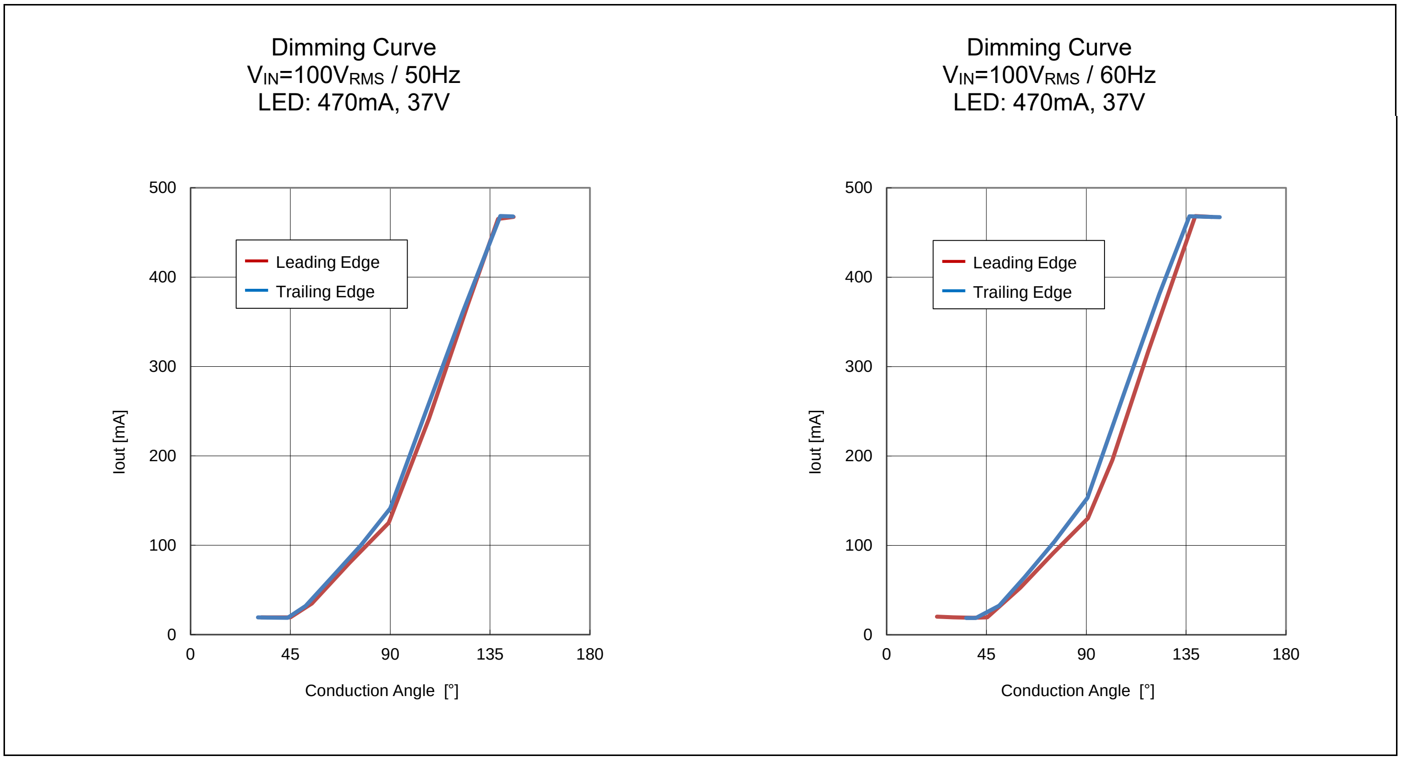


Table 10-2 17W Japan Dimmer Performance Data

Dimmer		Input Condition	Type	Minimum Angle (°)	Minimum I_{OUT} (mA)	Maximum Angle (°)	Maximum I_{OUT} (mA)
Vendor	Parts Name						
LUTRON	DVCL-123P-JA	V_{IN}=100V_{RMS} 50Hz (Japan Dimmer)	Leading Edge	31.9	19.2	141.8	468.4
Panasonic	WTC57521			38.0	19.2	145.6	467.6
	WN575280K			27.7	19.8	147.2	467.0
	NQ20203T			31.0	19.4	146.7	466.9
DAIKO	DP-37154			32.4	19.1	142.9	466.9
Mitsubishi	DEM1003B			28.3	19.7	147.8	466.9
TOSHIBA	DG9022H			46.4	19.4	151.9	467.2
	DG9048N			34.0	19.2	155.3	466.6
	WDG9001		Trailing Edge	30.4	18.8	145.4	468.4
LUTRON	DVCL-123P-JA	V_{IN}=100V_{RMS} 60Hz (Japan Dimmer)	Leading Edge	22.7	19.1	138.5	468.7
Panasonic	WTC57521			38.9	19.1	146.7	468.4
	WN575280K			27.4	19.6	146.2	466.8
	NQ20203T			27.6	19.6	144.3	467.3
DAIKO	DP-37154			33.0	19.1	144.3	467.0
Mitsubishi	DEM1003B			25.9	19.9	145.2	467.2
TOSHIBA	DG9022H			22.0	18.8	150.8	467.0
	DG9048N			22.7	19.6	153.6	466.5
	WDG9001		Trailing Edge	35.9	18.7	150.1	468.3

Figure 10-4 17W USA Dimmer Performance Data

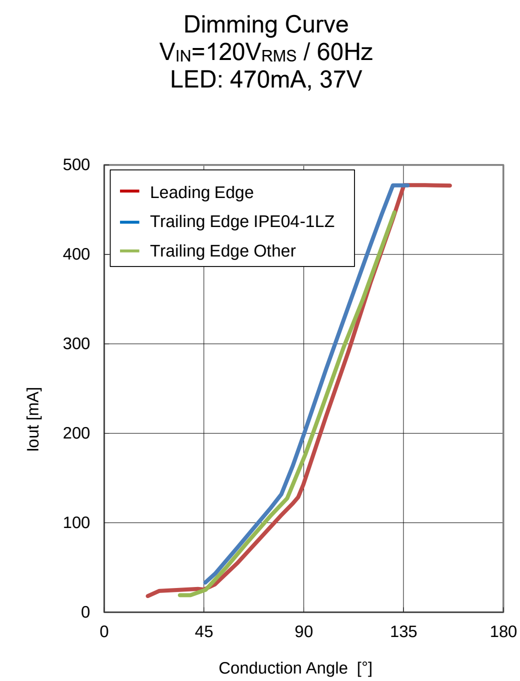


Table 10-3 17W USA Dimmer Performance Data

Dimmer		Input Condition	Type	Minimum Angle (°)	Minimum I_{OUT} (mA)	Maximum Angle (°)	Maximum I_{OUT} (mA)
Vendor	Parts Name						
LEVITON	IPI06-1LZ	V_{IN}=120V_{RMS} 60Hz (USA Dimmer)	Leading Edge	42.3	25.3	156.0	477.5
	6631-LW			21.8	20.1	144.1	470.2
	6641-W			39.1	19.5	147.7	471.5
	6683			35.2	19.5	155.5	468.9
LUTRON	SLV-600-WH			19.7	18.0	135.4	454.2
	S-600P-WH			35.0	19.5	137.6	470.6
	TG-600PH-WH			45.4	19.8	140.4	470.5
	AY-600P-WH			40.2	19.5	143.6	470.6
	GL-600H-DK			25.1	20.0	135.9	457.3
	TG-600PNLH-WH			34.1	19.5	141.0	470.8
	TGCL-153PH-WH			33.3	19.4	135.0	455.4
	TT-300NLH-WH			41.7	19.5	143.2	470.5
	DV-603PG-WH			35.6	19.4	116.4	316.5
	DVCL-153-WH			38.0	19.4	133.9	445.7
	DV603PH-WH			33.0	19.5	136.9	471.2
	LGCL-153PLH-WH			39.3	19.2	133.9	444.4
	D-603PH			24.2	20.0	133.5	439.1
	DV-600PH-WH			32.8	19.3	139.3	470.7
GE	52129			23.8	20.2	157.0	469.8
	18023			36.9	19.4	158.5	469.5
LEVITON	IPE04-1LZ		Trailing Edge	45.6	33.1	136.9	477.3
LUTRON	SELV-300P-WH			34.1	19.1	130.9	447.2
	DVELV-300P-WH			34.1	19.0	131.8	455.2

Figure 10-5 17W Parts Surface Temperature

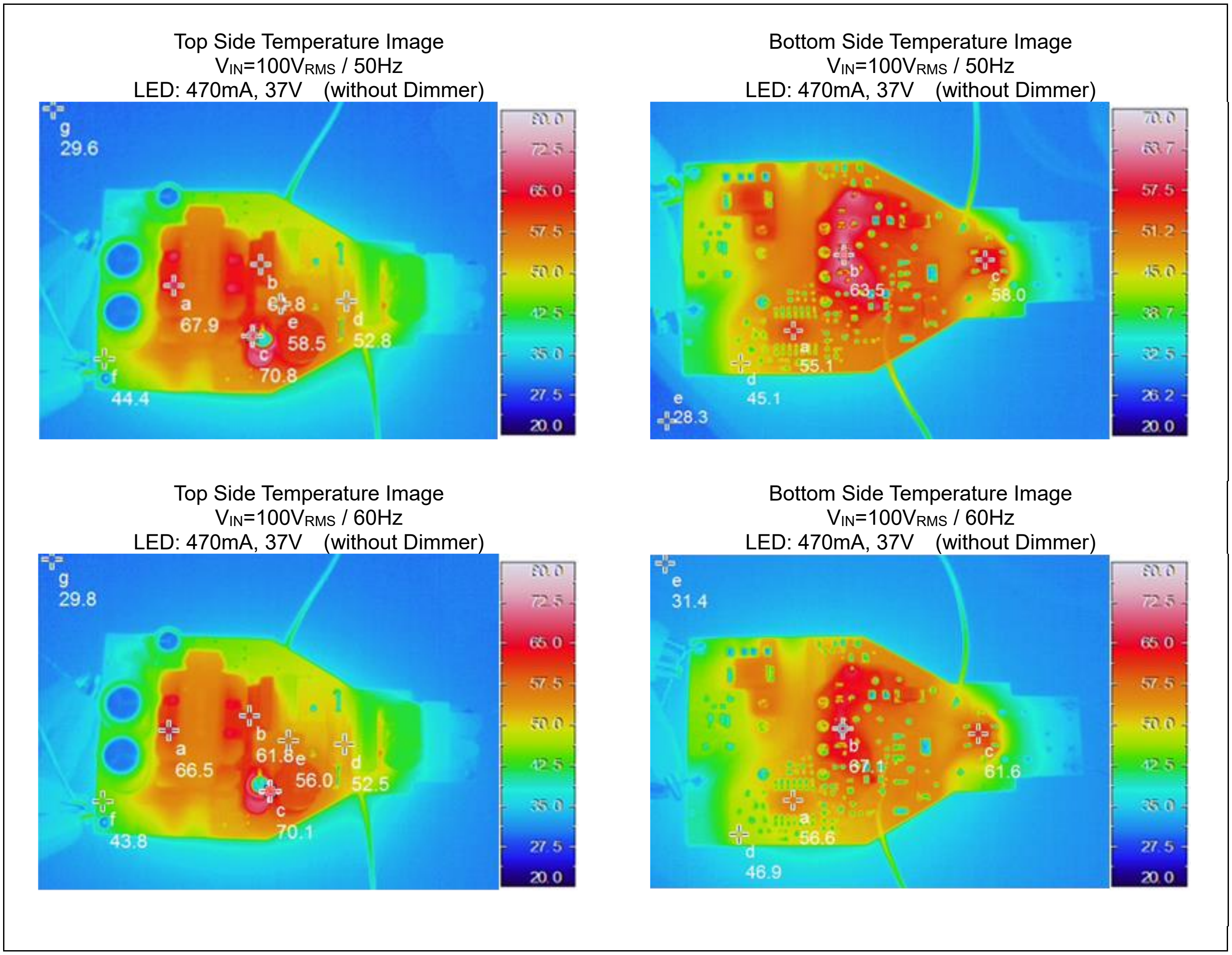


Table 10-4 17W Parts Surface Temperature Data

Side	Cursor Point		Surface Temperature [℃]		ΔTemperature [Δ℃]	
			50Hz	60Hz	50Hz	60Hz
Top	a	T2	68.0	66.5	38.3	36.8
	b	Q1	61.8	61.8	32.2	32.0
	c	R4	70.8	70.1	41.2	40.3
	d	R2	52.8	52.5	23.1	22.8
	e	Q2	58.5	56.0	28.9	26.2
	f	PCB	44.5	43.8	14.8	14.0
	g	Out of PCB	29.6	29.8	-	-
Bottom	a	M1	55.1	56.6	26.8	25.2
	b	Back side of R4	63.5	67.1	35.2	35.8
	c	BR1	58.0	61.6	29.7	30.2
	d	PCB	45.1	46.9	16.7	15.5
	e	Out of PCB	28.3	31.4	-	-

11. Usage Precautions

Do not configure the IC over the maximum ratings.

If the IC is used over the maximum ratings, the LSI may be permanently damaged.

It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

Use the device within the recommended operating conditions.

The recommended values guarantee the normal LSI operation under the recommended operating conditions.

The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

Take appropriate measures against static electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial between body and ground.

Do not apply negative voltages.

The use of negative voltages below - 0.3 V may make the parasitic transistor activated to the LSI, and can cause malfunctions.

12. RoHS Compliance Information

This product has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE).

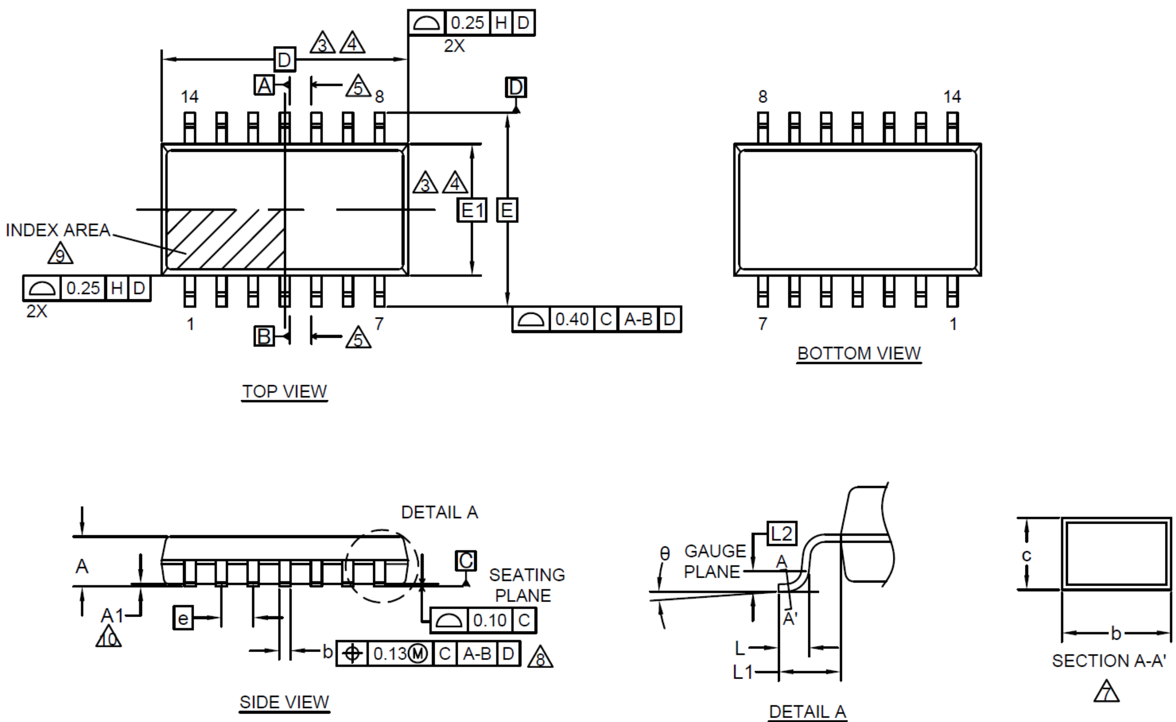
13. Ordering Information

Table 13-1 Ordering Information

Part Number	Package	Shipping Form
CY39C603PF-G-JNEFE1	14-pin plastic SOP (SOF014)	Emboss
CY39C603PF-G-JNE1		Tube

14. Package Dimensions

Package Code: SOF014



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	2.25
A1	0.05	—	0.20
D	10.15 BSC		
E	7.80 BSC		
E1	5.30 BSC		
θ	0°	—	8°
c	0.13	—	0.20
b	0.39	0.47	0.55
L	0.45	0.60	0.75
L1	1.25 REF		
L2	0.25 BSC		
e	1.27 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15859 Rev. **

15. Major Changes

Spansion Publication Number: MB39C603_DS405-00021

Page	Section	Descriptions
Revision1.0		
-	-	Initial release
Revision2.0		
7	7. Absolute Maximum Ratings	Removed ESD Voltage (Machine Model) from Table 7-1

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: CY39C603 Phase Dimmable PSR LED Driver IC for LED Lighting
Document Number: 002-08450

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TOYO	02/20/2015	Migrated to Cypress and assigned document number 002-08450. No change to document contents or format.
*A	5211117	TOYO	04/07/2016	Updated to Cypress format.
*B	5742340	HIXT	05/22/2017	Updated Pin Assignment: Change the package name from FPT-14P-M04 to SOF014 Added RoHS Compliance Information Updated Ordering Information: Change the package name from FPT-14P-M04 to SOF014 Deleted “Marking Format” Deleted “Recommended Mounting Condition [JEDEC Level3] Lead Free” Updated Package Dimensions: Updated to Cypress format
*C	6437385	ATTS	01/10/2019	Changed part number to CY39C603

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- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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