

General Description

Micrel's MIC2193 is a high efficiency, PWM synchronous buck control IC housed in the SO-8 package. Its 2.9V to 14V input voltage range allows it to efficiently step down voltages in 3.3V, 5V, and 12V systems as well as 1- or 2-cell Li Ion battery powered applications.

The MIC2193 solution saves valuable board space. The device is housed in the space-saving SO-8 package, whose low pin-count minimizes external components. Its 400kHz PWM operation allows a small inductor and small output capacitors to be used. The MIC2193 can implement all-ceramic capacitor solutions.

The MIC2193 drives a high-side P-channel MOSFET, eliminating the need for high-side boot-strap circuitry. This feature allows the MIC2193 to achieve maximum duty cycles of 100%, which can be useful in low headroom applications. A low output driver impedance of 4Ω allows the MIC2193 to drive large external MOSFETs to generate a wide range of output currents.

The MIC2193 is available in an 8 pin SOIC package with a junction temperature range of -40°C to +125°C.

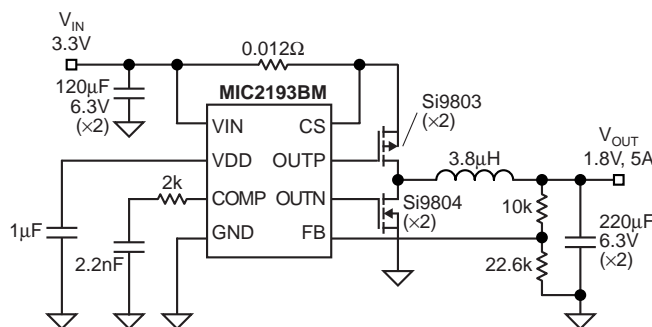
Features

- 2.9V to 14V input voltage range
- 400kHz oscillator frequency
- PWM current mode control
- 100% maximum duty cycle
- Front edge blanking
- 4Ω output drivers
- Cycle-by-cycle current limiting
- Frequency foldback short circuit protection
- 8 lead SOIC package

Applications

- Point of load power supplies
- Distributed power systems
- Wireless Modems
- ADSL line cards
- Servers
- Step down conversion in 3.3V, 5V, and 12V systems
- 1-and 2-cell Li Ion battery operated equipment

Typical Application

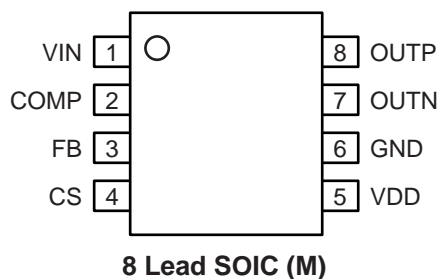


Adjustable Output Synchronous Buck Converter

Ordering Information

| Part Number | Voltage | Frequency | Temperature Range | Package | Lead Finish |
|-------------|------------|-----------|-------------------|------------|-------------|
| MIC2193BM | Adjustable | 400KHz | –40°C to +125°C | 8-lead SOP | Standard |
| MIC2193YM | Adjustable | 400KHz | –40°C to +125°C | 8-lead SOP | Pb-Free |

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Function |
|------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1 | VIN | Controller supply voltage. Also the (+) input to the current sense amp. |
| 2 | COMP | Compensation (Output): Internal error amplifier output. Connect to a capacitor or series RC network to compensate the regulator's control loop. |
| 3 | FB | Feedback Input: The circuit regulates this pin to 1.245V. |
| 4 | CS | The (–) input to the current limit comparator. A built in offset of 110mV between VIN and CSL in conjunction with the current sense resistor sets the current limit threshold level. This is also the (–) input to the current amplifier. |
| 5 | VDD | 3V internal linear-regulator output. VDD is also the supply voltage bus for the chip. Bypass to GND with 1μF. |
| 6 | GND | Ground. |
| 7 | OUTN | High current drive for the synchronous N-channel MOSFET. Voltage swing is from ground to VIN. On-resistance is typically 6Ω at 5V _{IN} . |
| 8 | OUTP | High current drive for the high side P-channel MOSFET. Voltage swing is from ground to VIN. On-resistance is typically 6Ω at 5V _{IN} . |

Absolute Maximum Ratings (Note 1)

| | |
|---------------------------------------------|----------------------------------|
| Supply Voltage (V_{IN}) | 15V |
| Digital Supply Voltage (V_{DD}) | 7V |
| Comp Pin Voltage (V_{COMP}) | -0.3V to +3V |
| Feedback Pin Voltage (V_{FB}) | -0.3V to +3V |
| Current Sense Voltage ($V_{IN} - V_{CS}$) | -0.3V to +1V |
| Power Dissipation (P_D) | 285mW @ $T_A = 85^\circ\text{C}$ |
| Ambient Storage Temp | -65°C to +150°C |
| ESD Rating Note 3 | 2kV |

Operating Ratings (Note 2)

| | |
|-----------------------------|------------------------------------------------------|
| Supply Voltage (V_{IN}) | +2.9V to +14V |
| Junction Temperature | $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| Package Thermal Resistance | |
| θ_{JA} 8-lead SOP | 140°C/W |

Electrical Characteristics

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $T_J = 25^\circ\text{C}$, unless otherwise specified. **Bold** values indicate $-40^\circ\text{C} < T_J < +125^\circ\text{C}$.

| Parameter | Condition | Min | Typ | Max | Units |
|-----------------------------------------------|----------------------------------------------------------------------------|----------------------|----------------|----------------------|--------|
| Regulation | | | | | |
| Feedback Voltage Reference | (1%) (2%) | 1.233 1.22 | 1.245 1.245 | 1.257 1.27 | V V |
| Feedback Bias Current | | | 50 | | nA |
| Output Voltage Line Regulation | $5V \leq V_{IN} \leq 12V$ | | 0.09 | | % / V |
| Output Voltage Load Regulation | $0mV < (V_{IN} - V_{CS}) < 75mV$ | | 0.9 | | % |
| Output Voltage Total Regulation | $5V \leq V_{IN} \leq 12V$, $0mV < (V_{IN} - V_{CS}) < 75mV$ ($\pm 3\%$) | 1.208 | | 1.282 | V |
| Input & V_{DD} Supply | | | | | |
| V_{IN} Input Current (I_Q) | (excluding external MOSFET gate current) | | 1 | 2 | mA |
| Digital Supply Voltage (V_{DD}) | $I_L = 0$ | 2.82 | 3.0 | 3.18 | V |
| Digital Supply Load Regulation | $I_L = 0$ to 1mA | | 0.1 | | V |
| Undervoltage Lockout | V_{DD} upper threshold (turn on threshold) | | 2.65 | | V |
| UVLO Hysteresis | | | 100 | | mV |
| Current Limit | | | | | |
| Current Limit Threshold Voltage | $V_{IN} - V_{CS}$ voltage to trip current limit | 90 | 110 | 130 | mV |
| Error Amplifier | | | | | |
| Error Amplifier Gain | | | 20 | | V/V |
| Current Amplifier | | | | | |
| Current Amplifier Gain | | | 3.0 | | V/V |
| Oscillator Section | | | | | |
| Oscillator Frequency (f_O) | | 360 | 400 | 440 | kHz |
| Maximum Duty Cycle | $V_{FB} = 1.0V$ | 100 | | | % |
| Minimum On Time | $V_{FB} = 1.5V$ | | 165 | | ns |
| Frequency Foldback Threshold | Measured on FB | | 0.3 | | V |
| Frequency Foldback Frequency | | | 90 | | kHz |

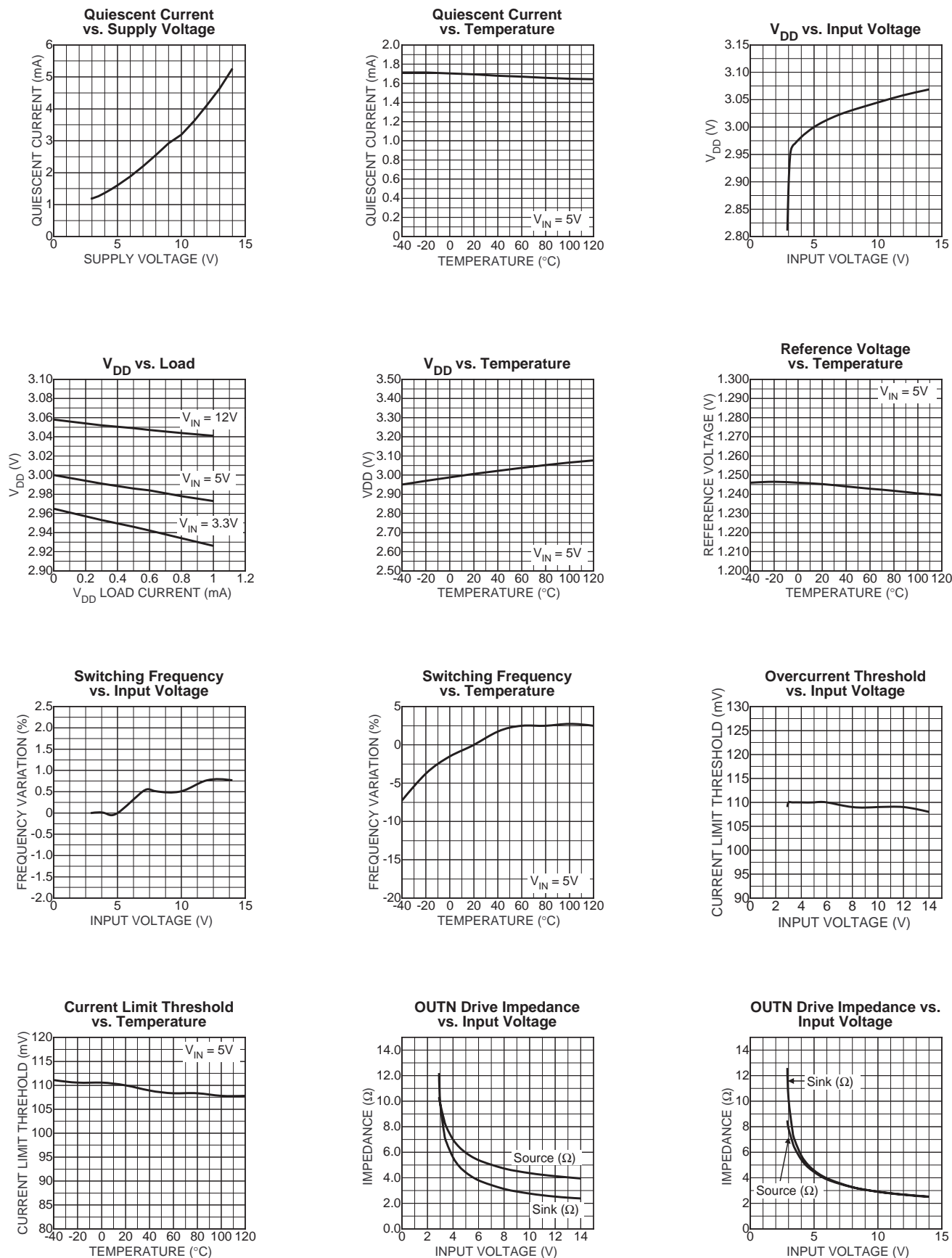
| Parameter | Condition | Min | Typ | Max | Units |
|-------------------------|-------------------------------|-----|-----|-----------|----------|
| Gate Drivers | | | | | |
| Rise/Fall Time | $C_L = 3300\text{pF}$ | | 50 | | ns |
| Output Driver Impedance | Source, $V_{IN} = 12\text{V}$ | | 4 | 10 | Ω |
| | Sink, $V_{IN} = 12\text{V}$ | | 4 | 10 | Ω |
| | Source, $V_{IN} = 5\text{V}$ | | 6 | 12 | Ω |
| | Sink, $V_{IN} = 5\text{V}$ | | 6 | 12 | Ω |
| Driver Non-overlap Time | $V_{IN} = 12\text{V}$ | | 50 | | ns |
| | $V_{IN} = 5\text{V}$ | | 80 | | ns |
| | $V_{IN} = 3.3\text{V}$ | | 160 | | ns |

Note 1. Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its operating ratings. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(\text{Max})}$, the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A .

Note 2. The device is not guaranteed to function outside its operating rating.

Note 3. Devices are ESD sensitive, handling precautions required. Human body model, 1.5k Ω in series with 100pF.

Typical Characteristics



The MIC2193 controller is broken down into five functions.

- Control loop
 - PWM operation
 - Current mode control
- Current limit
- Reference and V_{DD}
- MOSFET gate drive
- Oscillator

Control Loop

PWM Control Loop

The MIC2193 uses current mode control to regulate the output voltage. This dual control loop method (illustrated in Figure 2) senses the output voltage (outer loop) and the inductor current (inner loop). It uses inductor current and output voltage to determine the duty cycle of the buck converter. Sampling the inductor current effectively removes the inductor from the control loop, which simplifies compensation.

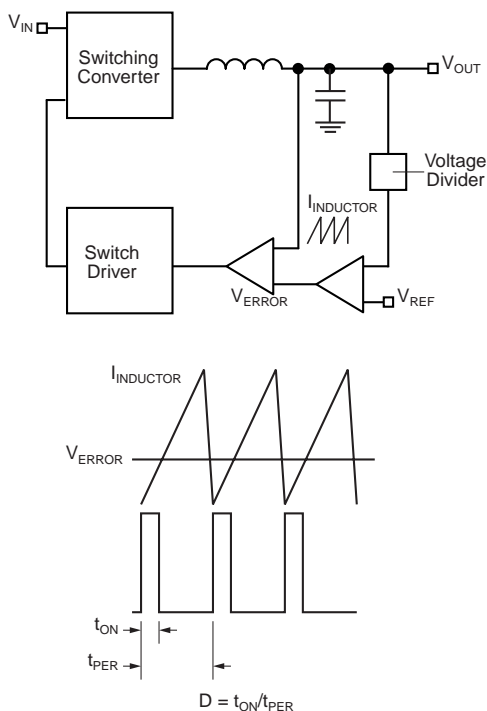


Figure 2. Current Mode Control Example

As shown in Figure 1, the inductor current is sensed by measuring the voltage across the resistor, R_{SENSE} . A ramp is added to the amplified current sense signal to provide slope compensation, which is required to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used for the error amplifier, which compares an attenuated sample of the output voltage with a reference voltage. The output of the error amplifier is the compensation pin (COMP), which is compared to the current sense waveform in the PWM block. When the current signal becomes greater than the error signal, the comparator turns off the high-side drive. The COMP pin provides access to the output of the error amplifier and allows the use of external components to stabilize the voltage loop.

Current Limit

The output current is detected by the voltage drop across the external current sense resistor (R_{SENSE} in Figure 1.). The current sense resistor must be sized using the minimum current limit threshold. The external components must be designed to withstand the maximum current limit. The current sense resistor value is calculated by the equation below:

$$R_{SENSE} = \frac{MIN_CURRENT_SENSE_THRESHOLD}{I_{OUT_MAX}}$$

The maximum output current is:

$$I_{OUT_MAX} = \frac{MAX_CURRENT_SENSE_THRESHOLD}{R_{SENSE}}$$

The current sense pins VIN (pin 1) and CSL (pin 4) are noise sensitive due to the low signal level and high input impedance and switching noise on the VIN pin. The PCB traces should be short and routed close to each other. A 10nF capacitor across the pins will attenuate high frequency switching noise.

When the peak inductor current exceeds the current limit threshold, the overcurrent comparator turns off the high side MOSFET for the remainder of the switching cycle, effectively decreasing the duty cycle. The output voltage drops as additional load current is pulled from the converter. When the voltage at the feedback pin (FB) reaches approximately 0.3V, the circuit enters frequency foldback mode and the oscillator frequency will drop to approximately 1/4 of the switching frequency. This limits the maximum output power delivered to the load under a short circuit condition.

Reference and V_{DD} Circuits

The output drivers are enabled when the V_{DD} voltage (pin 5) is greater than its undervoltage threshold.

The internal bias circuit generates an internal 1.245V band-gap reference voltage for the voltage error amplifier and a 3V V_{DD} voltage for the internal control circuitry. The V_{DD} pin must be decoupled with a 1 μ F ceramic capacitor. The capacitor must be placed close to the V_{DD} pin. The other end of the capacitor must be connected directly to the ground plane.

MOSFET Gate Drive

The MIC2193 is designed to drive a high-side, P-Channel MOSFET and a low side, N-Channel MOSFET. The source pin of the P-channel MOSFET is connected to the input of the power supply. It is turned on when OUTP pulls the gate of the MOSFET low. The advantage of using a P-channel MOSFET is that it does not required a bootstrap circuit to boost the gate voltage higher than the input, as would be required for an N-channel MOSFET.

The VIN pin (pin 1) supplies the drive voltage to both gate drive pins, OUTN and OUTP. The VIN pin must be well decoupled to prevent noise from affecting the current sense circuit, which uses VIN as one of the sense pins.

A non-overlap time is built into the MOSFET driver circuitry. This dead time prevents the high-side and low-side MOSFET drivers from being on at the same time. Either an external diode or the low-side MOSFET internal parasitic diode conducts the inductor current during the dead time.

MOSFET Selection

The P-channel MOSFET must have a V_{GS} threshold voltage equal to or lower than the input voltage when used in a buck converter topology. There is a limit to the maximum gate charge the MIC2193 will drive. MOSFETs with higher gate charge will have slower turn-on and turn-off times. Slower transition times will cause higher power dissipation in the MOSFETs due to higher switching transition losses. The MOSFETs must be able to completely turn on and off within the driver non-overlap time. If both MOSFETs are conducting at the same time, shoot-through will occur, which greatly increases power dissipation in the MOSFETs and reduces converter efficiency.

The MOSFET gate charge is also limited by power dissipation in the MIC2193. The power dissipated by the gate drive circuitry is calculated below:

$$P_{GATE_DRIVE} = Q_{GATE} \times V_{IN} \times f_S$$

where:

Q_{GATE} is the total gate charge of both the N and P-channel MOSFETs.

f_S is the switching frequency

V_{IN} is the gate drive voltage

The graph in Figure 3 shows the total gate charge that can be driven by the MIC2193 over the input voltage range, for different values of switching frequency.

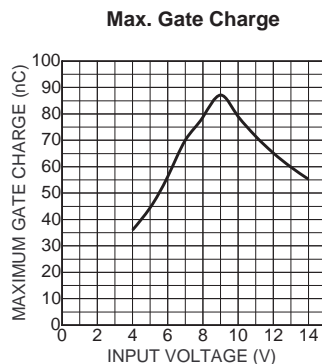


Figure 3. MIC2193 Frequency vs Max. Gate Charge

Oscillator

The internal oscillator is free running and requires no external components. The maximum duty cycle is 100%. This is another advantage of using a P-channel MOSFET for the high-side drive: it can continuously turned on.

A frequency foldback mode is enabled if the voltage on the feedback pin (pin 3) is less than 0.3V. In frequency foldback, the oscillator frequency is reduced by approximately a factor of 4. Frequency foldback is used to limit the energy delivered to the output during a short circuit fault condition.

Voltage Setting Components

The MIC2193 requires two resistors to set the output voltage as shown in Figure 4.

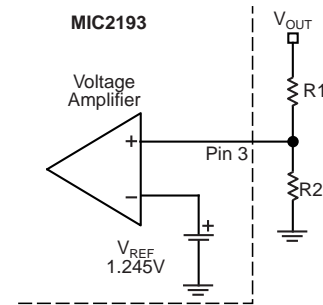


Figure 4

The output voltage is determined by the equation below.

$$V_{OUT} = V_{REF} \times 1 + \frac{R1}{R2}$$

Where: V_{REF} for the MIC2193 is typically 1.245V.

Lower values of R1 are preferred to prevent noise from appearing on the FB pin. A typically recommended value is 10kΩ. If R1 is too small in value it will decrease the efficiency of the power supply, especially at low output loads.

Once R1 is selected, R2 can be calculated with the following formula.

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}}$$

Efficiency Considerations

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the buck converter. Under light output load, the significant contributors are:

- The V_{IN} supply current

To maximize efficiency at light loads:

- Use a low gate charge MOSFET or use the smallest MOSFET, which is still adequate for maximum output current.
- Use a ferrite material for the inductor core, which has less core loss than an MPP or iron power core.

Under heavy output loads the significant contributors to power loss are (in approximate order of magnitude):

- Resistive on time losses in the MOSFETs
- Switching transition losses in the high side MOSFET
- Inductor resistive losses
- Current sense resistor losses
- Input capacitor resistive losses (due to the capacitors ESR)

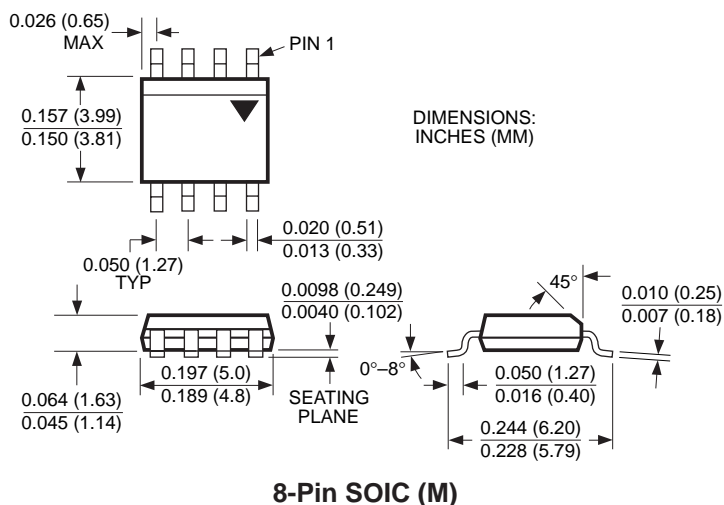
To minimize power loss under heavy loads:

- Use low on resistance MOSFETs. Use low threshold logic level MOSFETs when the input voltage is below 5V. Multiplying the gate charge by the on resistance gives a figure of merit, providing a good balance between low load and high load efficiency.
- Slow transition times and oscillations on the voltage and current waveforms dissipate more power during the turn on and turn off of the MOSFETs. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate charge MOSFETs will

transition faster than those with higher gate charge requirements.

- For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will require more output capacitors to filter the output ripple, which will force a smaller bandwidth, slower transient response and possible instability under certain conditions.
- Lowering the current sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and will require larger MOSFETs and inductor components.
- Use low ESR input capacitors to minimize the power dissipated in the capacitors ESR.

Package Information



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