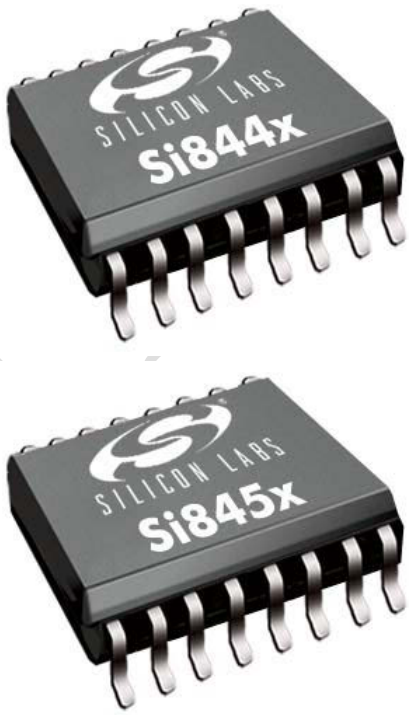
Four and Five-Channel Digital Isolators

Features

- High-speed operation
  - DC to 150 Mbps
- No start-up initialization required
- Wide Operating Supply Voltage: 2.70–5.5 V
- Ultra low power (typical)
  5 V Operation:
  - < 1.6 mA per channel at 1 Mbps
  - < 6 mA per channel at 100 Mbps
  2.70 V Operation:
  - < 1.4 mA per channel at 1 Mbps
  - < 4 mA per channel at 100 Mbps
- High electromagnetic immunity
- Up to 1000 V_{RMS} isolation
- Precise timing (typical)
  - <10 ns worst case
  - 1.5 ns pulse width distortion
  - 0.5 ns channel-channel skew
  - 2 ns propagation delay skew
  - 6 ns minimum pulse width
- Transient Immunity 25 kV/µs
- Wide temperature range
  - –40 to 125 °C at 150 Mbps
- RoHS-compliant packages
  - QSOP-16



Ordering Information:
See page 25.

Applications

- Industrial automation systems
- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power inverters
- Communications systems

Safety Regulatory Approvals

- UL 1577 recognized
  - Up to 1000 V_{RMS} for 1 minute
- CSA component notice 5A approval
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

Silicon Lab's family of ultra-low-power digital isolators are CMOS devices offering substantial data rate, propagation delay, power, size, reliability, and external BOM advantages when compared to legacy isolation technologies. The operating parameters of these products remain stable across wide temperature ranges throughout their service life. For ease of design, only VDD bypass capacitors are required.

Data rates up to 150 Mbps are supported, and all devices achieve worst-case propagation delays of less than 10 ns. These devices are available in a 16-pin QSOP package.

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1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	°C
Supply Voltage	V_{DD1}		2.70	—	5.5	V
	V_{DD2}		2.70	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature[2]	T_{STG}	–65	—	150	°C
Ambient Temperature Under Bias	T_A	–40	—	125	°C
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	6.0	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	I_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	°C
Maximum Isolation (Input to Output) (1 sec) QSOP-16		—	—	1000	V_{RMS}

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

Table 3. Electrical Characteristics

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at Supply)						
Si8455Bx						
V_{DD1}		All inputs 0 DC	—	1.6	2.4	mA
V_{DD2}		All inputs 0 DC	—	2.9	4.4	
V_{DD1}		All inputs 1 DC	—	7.0	10.5	
V_{DD2}		All inputs 1 DC	—	3.1	4.7	
Si8442Bx						
V_{DD1}		All inputs 0 DC	—	2.3	3.5	mA
V_{DD2}		All inputs 0 DC	—	2.3	3.5	
V_{DD1}		All inputs 1 DC	—	4.5	6.8	
V_{DD2}		All inputs 1 DC	—	4.5	6.8	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx						
V_{DD1}			—	4.3	6.5	mA
V_{DD2}			—	3.5	5.3	
Si8442Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.6	5.4	
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx						
V_{DD1}			—	4.3	6.5	mA
V_{DD2}			—	4.8	6.7	
Si8442Bx						
V_{DD1}			—	4.2	5.9	mA
V_{DD2}			—	4.2	5.9	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics (Continued)
(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx V_{DD1} V_{DD2}			 — —	 4.6 24	 6.9 30	mA
Si8442Bx V_{DD1} V_{DD2}			 — —	 11.8 11.8	 14.8 14.8	mA
Timing Characteristics						
Si845xAx, Si8442Bx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si845xBx, Si8442Bx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	3.8	5.0	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	2.8	3.7	ns
Common Mode Transient Immunity	CMTI	$V_I = V_{DD}$ or 0 V	—	25	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

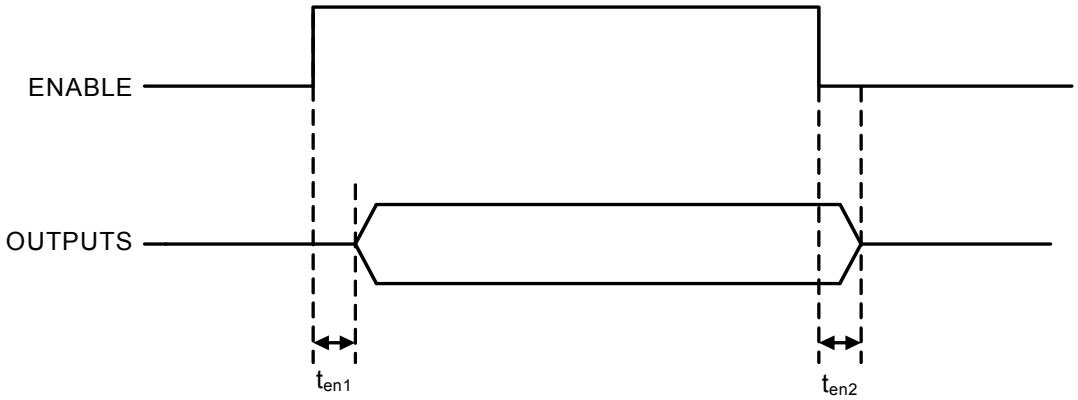


Figure 1. ENABLE Timing Diagram

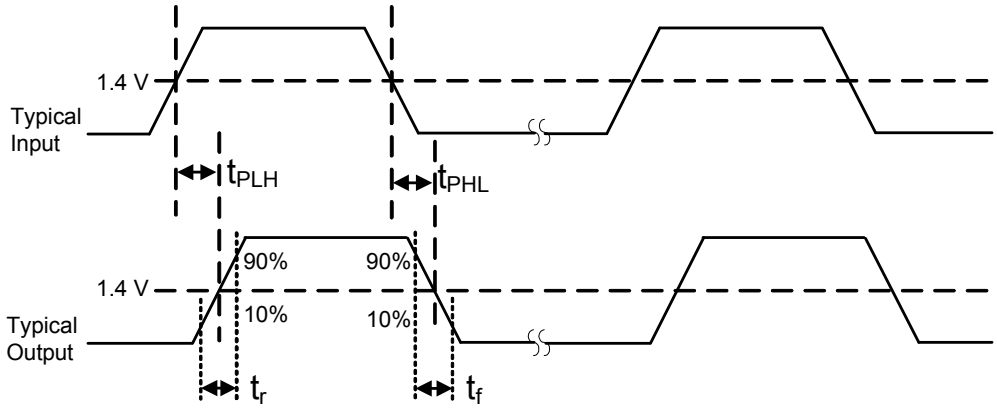


Figure 2. Propagation Delay Timing

Table 4. Electrical Characteristics

(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[1]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8455Bx						
V_{DD1}		All inputs 0 dc	—	1.6	2.4	mA
V_{DD2}		All inputs 0 dc	—	2.9	4.4	
V_{DD1}		All inputs 1 dc	—	7.0	10.5	
V_{DD2}		All inputs 1 dc	—	3.1	4.7	
Si8442Bx						
V_{DD1}		All inputs 0 dc	—	2.3	3.5	mA
V_{DD2}		All inputs 0 dc	—	2.3	3.5	
V_{DD1}		All inputs 1 dc	—	4.5	6.8	
V_{DD2}		All inputs 1 dc	—	4.5	6.8	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx						
V_{DD1}			—	4.3	6.5	mA
V_{DD2}			—	3.5	5.3	
Si8442Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.6	5.4	
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx						
V_{DD1}			—	4.3	6.5	mA
V_{DD2}			—	4.8	6.7	
Si8442Bx						
V_{DD1}			—	4.2	5.9	mA
V_{DD2}			—	4.2	5.9	

Notes:

1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Electrical Characteristics (Continued)
(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx V_{DD1} V_{DD2}			 — —	 4.4 16.8	 6.6 21	mA
Si8442Bx V_{DD1} V_{DD2}			 — —	 8.6 8.6	 10.8 10.8	mA
Timing Characteristics						
Si845xBx, Si8442Bx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si845xBx, Si8442Bx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.3	6.1	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.0	4.3	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[3]	t_{SU}		—	15	40	µs

Notes:
1. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1]

(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance[2]	Z_O		—	85	—	Ω
Enable Input High Current	I_{ENH}	V_{ENx} = V_{IH}	—	2.0	—	µA
Enable Input Low Current	I_{ENL}	V_{ENx} = V_{IL}	—	2.0	—	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8455Bx						
V_{DD1}		All inputs 0 DC	—	1.6	2.4	mA
V_{DD2}		All inputs 0 DC	—	2.9	4.4	
V_{DD1}		All inputs 1 DC	—	7.0	10.5	
V_{DD2}		All inputs 1 DC	—	3.1	4.7	
Si8442Bx						
V_{DD1}		All inputs 0 DC	—	2.3	3.5	mA
V_{DD2}		All inputs 0 DC	—	2.3	3.5	
V_{DD1}		All inputs 1 DC	—	4.5	6.8	
V_{DD2}		All inputs 1 DC	—	4.5	6.8	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx						
V_{DD1}			—	4.3	6.5	mA
V_{DD2}			—	3.5	5.3	
Si8442Bx						
V_{DD1}			—	3.6	5.4	mA
V_{DD2}			—	3.6	5.4	
10 Mbps Supply Current (All inputs = 5 MHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx						
V_{DD1}			—	4.3	6.5	mA
V_{DD2}			—	4.8	6.7	
Si8442Bx						
V_{DD1}			—	4.2	5.9	mA
V_{DD2}			—	4.2	5.9	

Notes:

1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8455Bx V_{DD1} V_{DD2}			 — —	 4.3 13.3	 6.5 16.6	mA
Si8442Bx V_{DD1} V_{DD2}			 — —	 7.2 7.2	 9.0 9.0	mA
Timing Characteristics						
Si845xBx, Si8442Bx						
Maximum Data Rate			0	—	1.0	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 2	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si845xBx, Si8442Bx						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6.0	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 2	3.0	6.0	9.5	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 2	—	1.5	2.5	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	2.0	3.0	ns
Channel-Channel Skew	t_{PSK}		—	0.5	1.8	ns

Notes:
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 5. Electrical Characteristics[1] (Continued)
(V_{DD1} = 2.70 V, V_{DD2} = 2.70 V, T_A = –40 to 125 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 2	—	4.8	6.5	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 2	—	3.2	4.6	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	—	25	—	kV/µs
Enable to Data Valid	t_{en1}	See Figure 1	—	5.0	8.0	ns
Enable to Data Tri-State	t_{en2}	See Figure 1	—	7.0	9.2	ns
Start-up Time[4]	t_{SU}		—	15	40	µs

Notes:
1. Specifications in this table are also valid at VDD1 = 2.6 V and VDD2 = 2.6 V when the operating temperature range is constrained to T_A = 0 to 85 °C.
2. The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 6. Regulatory Information*

CSA
The Si84xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
VDE
The Si84xx is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
60747-5-2: Up to 560 V_{peak} for basic insulation working voltage.
UL
The Si84xx is certified under UL1577 component recognition program. For more details, see File E257455.
***Note:** Regulatory Certifications apply to 1.0 kV_{RMS} rated devices which are production tested to 1.2 kV_{RMS} for 1 sec. For more information, see "5. Ordering Guide" on page 25.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			QSOP-16	
Nominal Air Gap (Clearance)	L(IO1)		3.6	mm
Nominal External Tracking (Creepage)	L(IO2)		3.6	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC 60112	600	V_{RMS}
Erosion Depth	ED		0.031	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	2.0	pF
Input Capacitance[2]	C_I		4.0	pF

Notes:
1. To determine resistance and capacitance, the Si84xx is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0844 Part 2) Ratings

Parameter	Test Condition	Specification
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II
	Rated Mains Voltages ≤ 600 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si84xxxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max		Unit
					Si844x QSOP-16	Si845x QSOP-16	
Case Temperature	T_S		—	—	150	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 105 °C/W (QSOP-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	210	215	mA
Device Power Dissipation[2]	P_D		—	—	275	415	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3 and 4.
2. The Si84xx is tested with VDD1 = VDD2 = 5.5 V, TJ = 150 ºC, CL = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Si84xx QSOP-16	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	105	°C/W

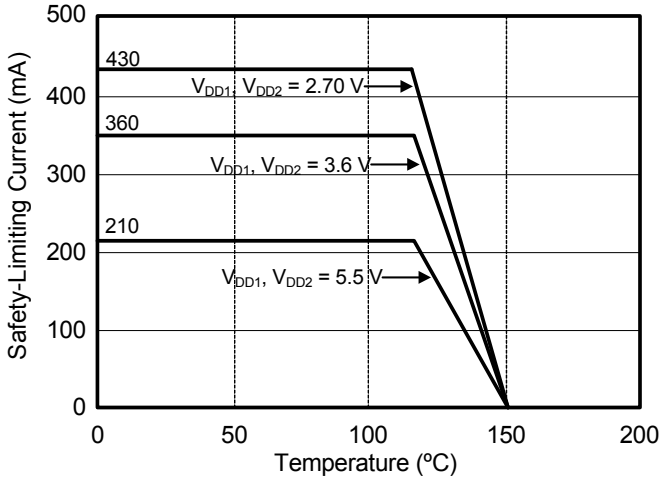


Figure 3. (Si844x, QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

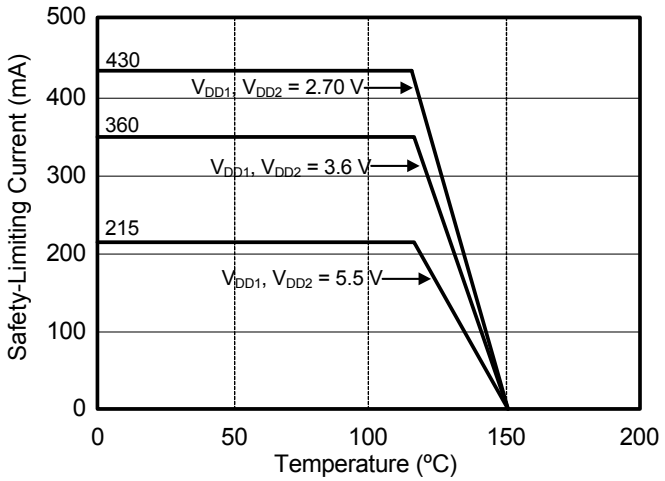


Figure 4. (Si845x, QSOP-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Functional Description

2.1. Theory of Operation

The operation of an Si84xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si84xx channel is shown in Figure 5.

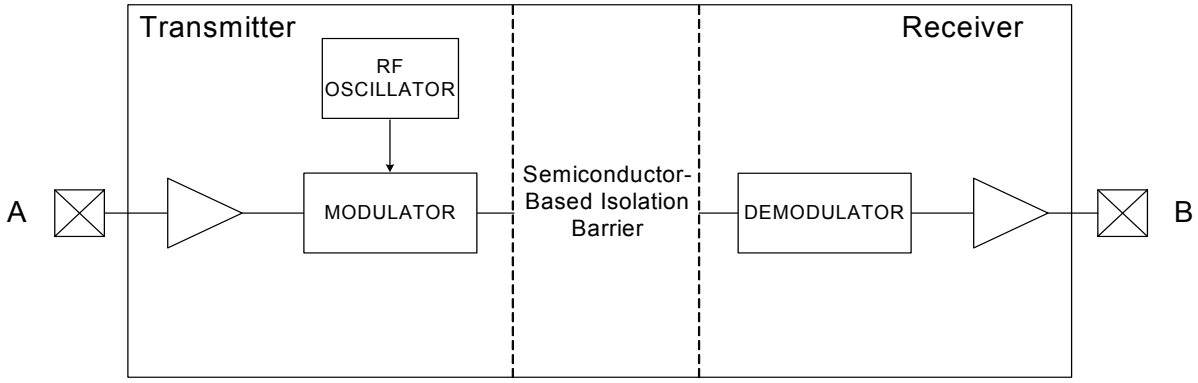


Figure 5. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 6 for more details.

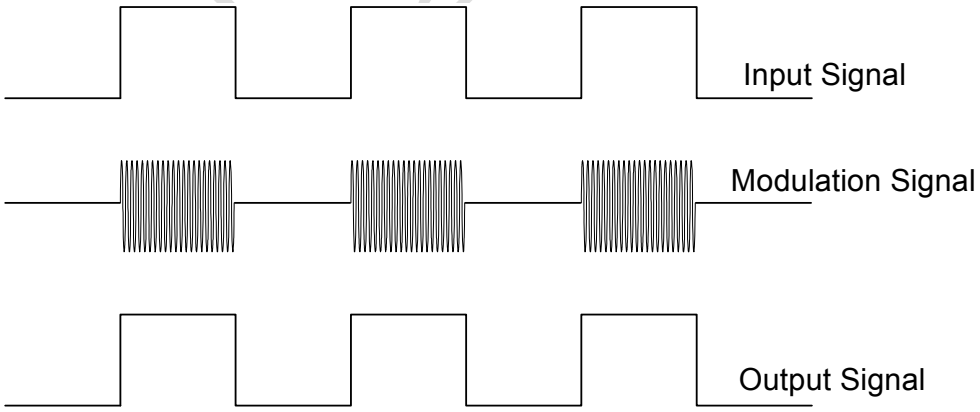


Figure 6. Modulation Scheme

2.2. Eye Diagram

Figure 7 illustrates an eye-diagram taken on an Si8455. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8455 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

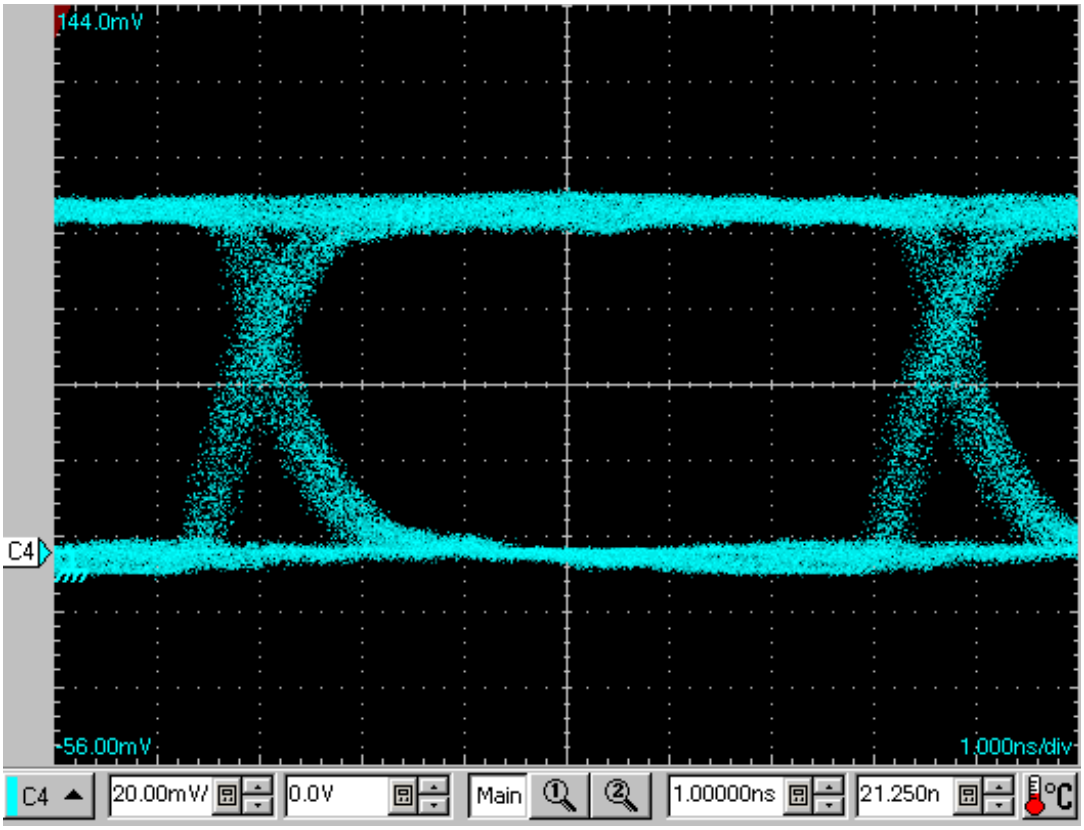


Figure 7. Eye Diagram

2.3. Device Operation

Device behavior during start-up, normal operation, and shutdown is shown in Table 12. Table 13 provides an overview of the output states when the Enable pins are active.

Table 12. Si84xx Logic Operation Table

V_I Input[1,2]	EN Input[1,2,3]	VDDI State[1,4,5]	VDDO State[1,4,5]	V_O Output[1,2]	Comments
H	H or NC	P	P	H	Enabled, normal operation.
L	H or NC	P	P	L	
X[6]	L	P	P	Hi-Z[7]	Disabled.
X[6]	H or NC	UP	P	L	Upon transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X[6]	L	UP	P	Hi-Z[7]	Disabled.
X[6]	X[6]	P	UP	Undetermined	Upon transition of VDDO from unpowered to powered, V_O returns to the same state as V_I within 1 µs, if EN is in either the H or NC state. Upon transition of VDDO from unpowered to powered, V_O returns to Hi-Z within 1 µs if EN is L.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals. EN is the enable control input located on the same output side.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. It is recommended that the enable inputs be connected to an external logic high or low level when the Si84xx is operating in noisy environments.
4. "Powered" state (P) is defined as 2.70 V < VDD < 5.5 V.
5. "Unpowered" state (UP) is defined as VDD = 0 V.
6. Note that an I/O can power the die for a given side through an internal diode if its source has adequate current.
7. When using the enable pin (EN) function, the output pin state goes into a high-impedance state when the EN pin is disabled (EN = 0).

Table 13. Enable Input Truth Table[1]

P/N	EN1[1,2]	EN2[1,2]	Operation
Si8442	H	X	Outputs A3 and A4 are enabled and follow input state.
	L	X	Outputs A3 and A4 are disabled and Logic Low or in high impedance state.[3]
	X	H	Outputs B1 and B2 are enabled and follow input state.
	X	L	Outputs B1 and B2 are disabled and Logic Low or in high impedance state.[3]
Si8455	—	—	Outputs B1, B2, B3, B4, B5 are enabled and follow input state.

Notes:

1. Enable inputs EN1 and EN2 can be used for multiplexing, for clock sync, or other output control. These inputs are internally pulled-up to local VDD by a 3 µA current source allowing them to be connected to an external logic level (high or low) or left floating. To minimize noise coupling, do not connect circuit traces to EN1 or EN2 if they are left floating. If EN1, EN2 are unused, it is recommended they be connected to an external logic level, especially if the Si845x is operating in a noisy environment.
2. X = not applicable; H = Logic High; L = Logic Low.
3. When using the enable pin (EN) function, the output pin state goes into a high-impedance state when the EN pin is disabled (EN = 0).

2.4. Layout Recommendations

To ensure safety in the end user application, high voltage circuits (i.e., circuits with >30 V_{AC}) must be physically separated from the safety extra-low voltage circuits (SELV is a circuit with <30 V_{AC}) by a certain distance (creepage/clearance). If a component, such as a digital isolator, straddles this isolation barrier, it must meet those creepage/clearance requirements and also provide a sufficiently large high-voltage breakdown protection rating (commonly referred to as working voltage protection). Refer to the end-system specification (61010-1, 60950-1, etc.) requirements before starting any design that uses a digital isolator.

The following sections detail the recommended bypass and decoupling components necessary to ensure robust overall performance and reliability for systems using the Si84xx digital isolators.

2.4.1. Supply Bypass

Digital integrated circuit components typically require 0.1 µF (100 nF) bypass capacitors when used in electrically quiet environments. However, digital isolators are commonly used in hazardous environments with excessively noisy power supplies. To counteract these harsh conditions, it is recommended that an additional 1 µF bypass capacitor be added between VDD and GND on both sides of the package. The capacitors should be placed as close as possible to the package to minimize stray inductance. If the system is excessively noisy, it is recommended that the designer add 50 to 100 Ω resistors in series with the VDD supply voltage source and 50 to 300 Ω resistors in series with the digital inputs/outputs (see Figure 8). For more details, see "3. Errata and Design Migration Guidelines" on page 23.

All components upstream or downstream of the isolator should be properly decoupled as well. If these components are not properly decoupled, their supply noise can couple to the isolator inputs and outputs, potentially causing damage if spikes exceed the maximum ratings of the isolator (6 V). In this case, the 50 to 300 Ω resistors protect the isolator's inputs/outputs (note that permanent device damage may occur if the absolute maximum ratings are exceeded). Functional operation should be restricted to the conditions specified in Table 1, “Recommended Operating Conditions,” on page 4.

2.4.2. Pin Connections

No connect pins are not internally connected. They can be left floating, tied to V_{DD}, or tied to GND.

2.4.3. Output Pin Termination

The nominal output impedance of an isolator driver channel is approximately 85 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces. The series termination resistor values should be scaled appropriately while keeping in mind the recommendations described in “2.4.1. Supply Bypass” above.

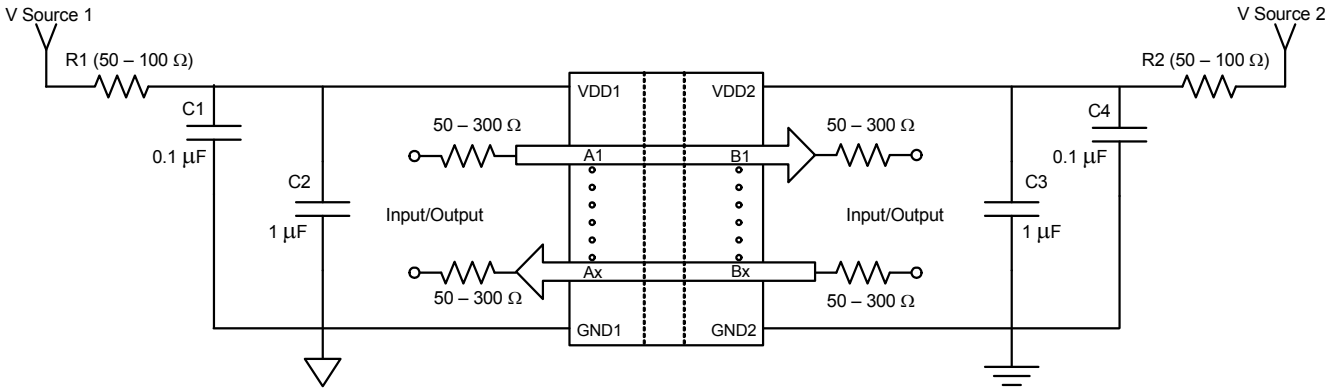


Figure 8. Recommended Bypass Components for the Si84xx Digital Isolator Family

2.5. Typical Performance Characteristics

The typical performance characteristics depicted in the following diagrams are for information purposes only. Refer to Tables 3, 4, and 5 for actual specification limits.

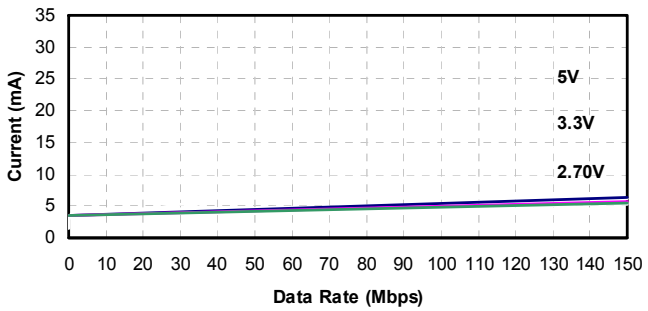


Figure 9. Si8455 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation

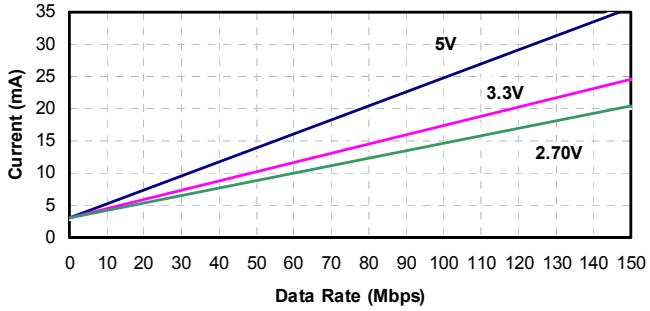


Figure 11. Si8455 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

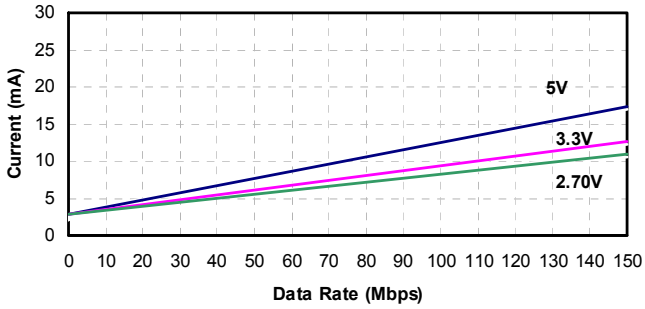


Figure 10. Si8442 Typical V_{DD1} or V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.70 V Operation (15 pF Load)

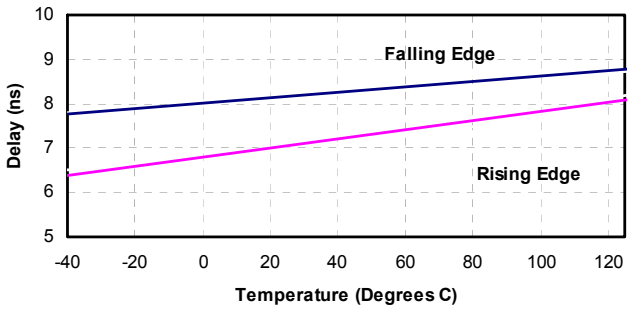


Figure 12. Propagation Delay vs. Temperature

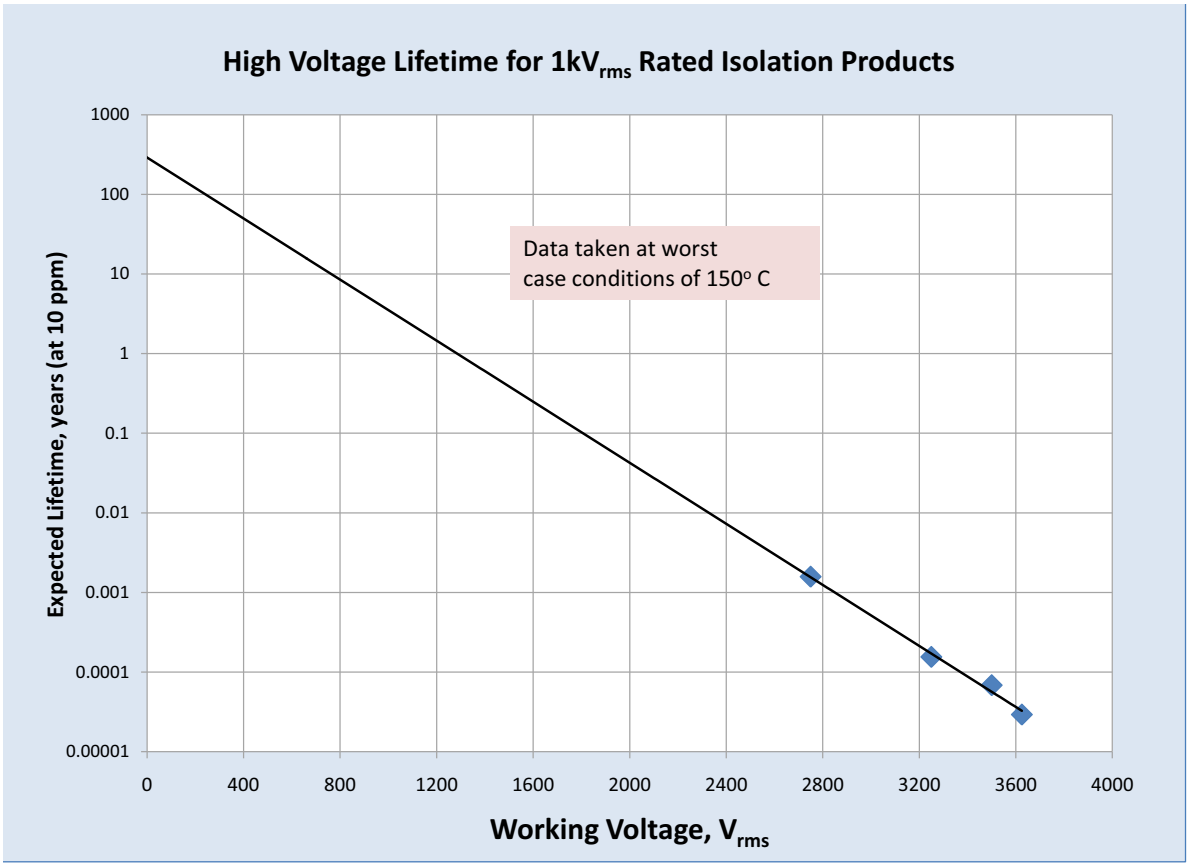


Figure 13. Si84xx Time-Dependent Dielectric Breakdown

3. Errata and Design Migration Guidelines

No errata exist for Revision D. However, the following recommendations apply to Revision D devices. See "5. Ordering Guide" on page 25 for more details.

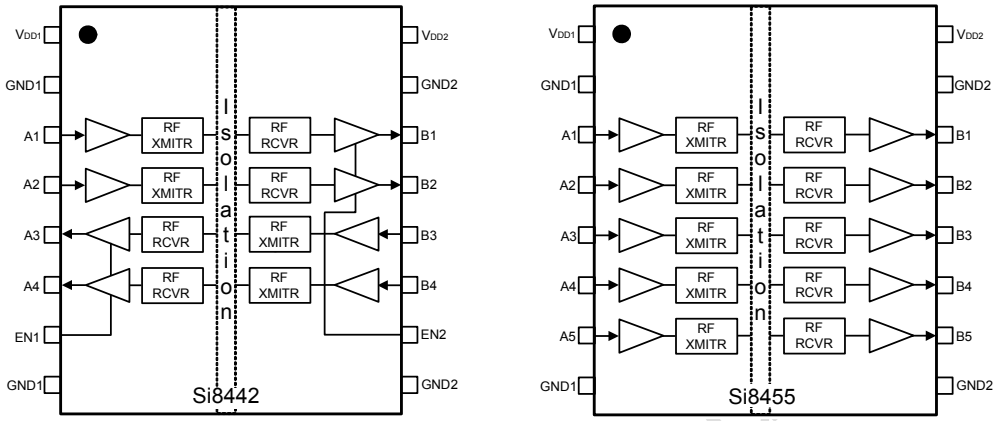
3.1. Power Supply Bypass Capacitors (Revision C and Revision D)

When using the Si844x isolators with power supplies ≥ 4.5 V, sufficient VDD bypass capacitors must be present on both the VDD1 and VDD2 pins to ensure the VDD rise time is less than 0.5 V/µs (which is > 9 µs for a ≥ 4.5 V supply). Although rise time is power supply dependent, ≥ 1 µF capacitors are required on both power supply pins (VDD1, VDD2) of the isolator device.

3.1.1. Resolution

For recommendations on resolving this issue, see "2.4.1. Supply Bypass" on page 20. Additionally, refer to "5. Ordering Guide" on page 25 for current ordering information.

4. Pin Descriptions



Name	SOIC-16 Pin#	Type	Description (Si8442)	Description (Si8455)
V_{DD1}	1	Supply	Side 1 power supply	Side 1 power supply
GND1	2	Ground	Side 1 ground	Side 1 ground
A1	3	Digital Input	Side 1 digital input	Side 1 digital input
A2	4	Digital Input	Side 1 digital input	Side 1 digital input
A3	5	Digital I/O	Side 1 digital output	Side 1 digital input
A4	6	Digital I/O	Side 1 digital output	Side 1 digital input
A5/EN1	7	Digital Input	Side 1 active high enable	Side 1 digital input
GND1	8	Ground	Side 1 ground	Side 1 ground
GND2	9	Ground	Side 2 ground	Side 2 ground
B5/EN2	10	Digital Input or Enable	Side 2 active high enable	Side 2 digital output
B4	11	Digital I/O	Side 2 digital input	Side 2 digital output
B3	12	Digital I/O	Side 2 digital input	Side 2 digital output
B2	13	Digital Output	Side 2 digital output	Side 2 digital output
B1	14	Digital Output	Side 2 digital output	Side 2 digital output
GND2	15	Ground	Side 2 ground	Side 2 ground
V_{DD2}	16	Supply	Side 2 power supply	Side 2 power supply

5. Ordering Guide

These devices are not recommended for new designs. Please see the Si864x or Si865x datasheet for replacement options.

Table 14. Ordering Guide for Valid OPNs*

Ordering Part Number (OPN)	Alternative Part Number (APN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Package Type
Si8442BA-D-IU	Si8642BA-C-IU	2	2	150	1 kVrms	QSOP-16
Si8455BA-B-IU	Si8655BA-C-IU	5	0	150	1 kVrms	

***Note:** All packages are RoHS-compliant. Moisture sensitivity level is MSL2A with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications and peak solder temperature.

6. Package Outline: 16-Pin QSOP

Figure 14 illustrates the package details for the Si84xx in a 16-pin QSOP package. Table 15 lists the values for the dimensions shown in the illustration.

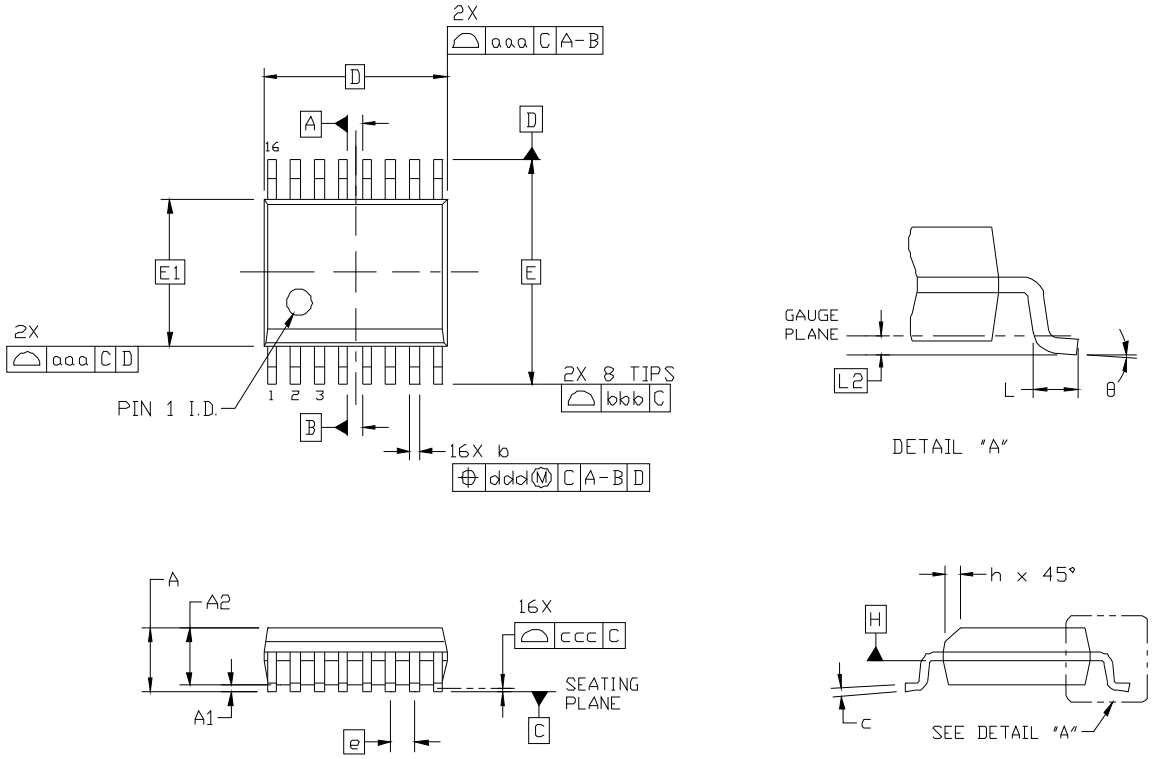


Figure 14. 16-pin QSOP Package

Table 15. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.20	0.30
c	0.17	0.25
D	4.89 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	0.635 BSC	
L	0.40	1.27
L2	0.25 BSC	
h	0.25	0.50

Table 15. Package Diagram Dimensions (Continued)

Dimension	Min	Max
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation AB.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Land Pattern: 16-Pin QSOP

Figure 15 illustrates the recommended land pattern details for the Si84xx in a 16-pin QSOP. Table 16 lists the values for the dimensions shown in the illustration.

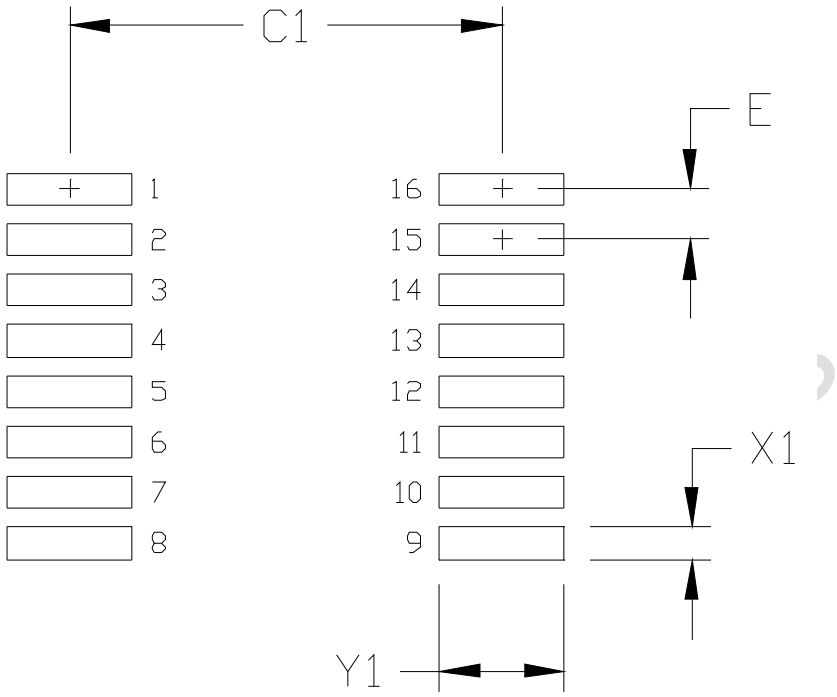


Figure 15. 16-Pin QSOP PCB Land Pattern

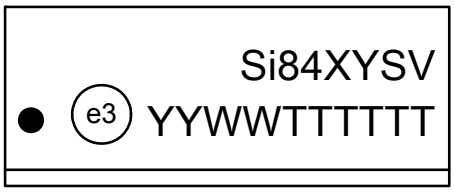
Table 16. 16-Pin QSOP Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	0.635
X1	Pad Width	0.40
Y1	Pad Length	1.55

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOP63P602X173-16N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

8. Top Marking: 16-Pin QSOP

8.1. 16-Pin QSOP Top Marking



8.2. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (5, 4) Y = # of reverse channels (2, 0)* S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV
Line 2 Marking:	Circle = 1.2 mm Diameter	"e3" Pb-Free Symbol
	YY = Year WW = Work Week	Assigned by the assembly subcontractor. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg code	Manufacturing code from assembly purchase order form.
	Circle = 1.2 mm diameter	"e3" Pb-Free Symbol.
***Note:** Si8455 has 0 reverse channels.		

Document Change List

Revision 0.1 to Revision 1.0

- Changed document name from Si84x/5x QSOP to Si844x/5x QSOP.
- Updated " Features" on page 1.
- Moved Tables 1 and 2 to page 4.
- Updated Tables 6, 7, 8, and 9.
- Updated Table 12 footnotes.
- Added Figure 13, “Si84xx Time-Dependent Dielectric Breakdown,” on page 22.

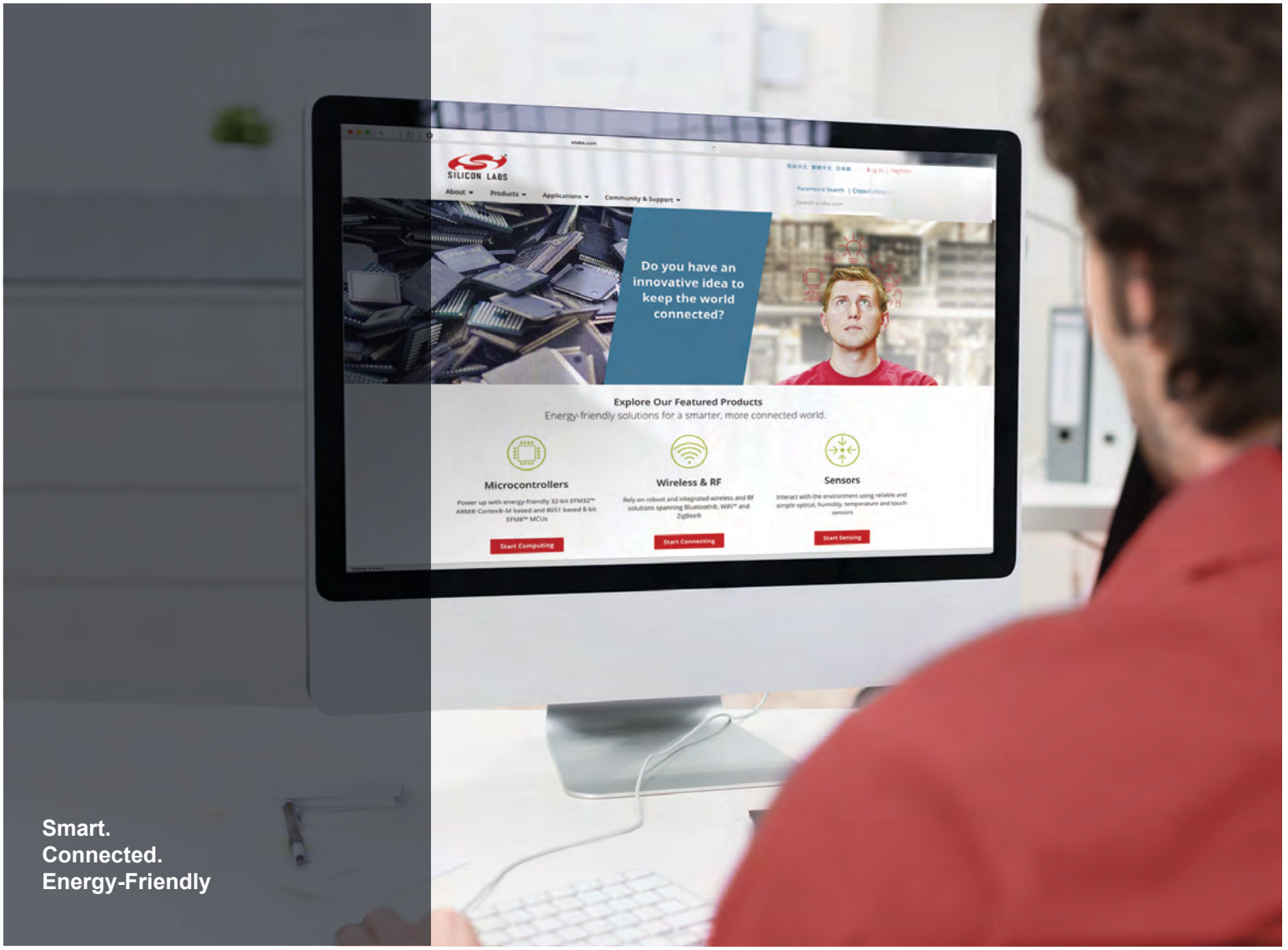
Revision 1.0 to Revision 1.1

- Deleted all references to 2.5 kV_{RMS}
- Updated Table 6, “Regulatory Information*,” on page 12.
- Updated Figure 13, “Si84xx Time-Dependent Dielectric Breakdown,” on page 22.
- Updated "2.4.1. Supply Bypass" on page 20.
- Added Figure 8, “Recommended Bypass Components for the Si84xx Digital Isolator Family,” on page 20.
- Updated "3.1. Power Supply Bypass Capacitors (Revision C and Revision D)" on page 23.

Revision 1.1 to Revision 1.2

- Updated "5. Ordering Guide" on page 25 to include new title note and “ Alternative Part Number (APN)” column.

NOTES:



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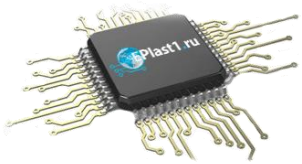

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