

FEATURES

12-Bit CMOS MDAC with Output Amplifier
 4-Quadrant Multiplication
 Guaranteed Monotonic (T_{MIN} to T_{MAX})
 Space-Saving 0.3" DIPs and 24- or 28-Terminal Surface Mount Packages
 Application Resistors On Chip for Gain Ranging, etc.
 Low Power LC²MOS

APPLICATIONS

Automatic Test Equipment
 Digital Attenuators
 Programmable Power Supplies
 Programmable Gain Amplifiers
 Digital-to-4-20 mA Converters

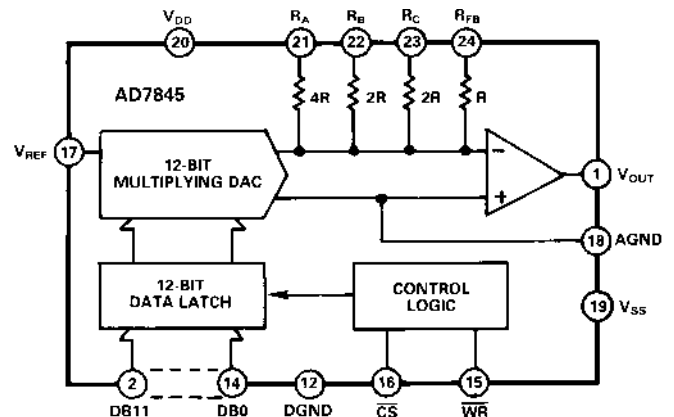
GENERAL DESCRIPTION

The AD7845 is the industry's first 4-quadrant multiplying D/A converter with an on-chip amplifier. It is fabricated on the LC²MOS process, which allows precision linear components and digital circuitry to be implemented on the same chip.

The 12 data inputs drive latches which are controlled by standard \overline{CS} and \overline{WR} signals, making microprocessor interfacing simple. For stand-alone operation, the \overline{CS} and \overline{WR} inputs can be tied to ground, making all latches transparent. All digital inputs are TTL and 5 V CMOS compatible.

The output amplifier can supply ± 10 V into a 2 k Ω load. It is internally compensated, and its input offset voltage is low due to laser trimming at wafer level. For normal operation, R_{FB} is tied to V_{OUT} , but the user may alternatively choose R_A , R_B or R_C to scale the output voltage range.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT HIGHLIGHTS

- 1. Voltage Output Multiplying DAC**
 The AD7845 is the first DAC which has a full 4-quadrant multiplying capability and an output amplifier on chip. All specifications include amplifier performance.
- 2. Matched Application Resistors**
 Three application resistors provide an easy facility for gain ranging, voltage offsetting, etc.
- 3. Space Saving**
 The AD7845 saves space in two ways. The integration of the output amplifier on chip means that chip count is reduced. The part is housed in skinny 24-lead 0.3" DIP, 28-terminal LCC and PLCC and 24-terminal SOIC packages.

REV. B

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AD7845—SPECIFICATIONS¹ ($V_{DD} = +15\text{ V}, \pm 5\%$, $V_{SS} = -15\text{ V}, \pm 5\%$, $V_{REF} = +10\text{ V}$, $AGND = DGND = 0\text{ V}$, V_{OUT} connected to R_{FB} . V_{OUT} load = $2\text{ k}\Omega$, 100 pF . All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

| Parameter | J Version | K Version | A Version | B Version | S Version | T Version | Units | Test Conditions/Comments |
|--|---------------|---------------|---------------|---------------|---------------|---------------|-------------------|---|
| ACCURACY | | | | | | | | |
| Resolution | 12 | 12 | 12 | 12 | 12 | 12 | Bits | $1\text{ LSB} = \frac{V_{REF}}{2^{12}} = 2.4\text{ mV}$ |
| Relative Accuracy at +25°C | ±1 | ±1/2 | ±1 | ±1/2 | ±1 | ±1/2 | LSB max | All Grades Are Guaranteed Monotonic over Temperature DAC Register Loaded with All 0s. |
| T_{MIN} to T_{MAX} | ±1 | ±3/4 | ±1 | ±3/4 | ±1 | ±3/4 | LSB max | |
| Differential Nonlinearity | ±1 | ±1 | ±1 | ±1 | ±1 | ±1 | LSB max | |
| Zero Code Offset Error at +25°C | ±2 | ±1 | ±2 | ±1 | ±2 | ±1 | mV max | |
| T_{MIN} to T_{MAX} | ±3 | ±2 | ±3 | ±2 | ±4 | ±3 | mV max | |
| Offset Temperature Coefficient; $(\Delta\text{Offset}/\Delta\text{Temperature})^2$ | ±5 | ±5 | ±5 | ±5 | ±5 | ±5 | µV/°C typ | |
| Gain Error | ±3 | ±2 | ±3 | ±2 | ±3 | ±2 | LSB max | |
| | ±6 | ±6 | ±6 | ±6 | ±6 | ±6 | LSB max | |
| | ±6 | ±6 | ±6 | ±6 | ±6 | ±6 | LSB max | |
| | ±7 | ±7 | ±7 | ±7 | ±7 | ±7 | LSB max | |
| Gain Temperature Coefficient; $(\Delta\text{Gain}/\Delta\text{Temperature})^2$ | ±2 | ±2 | ±2 | ±2 | ±2 | ±2 | ppm of FSR/°C typ | R_{FB} , V_{OUT} Connected |
| REFERENCE INPUT | | | | | | | | |
| Input Resistance, Pin 17 | 8 | 8 | 8 | 8 | 8 | 8 | kΩ min | Typical Input Resistance = 12 kΩ |
| | 16 | 16 | 16 | 16 | 16 | 16 | kΩ max | |
| APPLICATION RESISTOR RATIO MATCHING | | | | | | | | |
| | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | % max | Matching Between R_A , R_B , R_C |
| DIGITAL INPUTS | | | | | | | | |
| V_{IH} (Input High Voltage) | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | 2.4 | V min | Digital Inputs at 0 V and V_{DD} |
| V_{IL} (Input Low Voltage) | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | 0.8 | V max | |
| I_{IN} (Input Current) | ±1 | ±1 | ±1 | ±1 | ±1 | ±1 | µA max | |
| C_{IN} (Input Capacitance) ² | 7 | 7 | 7 | 7 | 7 | 7 | pF max | |
| POWER SUPPLY⁴ | | | | | | | | |
| V_{DD} Range | 14.25/15.75 | 14.25/15.75 | 14.25/15.75 | 14.25/15.75 | 14.25/15.75 | 14.25/15.75 | V min/V max | $V_{DD} = +15\text{ V} \pm 5\%$, $V_{REF} = -10\text{ V}$ $V_{SS} = -15\text{ V} \pm 5\%$. |
| V_{SS} Range | -14.25/-15.75 | -14.25/-15.75 | -14.25/-15.75 | -14.25/-15.75 | -14.25/-15.75 | -14.25/-15.75 | V min/V max | |
| Power Supply Rejection | | | | | | | | |
| $\Delta\text{Gain}/\Delta V_{DD}$ | ±0.01 | ±0.01 | ±0.01 | ±0.01 | ±0.01 | ±0.01 | % per % max | |
| $\Delta\text{Gain}/\Delta V_{SS}$ | ±0.01 | ±0.01 | ±0.01 | ±0.01 | ±0.01 | ±0.01 | % per % max | |
| I_{DD} | 6 | 6 | 6 | 6 | 6 | 6 | mA max | |
| I_{SS} | 4 | 4 | 4 | 4 | 4 | 4 | mA max | V_{OUT} Unloaded V_{OUT} Unloaded |

AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance and are not subject to test.

| | | | | | | | | |
|--|-----|-----|-----|-----|-----|-----|------------|--|
| DYNAMIC PERFORMANCE | | | | | | | | |
| Output Voltage Settling Time | 5 | 5 | 5 | 5 | 5 | 5 | µs max | To 0.01% of Full-Scale Range V_{OUT} Load = $2\text{ k}\Omega$, 100 pF . DAC Register Alternately Loaded with All 0s and All 1s. Typically $2.5\text{ }\mu\text{s}$ at 25°C. |
| Slew Rate | 11 | 11 | 11 | 11 | 11 | 11 | V/µs typ | V_{OUT} Load = $2\text{ k}\Omega$, 100 pF . Measured with $V_{REF} = 0\text{ V}$. DAC Register Alternately Loaded with All 0s and All 1s. |
| Digital-to-Analog Glitch Impulse | 55 | 55 | 55 | 55 | 55 | 55 | nV-s typ | |
| Multiplying Feedthrough Error ³ | 5 | 5 | 5 | 5 | 5 | 5 | mV p-p typ | $V_{REF} = \pm 10\text{ V}$, 10 kHz Sine Wave DAC Register Loaded with All 0s. |
| Unity Gain Small Signal Bandwidth | 600 | 600 | 600 | 600 | 600 | 600 | kHz typ | V_{OUT} , R_{FB} Connected. DAC Loaded with All 1s $V_{REF} = 100\text{ mV p-p}$ Sine Wave. |
| Full Power Bandwidth | 175 | 175 | 175 | 175 | 175 | 175 | kHz typ | V_{OUT} , R_{FB} Connected. DAC Loaded with All 1s. $V_{REF} = 20\text{ V p-p}$ Sine Wave. $R_L = 2\text{ k}\Omega$. |
| Total Harmonic Distortion | -90 | -90 | -90 | -90 | -90 | -90 | dB typ | $V_{REF} = 6\text{ V rms}$, 1 kHz Sine Wave. |
| OUTPUT CHARACTERISTICS⁵ | | | | | | | | |
| Open Loop Gain | 85 | 85 | 85 | 85 | 85 | 85 | dB min | V_{OUT} , R_{FB} Not Connected $V_{OUT} = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$ |
| Output Voltage Swing | ±10 | ±10 | ±10 | ±10 | ±10 | ±10 | V min | $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$ |
| Output Resistance | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | Ω typ | R_{FB} , V_{OUT} Connected, |
| Short Circuit Current @ +25°C | 11 | 11 | 11 | 11 | 11 | 11 | mA typ | V_{OUT} Shorted to AGND |
| Output Noise Voltage (0.1 Hz to 10 Hz) @ +25°C | 2 | 2 | 2 | 2 | 2 | 2 | µV rms typ | Includes Noise Due to Output Amplifier and Johnson Noise of R_{FB} |
| $f = 10\text{ Hz}$ | 250 | 250 | 250 | 250 | 250 | 250 | nV/√Hz typ | |
| $f = 100\text{ Hz}$ | 100 | 100 | 100 | 100 | 100 | 100 | nV/√Hz typ | |
| $f = 1\text{ kHz}$ | 50 | 50 | 50 | 50 | 50 | 50 | nV/√Hz typ | |
| $f = 10\text{ kHz}$ | 50 | 50 | 50 | 50 | 50 | 50 | nV/√Hz typ | |
| $f = 100\text{ kHz}$ | 50 | 50 | 50 | 50 | 50 | 50 | nV/√Hz typ | |

NOTES

¹Temperature ranges are as follows: J, K Versions: 0°C to +70°C; A, B Versions: -40°C to +85°C; S, T Versions: -55°C to +125°C.

²Guaranteed by design and characterization, not production tested.

³The metal lid on the ceramic D-24A package is connected to Pin 12 (DGND).

⁴The device is functional with a power supply of ±12 V.

⁵Minimum specified load resistance is 2 kΩ.

Specifications subject to change without notice.

TIMING CHARACTERISTICS¹ ($V_{DD} = +15\text{ V}, \pm 5\%$. $V_{SS} = -15\text{ V}, \pm 5\%$. $V_{REF} = +10\text{ V}$. $AGND = DGND = 0\text{ V}$.)

| Parameter | Limit at T_{MIN} to T_{MAX} (All Versions) | Units | Test Conditions/Comments |
|-----------|---|--------|---------------------------------|
| t_{CS} | 30 | ns min | Chip Select to Write Setup Time |
| t_{CH} | 0 | ns min | Chip Select to Write Hold Time |
| t_{WR} | 30 | ns min | Write Pulsewidth |
| t_{DS} | 80 | ns min | Data Setup Time |
| t_{DH} | 0 | ns min | Data Hold Time |

NOTES

¹Guaranteed by design and characterization, not production tested.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

($T_A = +25^\circ\text{C}$ unless otherwise stated)

| | | |
|---------------------------------|-------|--|
| V_{DD} to DGND | | -0.3 V to +17 V |
| V_{SS} to DGND | | +0.3 V to -17 V |
| V_{REF} to AGND | | $V_{DD} + 0.3\text{ V}, V_{SS} - 0.3\text{ V}$ |
| V_{RFB} to AGND | | $V_{DD} + 0.3\text{ V}, V_{SS} - 0.3\text{ V}$ |
| V_{RA} to AGND | | $V_{DD} + 0.3\text{ V}, V_{SS} - 0.3\text{ V}$ |
| V_{RB} to AGND | | $V_{DD} + 0.3\text{ V}, V_{SS} - 0.3\text{ V}$ |
| V_{RC} to AGND | | $V_{DD} + 0.3\text{ V}, V_{SS} - 0.3\text{ V}$ |
| V_{OUT} to AGND ² | | $V_{DD} + 0.3\text{ V}, V_{SS} - 0.3\text{ V}$ |
| AGND to DGND | | -0.3 V, V_{DD} |
| Digital Input Voltage to DGND | | -0.3 V to $V_{DD} + 0.3\text{ V}$ |
| Power Dissipation (Any Package) | | |
| To +75°C | | 650 mW |
| Derates above +75°C | | 10 mW/°C |

Operating Temperature Range

| | | |
|--------------------------------------|-------|-----------------|
| Commercial (J, K Versions) | | 0°C to +70°C |
| Industrial (A, B Versions) | | -40°C to +85°C |
| Extended (S, T Versions) | | -55°C to +125°C |
| Storage Temperature Range | | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | | +300°C |

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

² V_{OUT} may be shorted to AGND provided that the power dissipation of the package is not exceeded.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7845 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

**ORDERING GUIDE¹**

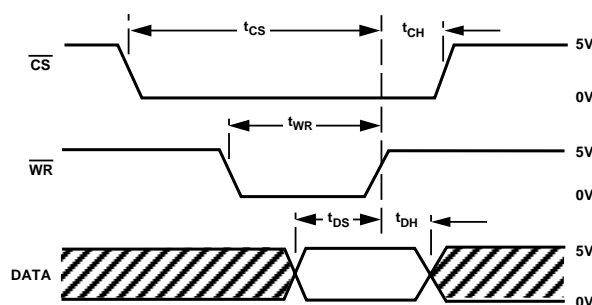
| Model ² | Temperature Range | Relative Accuracy @ +25°C | Package Option ³ |
|--------------------|-------------------|---------------------------|-----------------------------|
| AD7845JN | 0°C to +70°C | ±1 LSB | N-24 |
| AD7845KN | 0°C to +70°C | ±1/2 LSB | N-24 |
| AD7845JP | 0°C to +70°C | ±1 LSB | P-28A |
| AD7845KP | 0°C to +70°C | ±1/2 LSB | P-28A |
| AD7845JR | 0°C to +70°C | ±1 LSB | R-24 |
| AD7845KR | 0°C to +70°C | ±1/2 LSB | R-24 |
| AD7845AQ | -40°C to +85°C | ±1 LSB | Q-24 |
| AD7845BQ | -40°C to +85°C | ±1/2 LSB | Q-24 |
| AD7845AR | -40°C to +85°C | ±1 LSB | R-24 |
| AD7845BR | -40°C to +85°C | ±1/2 LSB | R-24 |
| AD7845SQ/883B | -55°C to +125°C | ±1 LSB | Q-24 |
| AD7845TQ/883B | -55°C to +125°C | ±1/2 LSB | Q-24 |
| AD7845SE/883B | -55°C to +125°C | ±1 LSB | E-28A |

NOTES

¹Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.

²To order MIL-STD-883, Class B processed parts, add /883B to part number.

³E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.



NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_R = t_F = 20\text{ ns}$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

Figure 1. AD7845 Timing Diagram

Typical Performance Characteristics—AD7845

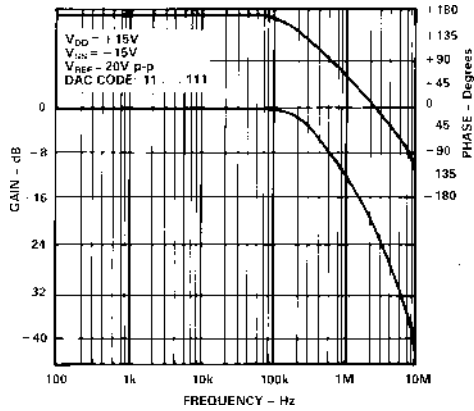


Figure 2. Frequency Response, $G = -1$

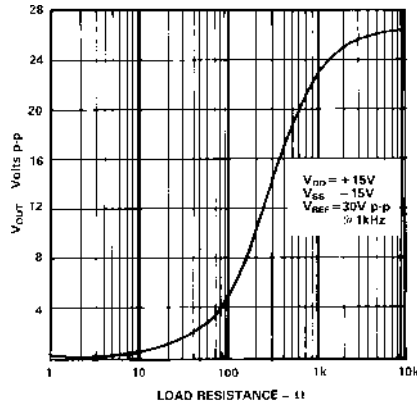


Figure 3. Output Voltage Swing vs. Resistive Load

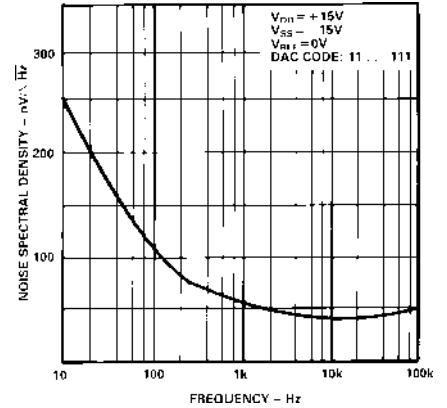


Figure 4. Noise Spectral Density

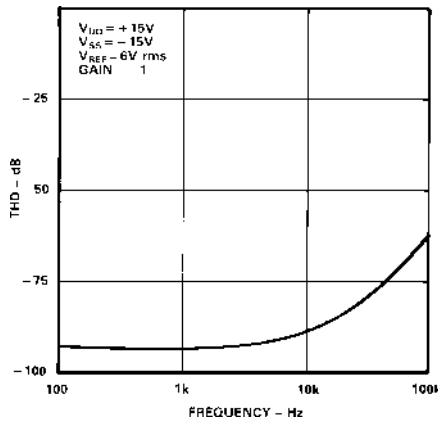


Figure 5. THD vs. Frequency

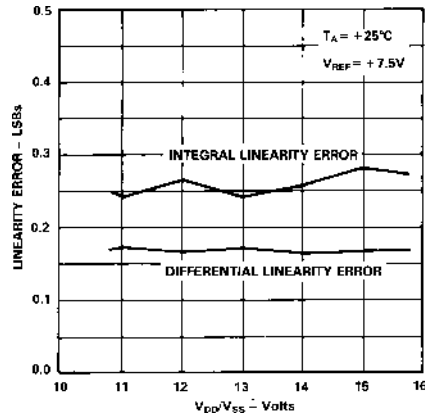


Figure 6. Typical AD7845 Linearity vs. Power Supply

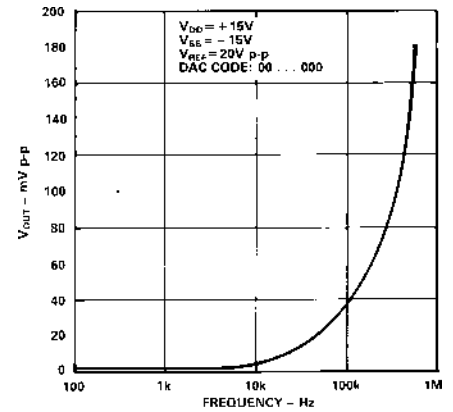


Figure 7. Multiplying Feedthrough Error vs. Frequency

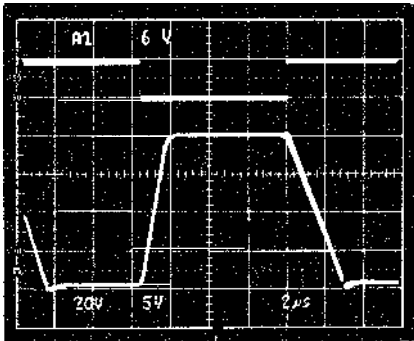


Figure 8. Unity Gain Inverter Pulse Response (Large Signal)

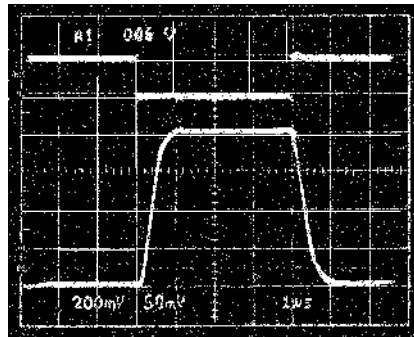


Figure 9. Unity Gain Inverter Pulse Response (Small Signal)

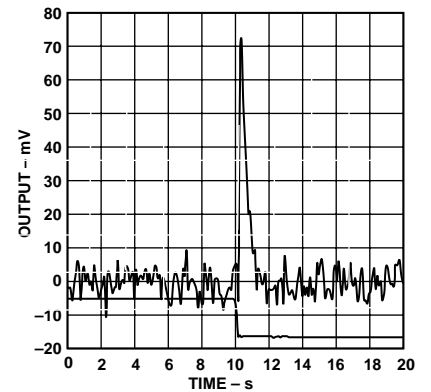


Figure 10. Digital-to-Analog Glitch Impulse (All 1s to All 0s Transition)

AD7845

PIN FUNCTION DESCRIPTION (DIP)

| Pin | Mnemonic | Description |
|-------|------------------|--|
| 1 | V _{OUT} | Voltage Output Terminal |
| 2-11 | DB11-DB2 | Data Bit 11 (MSB) to Data Bit 2 |
| 12 | DGND | Digital Ground. The metal lid on the ceramic package is connected to this pin |
| 13-14 | DB1-DB0 | Data Bit 1 to Data Bit 0 (LSB) |
| 15 | \overline{WR} | Write Input. Active low |
| 16 | \overline{CS} | Chip Select Input. Active low |
| 17 | V _{REF} | Reference Input Voltage which can be an ac or dc signal |
| 18 | AGND | Analog Ground. This is the reference point for external analog circuitry |
| 19 | V _{SS} | Negative power supply for the output amplifier (nominal -12 V to +15 V) |
| 20 | V _{DD} | Positive power supply (nominal +12 V to +15 V) |
| 21 | R _A | Application resistor. R _A = 4 R _{FB} |
| 22 | R _B | Application resistor. R _B = 2 R _{FB} |
| 23 | R _C | Application resistor. R _C = 2 R _{FB} |
| 24 | R _{FB} | Feedback resistor in the DAC. For normal operation this is connected to V _{OUT} |

CIRCUIT INFORMATION

Digital Section

Figure 11 is a simplified circuit diagram of the AD7845 input control logic. When \overline{CS} and \overline{WR} are both low, the DAC latch is loaded with the data on the data inputs. All the digital inputs are TTL, HCMOS and +5 V CMOS compatible, facilitating easy microprocessor interfacing. All digital inputs incorporate standard protection circuitry.

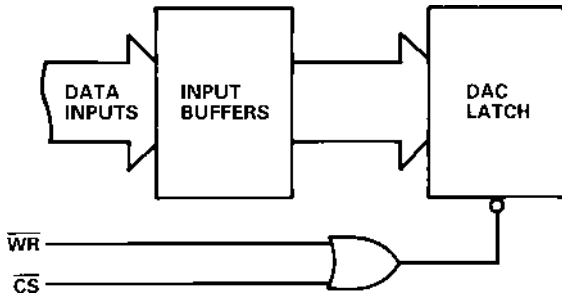


Figure 11. AD7845 Input Control Logic

D/A Section

Figure 12 shows a simplified circuit diagram for the AD7845 D/A section and output amplifier.

A segmented scheme is used whereby the 2 MSBs of the 12-bit data word are decoded to drive the three switches A-C. The remaining 10 bits drive the switches (S0-S9) in a standard R-2R ladder configuration.

Each of the switches A-C steers 1/4 of the total reference current with the remaining 1/4 passing through the R-2R section.

An output amplifier and feedback resistor perform the current-to-voltage conversion giving

$$V_{OUT} = -D \times V_{REF}$$

where D is the fractional representation of the digital word. (D can be set from 0 to 4095/4096.)

The amplifier can maintain ± 10 V across a 2 k Ω load. It is internally compensated and settles to 0.01% FSR (1/2 LSB) in less than 5 μ s. The input offset voltage is laser trimmed at wafer level. The amplifier slew rate is typically 11 V/ μ s, and the unity gain small signal bandwidth is 600 kHz. There are three extra on-chip resistors (R_A, R_B, R_C) connected to the amplifier inverting terminal. These are useful in a number of applications including offset adjustment and gain ranging.

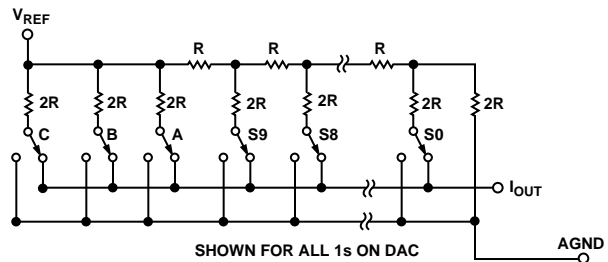


Figure 12. Simplified Circuit Diagram for the AD7845 D/A Section

UNIPOLAR BINARY OPERATION

Figure 13 shows the AD7845 connected for unipolar binary operation. When V_{IN} is an ac signal, the circuit performs 2-quadrant multiplication. The code table for Figure 13 is given in Table I.

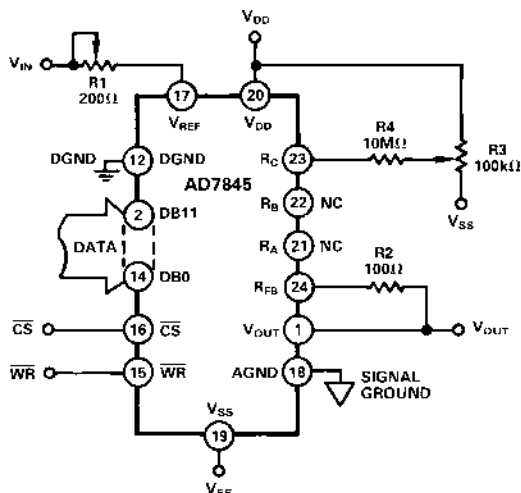


Figure 13. Unipolar Binary Operation

Table I. Unipolar Binary Code Table for AD7845

| Binary Number In DAC Register | | | Analog Output, V_{OUT} |
|-------------------------------|------|------|--|
| MSB | LSB | | |
| 1111 | 1111 | 1111 | $-V_{IN} \left(\frac{4095}{4096} \right)$ |
| 1000 | 0000 | 0000 | $-V_{IN} \left(\frac{2048}{4096} \right) = -1/2 V_{IN}$ |
| 0000 | 0000 | 0001 | $-V_{IN} \left(\frac{1}{4096} \right)$ |
| 0000 | 0000 | 0000 | 0 V |

OFFSET AND GAIN ADJUSTMENT FOR FIGURE 13

Zero Offset Adjustment

1. Load DAC with all 0s.
2. Trim R3 until $V_{OUT} = 0$ V.

Gain Adjustment

1. Load DAC with all 1s.
2. Trim R1 so that $V_{OUT} = -V_{IN} \frac{4095}{4096}$.

In fixed reference applications, full scale can also be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude. For high temperature applications, resistors and potentiometers should have a low temperature coefficient.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

The recommended circuit for bipolar operation is shown in Figure 14. Offset binary coding is used.

The offset specification of this circuit is determined by the matching of internal resistors R_B and R_C and by the zero code offset error of the device. Gain error may be adjusted by varying the ratio of R1 and R2.

To use this circuit without trimming and keep within the gain error specifications, resistors R1 and R2 should be ratio matched to 0.01%.

The code table for Figure 14 is given in Table II.

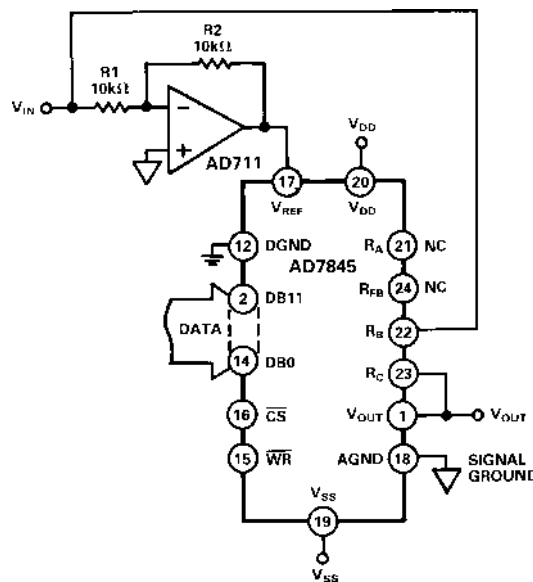


Figure 14. Bipolar Offset Binary Operation

Table II. Bipolar Code Table for Offset Binary Circuit of Figure 14

| Binary Number In DAC Register | | | Analog Output, V_{OUT} |
|-------------------------------|------|------|--|
| MSB | LSB | | |
| 1111 | 1111 | 1111 | $+V_{IN} \left(\frac{2047}{2048} \right)$ |
| 1000 | 0000 | 0001 | $+V_{IN} \left(\frac{1}{2048} \right)$ |
| 1000 | 0000 | 0000 | 0 V |
| 0111 | 1111 | 1111 | $-V_{IN} \left(\frac{1}{2048} \right)$ |
| 0000 | 0000 | 0000 | $-V_{IN} \left(\frac{2048}{2048} \right) = -V_{IN}$ |

AD7845

APPLICATIONS CIRCUITS

PROGRAMMABLE GAIN AMPLIFIER (PGA)

The AD7845 performs a PGA function when connected as in Figure 15. In this configuration, the R-2R ladder is connected in the amplifier feedback loop. R_{FB} is the amplifier input resistor. As the code decreases, the R-2R ladder resistance increases and so the gain increases.

$$V_{OUT} = -V_{IN} \times \frac{R_{DAC}}{D} \times \frac{1}{R_{FB}}, \left(D = 0 \text{ to } \frac{4095}{4096} \right)$$

$$= -V_{IN} \times \frac{R_{DAC}}{D} \times \frac{1}{R_{DAC}} = \frac{-V_{IN}}{D}, \text{ since } R_{FB} = R_{DAC}$$

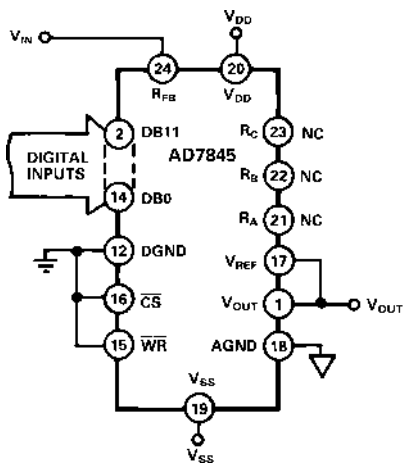


Figure 15. AD7845 Connected as PGA

As the programmed gain increases, the error and noise also increase. For this reason, the maximum gain should be limited to 256. Table III shows gain versus code.

Note that instead of using R_{FB} as the input resistor, it is also possible to use combinations of the other application resistors, R_A , R_B and R_C . For instance, if R_B is used instead of R_{FB} , the gain range for the same codes of Table II now goes from 1/2 to 128.

Table III. Gain and Error vs. Input Code for Figure 15

| Digital Inputs | | | Gain | Error (%) |
|----------------|------|------|-----------------------|-----------|
| 1111 | 1111 | 1111 | $4096/4095 \approx 1$ | 0.04 |
| 1000 | 0000 | 0000 | 2 | 0.07 |
| 0100 | 0000 | 0000 | 4 | 0.13 |
| 0010 | 0000 | 0000 | 8 | 0.26 |
| 0001 | 0000 | 0000 | 16 | 0.51 |
| 0000 | 1000 | 0000 | 32 | 1.02 |
| 0000 | 0100 | 0000 | 64 | 2.0 |
| 0000 | 0010 | 0000 | 128 | 4.0 |
| 0000 | 0001 | 0000 | 256 | 8.0 |

PROGRAMMABLE CURRENT SOURCES

The AD7845 is ideal for designing programmable current sources using a minimum of external components. Figures 16 and 17 are examples. The circuit of Figure 16 drives a programmable current I_L into a load referenced to a negative supply. Figure 17 shows the circuit for sinking a programmable current, I_L . The same set of circuit equations apply for both diagrams.

$$I_L = I_3 = I_2 + I_1$$

$$I_1 = \frac{D \times |V_{IN}|}{R_{DAC}}, \left(D = 0 \text{ to } \frac{4095}{4096} \right)$$

$$I_2 = \frac{1}{R1} \left(\frac{D \times |V_{IN}|}{R_{DAC}} \right) R_{FB} = \frac{D \times |V_{IN}|}{R1}, \text{ since } R_{FB} = R_{DAC}$$

$$I_L = \frac{D \times |V_{IN}|}{R1} + \frac{D \times |V_{IN}|}{R_{DAC}}$$

$$= \frac{D \times |V_{IN}|}{R1} \times \left(1 + \frac{R1}{R_{DAC}} \right)$$

Note that by making $R1$ much smaller than R_{DAC} , the circuit becomes insensitive to both the absolute value of R_{DAC} and its temperature variations. Now, the only resistor determining load current I_L is the sense resistor $R1$.

If $R1 = 100 \Omega$, then the programming range is 0 mA to 100 mA, and the resolution is 0.024 mA.

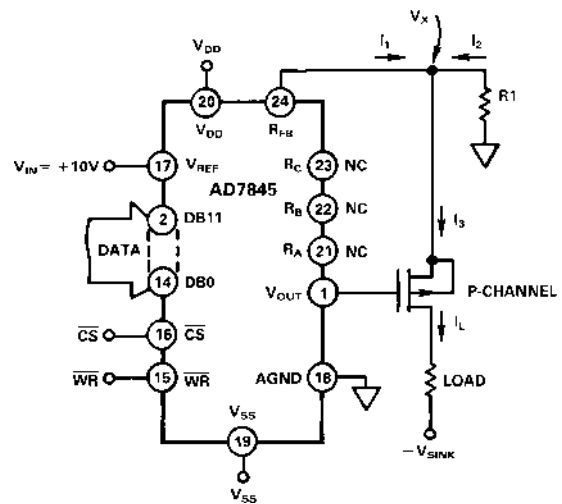


Figure 16. Programmable Current Source

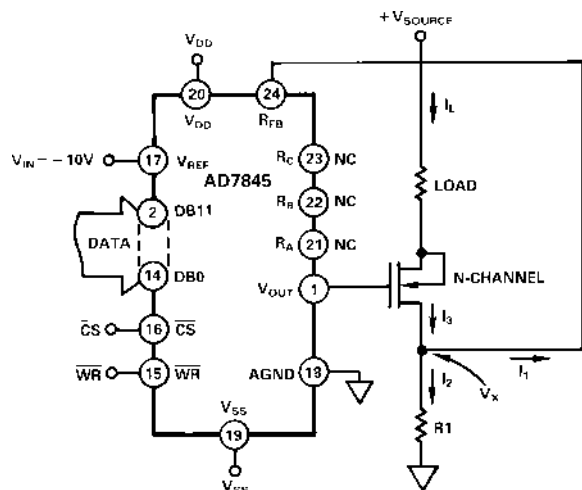


Figure 17. Programmable Current Sink

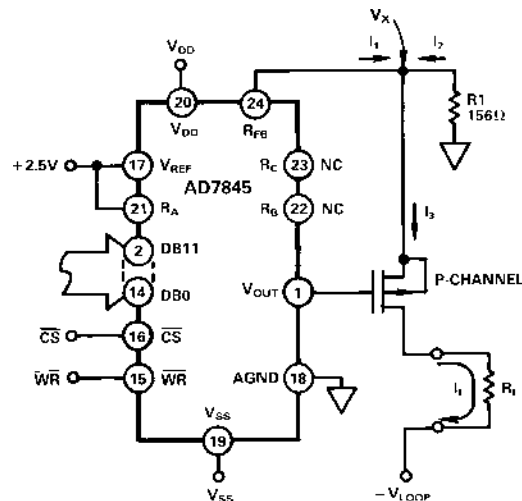


Figure 18. 4–20 mA Current Loop

4–20 mA CURRENT LOOP

The AD7845 provides an excellent way of making a 4–20 mA current loop circuit. This is basically a variation of the circuits in Figures 16 and 17 and is shown in Figure 18. The application resistor R_A (Value 4R) produces the effective 4 mA offset.

$$I_L = I_3 = I_2 + I_1$$

Since $I_2 > I_1$,

$$I_L = -\frac{V_X}{156} = \left(\frac{2.5}{4R} \times R_{FB} + \frac{2.5}{R_{DAC}} \times D \times R_{FB} \right) \times \frac{1}{156}$$

and since $R_{DAC} = R_{FB} = R$

$$I_L = \left(\frac{2.5}{4} + D \times 2.5 \right) \times \frac{1000}{156} \text{ mA}$$

= $[4 + (16 \times D)] \text{ mA}$, where D goes from 0 to 1 with Digital Code

When $D = 0$ (Code of all 0s):

$$I_L = 4 \text{ mA}$$

When $D = 1$ (Code of all 1s):

$$I_L = 20 \text{ mA}$$

The above circuit succeeds in significantly reducing the circuit component count. Both the on-chip output amplifier and the application resistor R_A contribute to this.

APPLICATION HINTS

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7845. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7845 AGND and DGND pins (IN914 or equivalent).

Digital Glitches: When a new digital word is written into the DAC, it results in a change of voltage applied to some of the DAC switch gates. This voltage change is coupled across the switch stray capacitance and appears as an impulse on the current output bus of the DAC. In the AD7845, impulses on this bus are converted to a voltage by R_{FB} and the output amplifier. The output voltage glitch energy is specified as the area of the resulting spike in nV-seconds. It is measured with V_{REF} connected to analog ground and for a zero to full-scale input code transition. Since microprocessor based systems generally have noisy grounds which couple into the power supplies, the AD7845 V_{DD} and V_{SS} terminals should be decoupled to signal ground.

Temperature Coefficients: The gain temperature coefficient of the AD7845 has a maximum value of 5 ppm/°C. This corresponds to worst case gain shift of 2 LSBs over a 100°C temperature range. When trim resistors R_1 and R_2 in Figure 13 are used to adjust full-scale range, the temperature coefficient of R_1 and R_2 must be taken into account. The offset temperature coefficient is 5 ppm of FSR/°C maximum. This corresponds to a worst case offset shift of 2 LSBs over a 100°C temperature range.

The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs," Publication Number E630C-5-3/86.

AD7845

MICROPROCESSOR INTERFACING 16-BIT MICROPROCESSOR SYSTEMS

Figures 19, 20 and 21 show how the AD7845 interfaces to three popular 16-bit microprocessor systems. These are the MC68000, 8086 and the TMS32010. The AD7845 is treated as a memory-mapped peripheral to the processors. In each case, a write instruction loads the AD7845 with the appropriate data. The particular instructions used are as follows:

MC68000: MOVE
8086: MOV
TMS32010: OUT

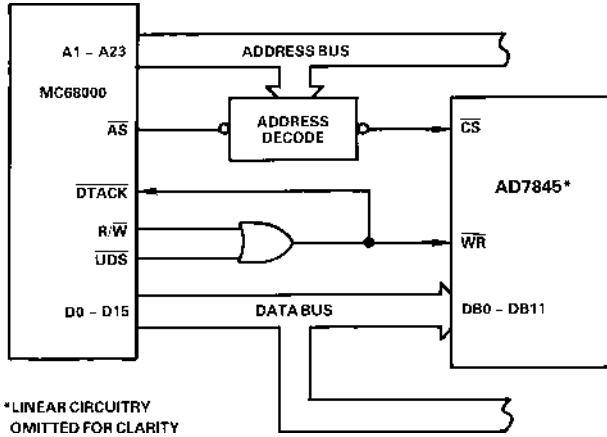


Figure 19. AD7845 to MC68000 Interface

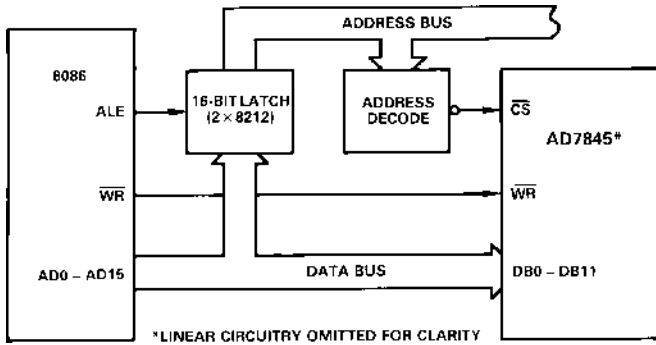


Figure 20. AD7845 to 8086 Interface

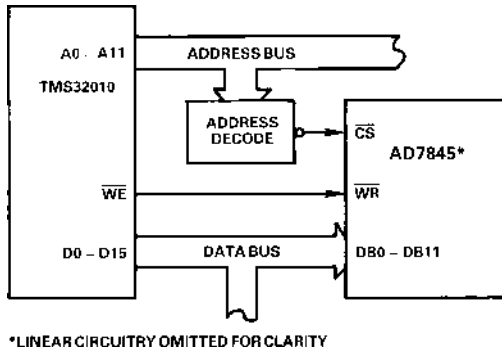


Figure 21. TMS32010

8-BIT MICROPROCESSOR SYSTEMS

Figure 22 shows an interface circuit for the AD7845 to the 8085A 8-bit microprocessor. The software routine to load data to the device is given in Table IV. Note that the transfer of the 12 bits of data requires two write operations. The first of these loads the 4 MSBs into the 7475 latch. The second write operation loads the 8 LSBs plus the 4 MSBs (which are held by the latch) into the DAC.

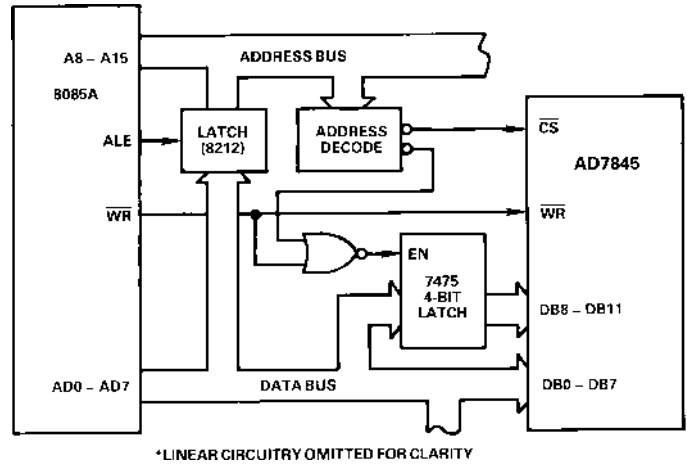
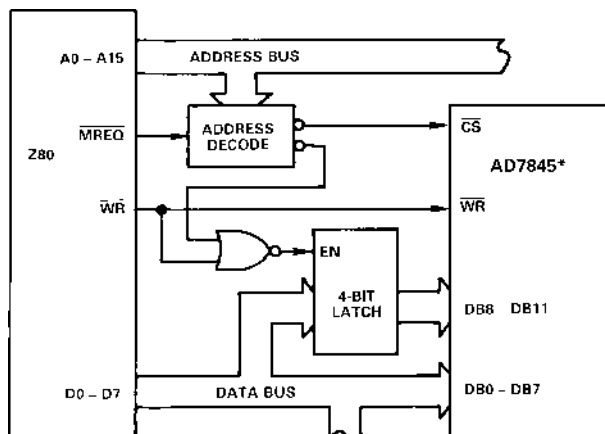


Figure 22. 8085A Interface

Table IV. Subroutine Listing for Figure 22

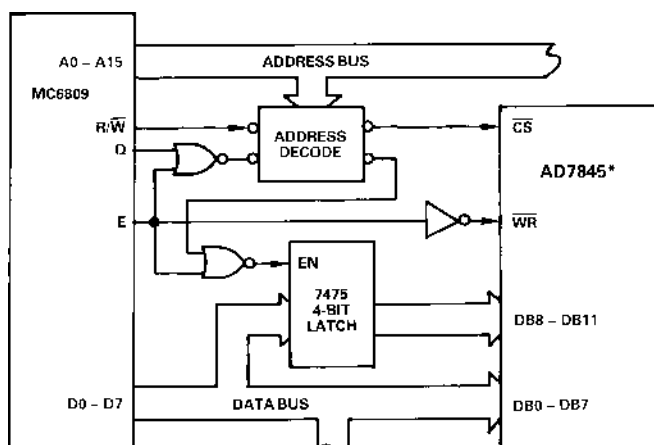
| | | |
|--------------------|-------------|---|
| 2000 LOAD DAC: LXI | H,#3000 | The H,L register pair are loaded with latch address 3000. |
| | MVI A,#"MS" | Load the 4 MSBs of data into accumulator. |
| | MOV M,A | Transfer data from accumulator to latch. |
| | INR L | Increment H,L pair to AD7845 address. |
| | MVI A,#"LS" | Load the 8 LSBs of data into accumulator. |
| | MOV M,A | Transfer data from accumulator to DAC. |
| | RET | End of routine. |

Figure 23 and 24 are the interface circuits for the Z80 and MC6809 microprocessors. Again, these use the same basic format as the 8085A interface.



*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 23. AD7845 to Z80 Interface

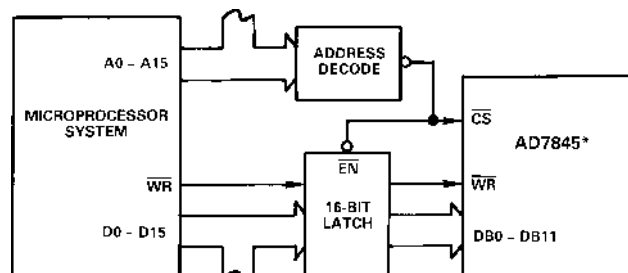


*LINEAR CIRCUITRY OMITTED FOR CLARITY

Figure 24. MC6809 Interface

DIGITAL FEEDTHROUGH

In the preceding interface configurations, most digital inputs to the AD7845 are directly connected to the microprocessor bus. Even when the device is not selected, these inputs will be constantly changing. The high frequency logic activity on the bus can feed through the DAC package capacitance to show up as noise on the analog output. To minimize this digital feedthrough isolate the DAC from the noise source. Figure 25 shows an interface circuit which uses this technique. All data inputs are latched from the bus by the \overline{CS} signal. One may also use other means, such as peripheral interface devices, to reduce the digital feedthrough.

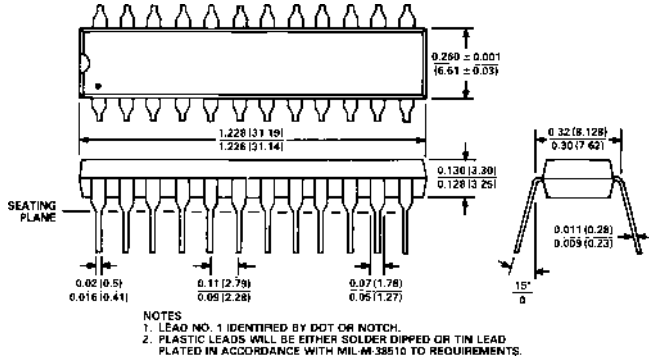


*LINEAR CIRCUITRY OMITTED FOR CLARITY

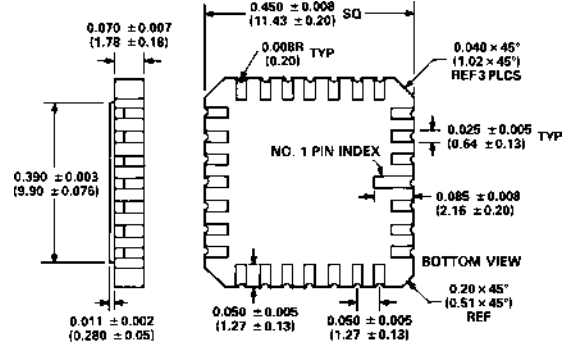
Figure 25. AD7845 Interface Circuit Using Latches to Minimize Digital Feedthrough

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

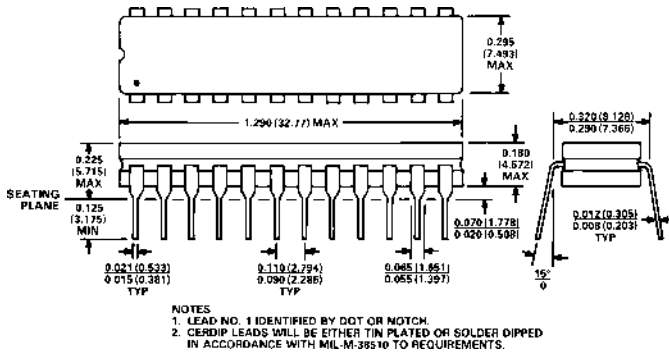
24-Lead Plastic DIP (N-24)



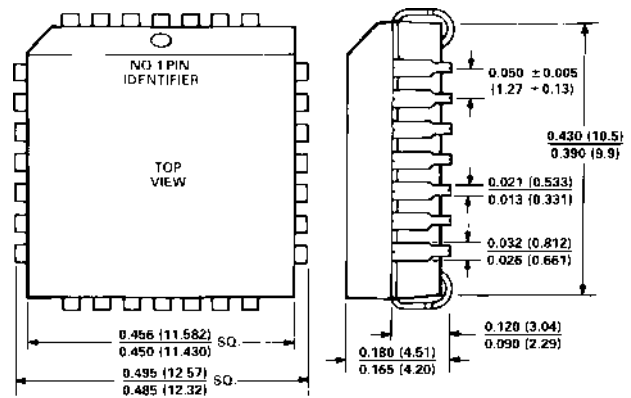
28-Terminal Leadless Ceramic Chip Carrier (E-28A)



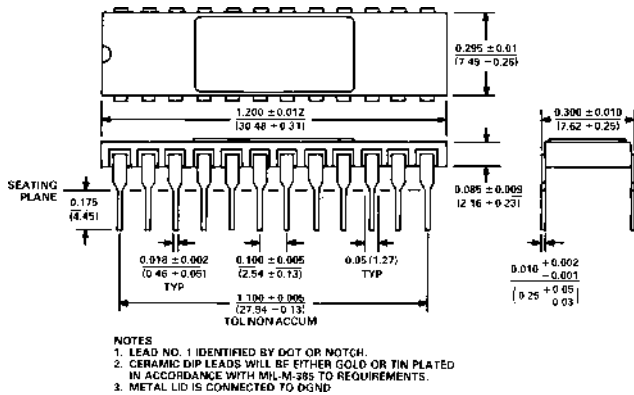
24-Lead Cerdip (Q-24)



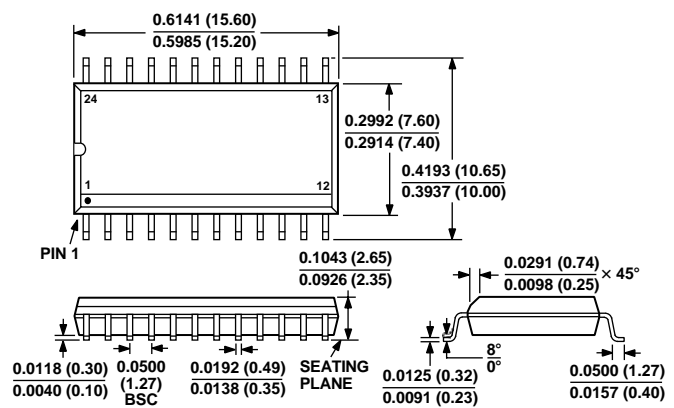
28-Terminal Plastic Leaded Chip Carrier (P-28A)



24-Lead Ceramic DIP (D-24A)



24-Lead SOIC (R-24)



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