IS61C1024AL
IS64C1024AL

128K x 8 HIGH-SPEED CMOS STATIC RAM

MAY 2012

FEATURES

- High-speed access time: 12, 15 ns
- Low active power: 160 mW (typical)
- Low standby power: 1000 µW (typical) CMOS standby
- Output Enable ($\overline{OE}$) and two Chip Enable ($\overline{CE1}$ and CE2) inputs for ease in applications
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 5V (±10%) power supply
- Commercial, industrial, and automotive temperature ranges available
- Lead free available

DESCRIPTION

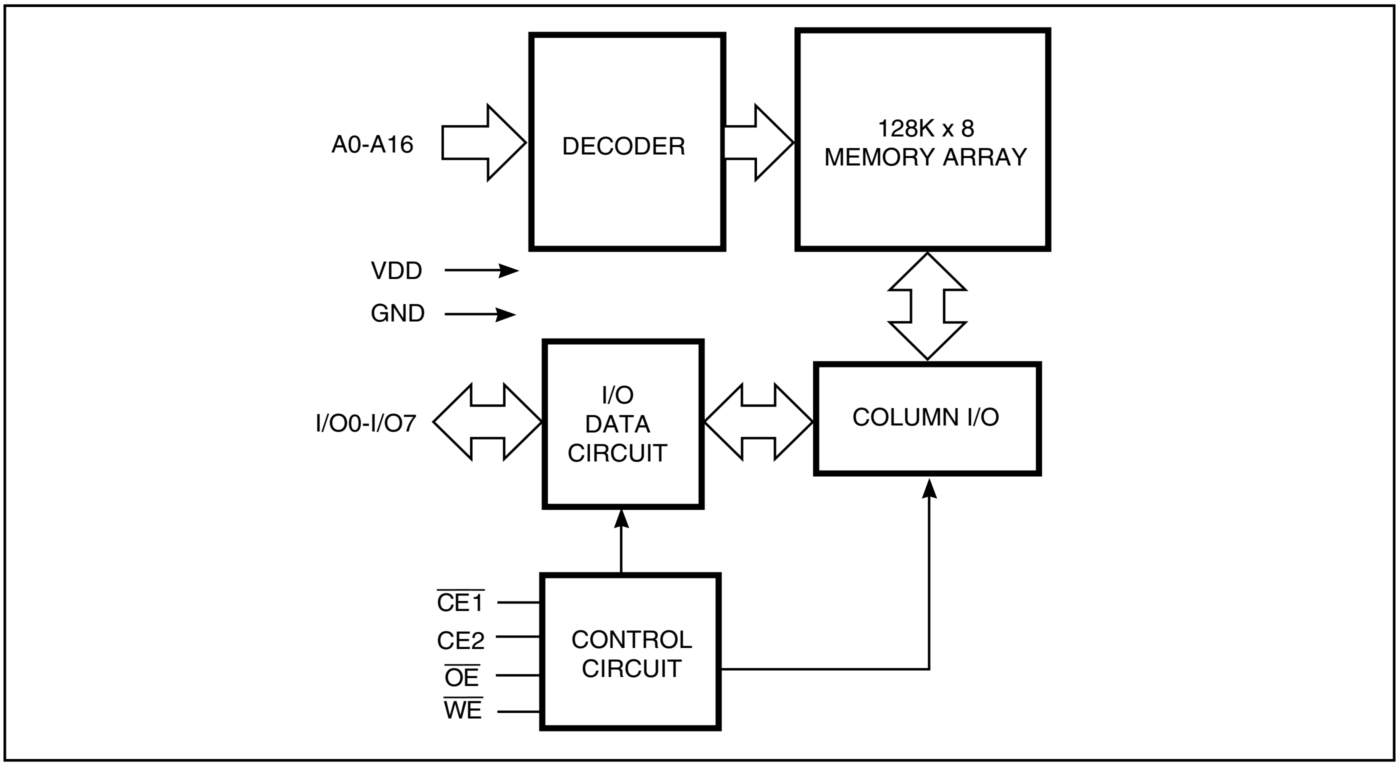
The *ISSI* IS61C1024AL/IS64C1024AL is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAMs. They are fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

When $\overline{CE1}$ is HIGH or CE2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced by using CMOS input levels.

Easy memory expansion is provided by using two Chip Enable inputs, $\overline{CE1}$ and CE2. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory.

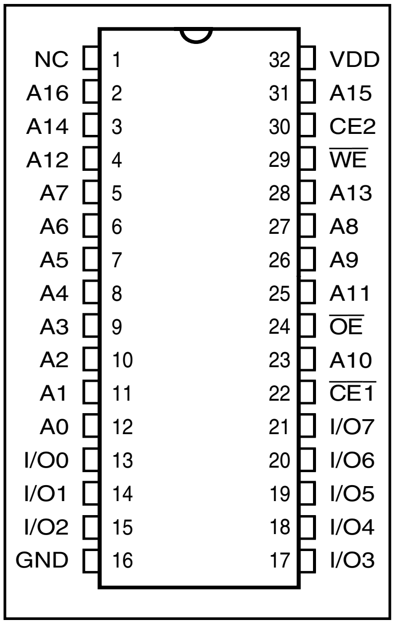
The IS61C1024AL/IS64C1024AL is available in 32-pin 300-mil SOJ, 32-pin 400-mil SOJ, 32-pin TSOP (Type I, 8x20), and 32-pin sTSOP (Type I, 8 x 13.4) packages.

FUNCTIONAL BLOCK DIAGRAM



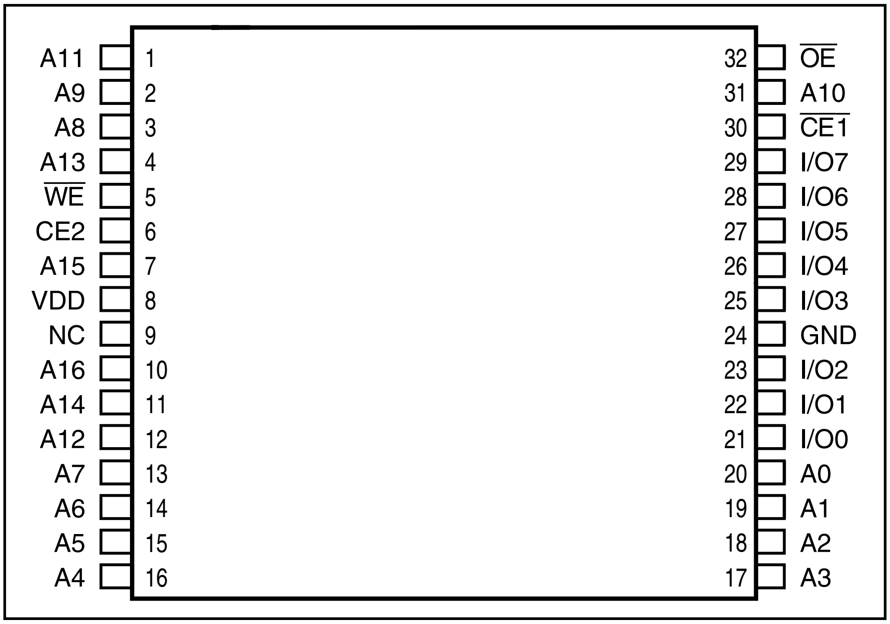
PIN CONFIGURATION

32-Pin SOJ



PIN CONFIGURATION

32-Pin TSOP (Type 1) (T) and sTSOP (Type 1) (H)



PIN DESCRIPTIONS

A0-A16	Address Inputs
$\overline{CE1}$	Chip Enable 1 Input
CE2	Chip Enable 2 Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O0-I/O7	Input/Output
V_{DD}	Power
GND	Ground

OPERATING RANGE (IS61C1024AL)

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

OPERATING RANGE (IS64C1024AL)

Range	Ambient Temperature	V_{DD}
Automotive	-40°C to +125°C	5V ± 10%

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O Operation	V_{DD} Current
Not Selected	X	H	X	X	High-Z	I_{SB1}, I_{SB2}
(Power-down)	X	X	L	X	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	High-Z	I_{CC1}, I_{CC2}
Read	H	L	H	L	D_{OUT}	I_{CC1}, I_{CC2}
Write	L	L	H	X	D_{IN}	I_{CC1}, I_{CC2}

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.5	W
I_{OUT}	DC Output Current (LOW)	20	mA

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	pF

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: $T_A = 25°C$, f = 1 MHz, $V_{DD} = 5.0V$.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{DD} = Min., I_{OH} = –4.0 mA		2.4	—	V
V_{OL}	Output LOW Voltage	V_{DD} = Min., I_{OL} = 8.0 mA		—	0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{DD} + 0.5	V
V_{IL}	Input LOW Voltage[1]			–0.3	0.8	V
I_{LI}	Input Leakage	$GND \le V_{IN} \le V_{DD}$	Com. Ind. Auto.	–1 –2 –5	1 2 5	µA
I_{LO}	Output Leakage	$GND \le V_{OUT} \le V_{DD}$ Outputs Disabled	Com. Ind. Auto.	–1 –2 –5	1 2 5	µA

Note:

1. V_{IL} = –3.0V for pulse width less than 10 ns.

IS61C1024AL/IS64C1024AL POWER SUPPLY CHARACTERISTICS(1) (Over Operating Range)

				-12 ns		-15 ns		
Symbol	**Parameter**	**Test Conditions**		**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
I_{CC1}	V_{DD} Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE1} = V_{IL}$	Com.	—	35			mA
		$I_{OUT} = 0$ mA, f = 0	Ind.	—	40			
			Auto.			—	45	
I_{CC2}	V_{DD} Dynamic Operating Supply Current	$V_{DD} = V_{DD\ MAX.}$, $\overline{CE1} = V_{IL}$	Com.	—	45			mA
		$I_{OUT} = 0$ mA, $f = f_{MAX}$	Ind.	—	50			
			Auto.			—	55	
			typ.(2)	—	32			
I_{SB1}	TTL Standby Current (TTL Inputs)	$V_{DD} = V_{DD\ MAX.}$,	Com.	—	1			mA
		$V_{IN} = V_{IH}$ or V_{IL}	Ind.	—	1.5			
		$\overline{CE1} \geq V_{IH}$, f = 0 or	Auto.			—	2	
		$CE2 \leq V_{IL}$, f = 0						
I_{SB2}	CMOS Standby Current (CMOS Inputs)	$V_{DD} = V_{DD\ MAX.}$,	Com.	—	400			µA
		$\overline{CE1} \geq V_{DD} - 0.2V$,	Ind.	—	450			
		$CE2 \leq 0.2V$	Auto.			—	500	
		$V_{IN} \geq V_{DD} - 0.2V$, or	typ.(2)	—	200			
		$V_{IN} \leq 0.2V$, f = 0						

Note:

1. At $f = f_{MAX}$, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical Values are measured at $V_{DD} = 5V$, $T_A = 25^{o}C$ and not 100% tested.

READ CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

		-12		-15		
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
t_{RC}	Read Cycle Time	12	—	15	—	ns
t_{AA}	Address Access Time	—	12	—	15	ns
t_{OHA}	Output Hold Time	3	—	3	—	ns
t_{ACE1}	$\overline{CE1}$ Access Time	—	12	—	15	ns
t_{ACE2}	CE2 Access Time	—	12	—	15	ns
t_{DOE}	$\overline{OE}$ Access Time	—	6	—	7	ns
t_{LZOE}(2)	$\overline{OE}$ to Low-Z Output	0	—	0	—	ns
t_{HZOE}(2)	$\overline{OE}$ to High-Z Output	0	6	0	6	ns
t_{LZCE1}(2)	$\overline{CE1}$ to Low-Z Output	2	—	2	—	ns
t_{LZCE2}(2)	CE2 to Low-Z Output	2	—	2	—	ns
t_{HZCE}(2)	$\overline{CE1}$ or CE2 to High-Z Output	0	7	0	8	ns
t_{PU}(3)	$\overline{CE1}$ or CE2 to Power-Up	0	—	0	—	ns
t_{PD}(3)	$\overline{CE1}$ or CE2 to Power-Down	—	12	—	12	ns

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.
3. Not 100% tested.

AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3 ns
Input and Output Timing and Reference Level	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

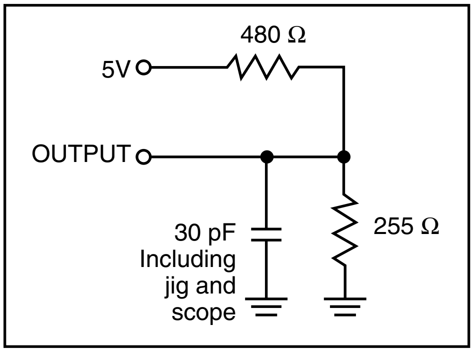


Figure 1

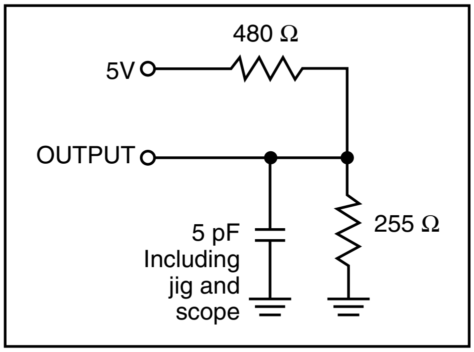
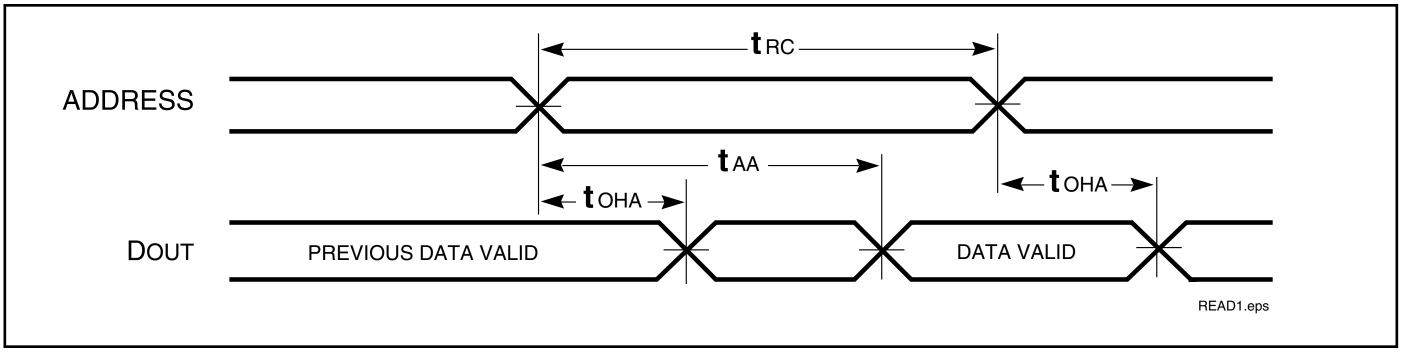


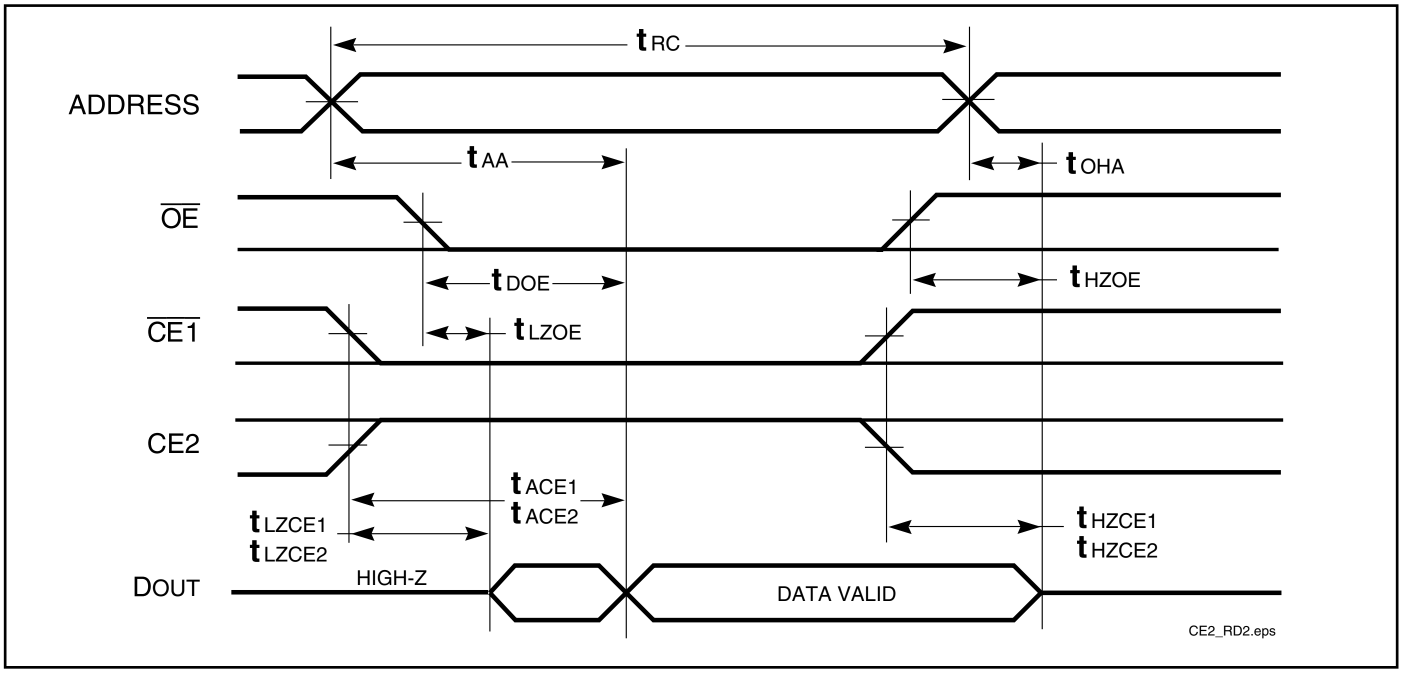
Figure 2

AC WAVEFORMS

READ CYCLE NO. 1[1,2]



READ CYCLE NO. 2[1,3]



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}.
3. Address is valid prior to or coincident with $\overline{CE1}$ LOW and CE2 HIGH transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range, Standard and Low Power)

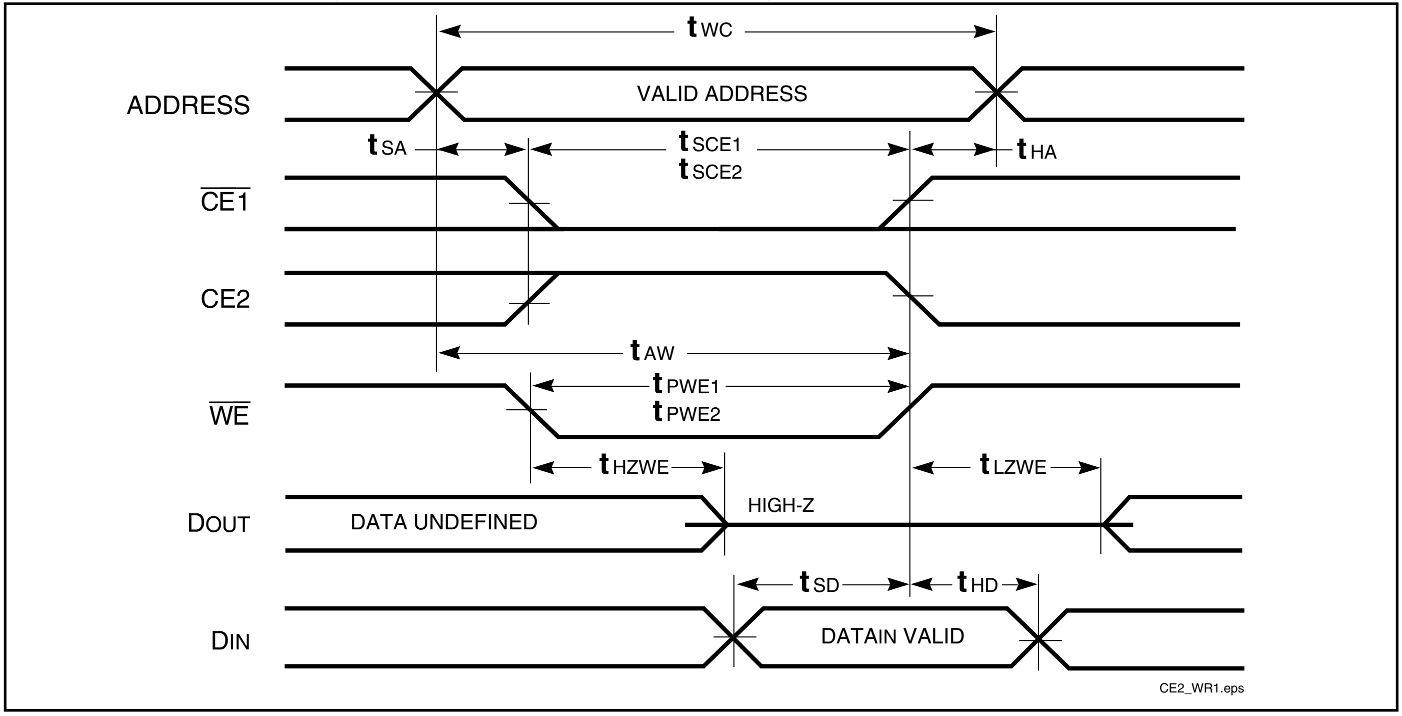
Symbol	Parameter	-12 ns Min.	-12 ns Max.	-15 ns Min.	-15 ns Max.	Unit
t_{WC}	Write Cycle Time	12	—	15	—	ns
t_{SCE1}	$\overline{CE1}$ to Write End	10	—	12	—	ns
t_{SCE2}	CE2 to Write End	10	—	12	—	ns
t_{AW}	Address Setup Time to Write End	10	—	12	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWE}(3)	$\overline{WE}$ Pulse Width	10	—	12	—	ns
t_{SD}	Data Setup to Write End	7	—	10	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}(4)	$\overline{WE}$ LOW to High-Z Output	—	7	—	7	ns
t_{LZWE}(4)	$\overline{WE}$ HIGH to Low-Z Output	2	—	2	—	ns

Notes:

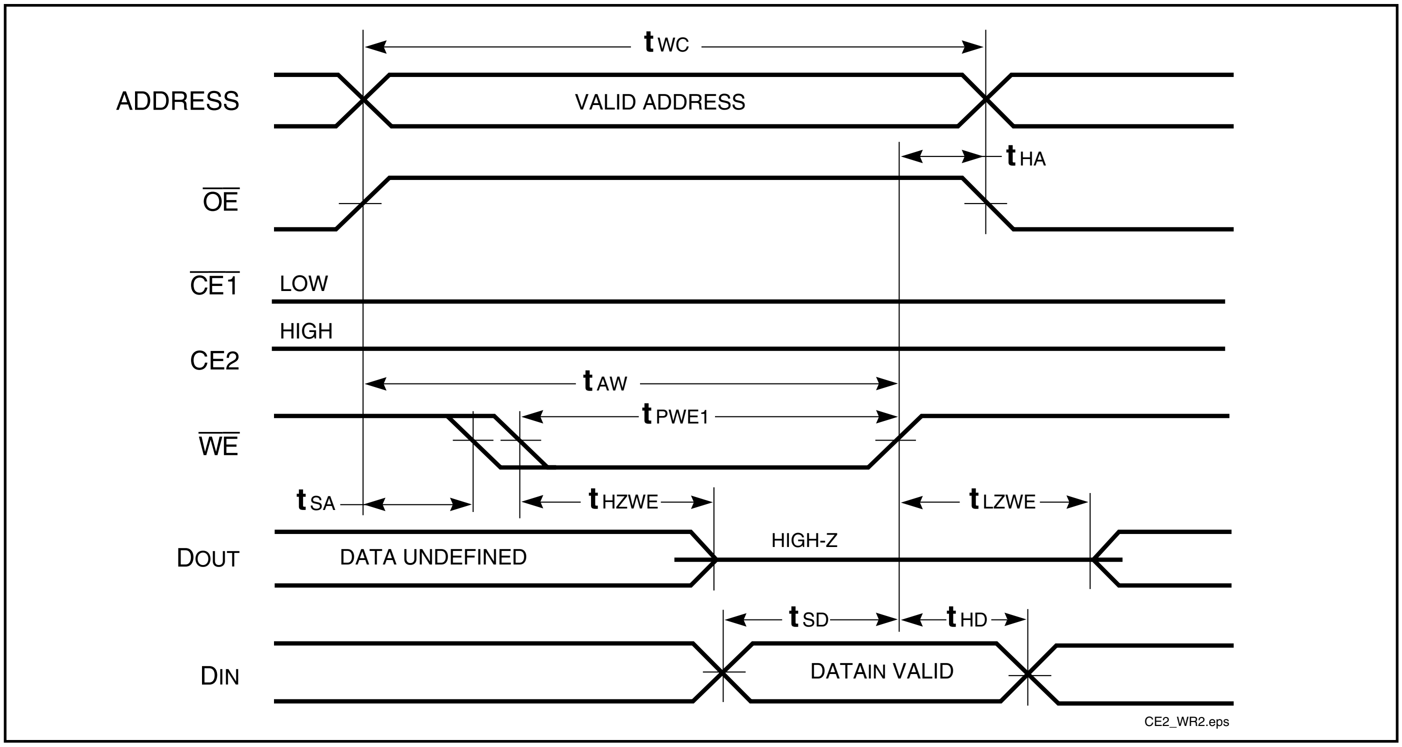
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CE1}$ LOW, CE2 HIGH and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
3. Tested with $\overline{OE}$ HIGH.
4. Tested with the load in Figure 2. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC WAVEFORMS

WRITE CYCLE NO. 1 ($\overline{\text{CE1}}$ Controlled, $\overline{\text{OE}}$ is HIGH or LOW) (1)



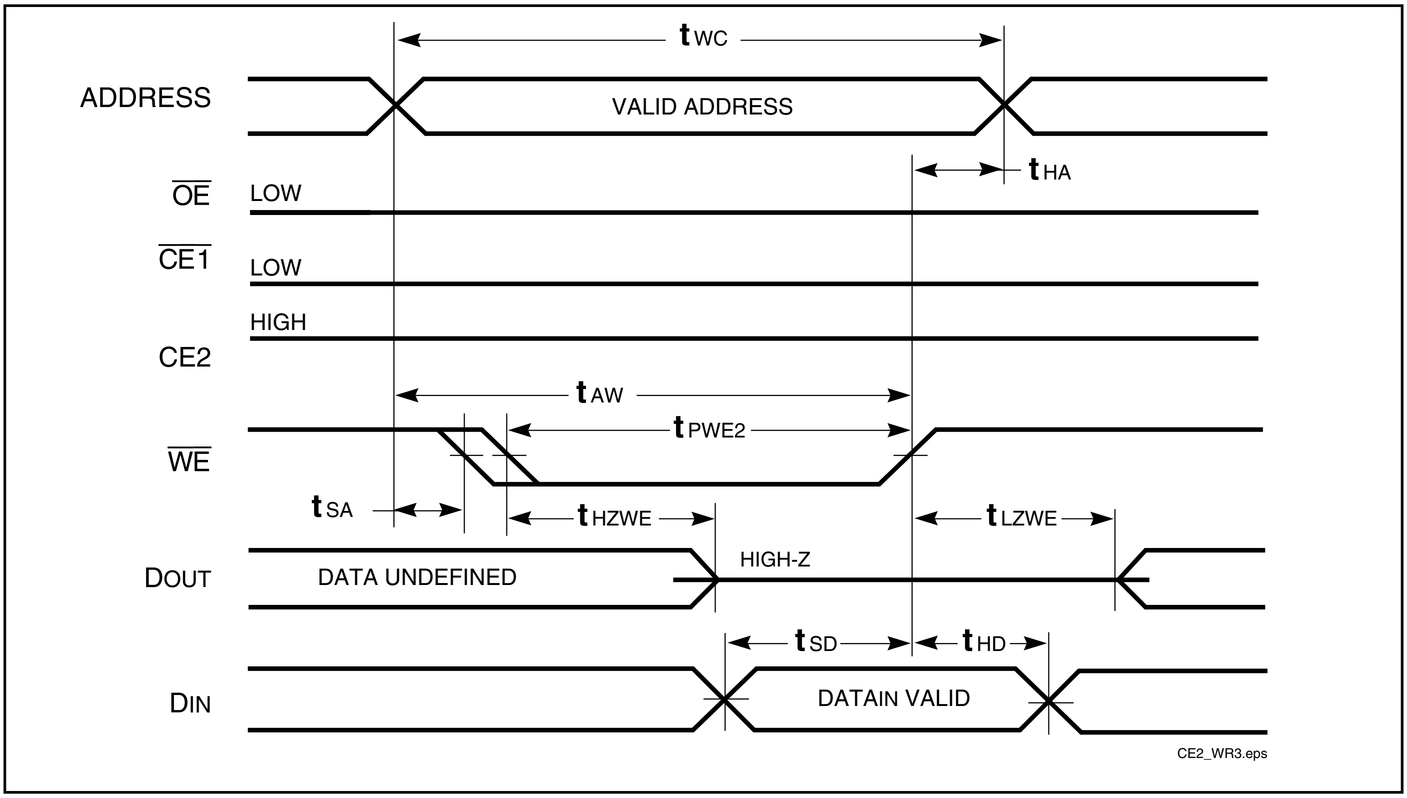
WRITE CYCLE NO. 2 ($\overline{\text{OE}}$ is HIGH During Write Cycle) (1,2)



Notes:

1. The internal write time is defined by the overlap of $\overline{\text{CE1}}$ LOW, CE2 HIGH and $\overline{\text{WE}}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if $\overline{\text{OE}}$ = V_{IH}.

WRITE CYCLE NO. 3 ($\overline{OE}$ is LOW During Write Cycle) (1)



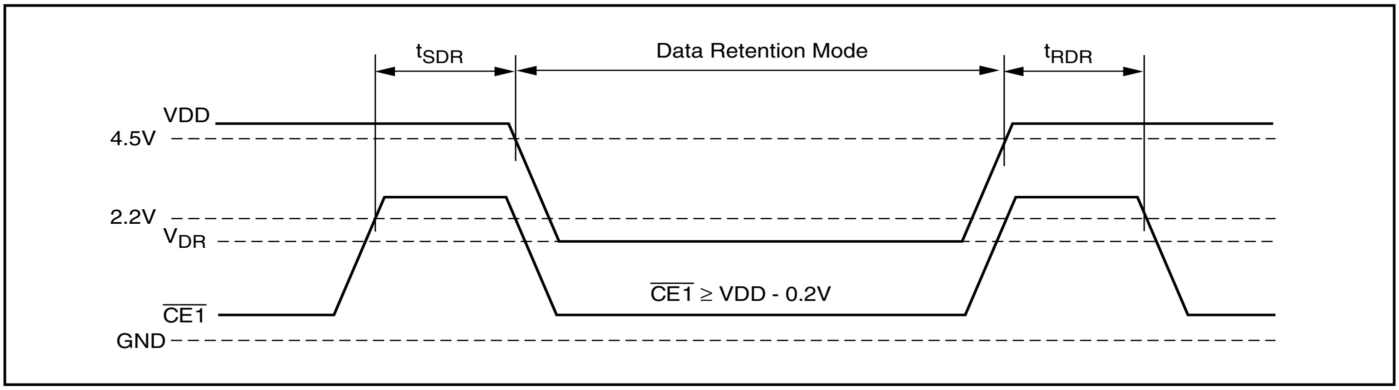
DATA RETENTION SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform		2.0		5.5	V
I_{DR}	Data Retention Current	$V_{DD} = 2.0V$, $\overline{CE1} \geq V_{DD} - 0.2V$	Com.	—	200	400	μA
		or $CE2 \leq 0.2V$	Ind.	—	—	450	
		$V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq V_{SS} + 0.2V$	Auto.	—	—	500	
t_{SDR}	Data Retention Setup Time	See Data Retention Waveform		0		—	ns
t_{RDR}	Recovery Time	See Data Retention Waveform		t_{RC}		—	ns

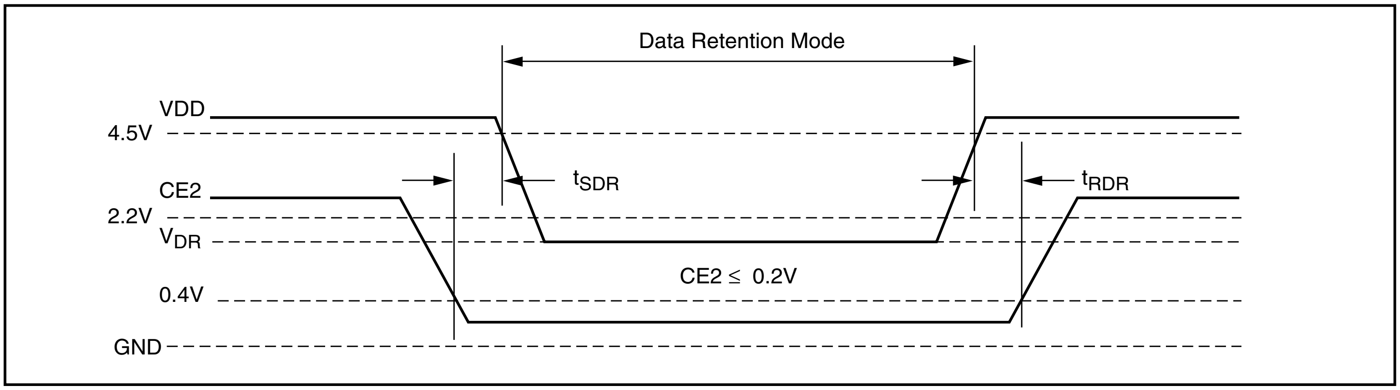
Note:

1. Typical Values are measured at $V_{DD} = 5V$, $T_A = 25^{\circ}C$ and not 100% tested.

DATA RETENTION WAVEFORM ($\overline{CE1}$ Controlled)



DATA RETENTION WAVEFORM (CE2 Controlled)



ORDERING INFORMATION: IS61C1024AL
Commercial Range: 0°C to +70°C

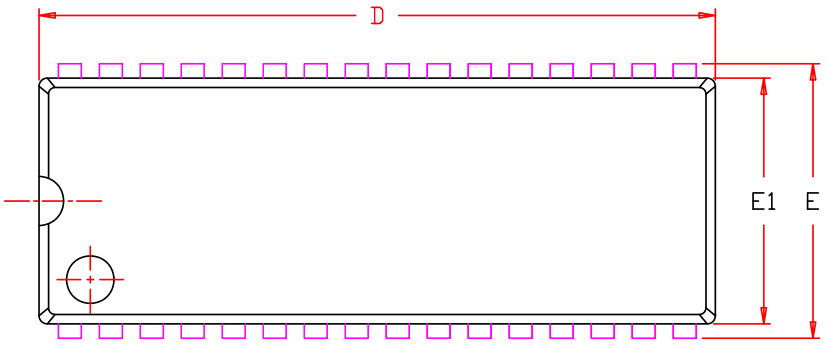
Speed (ns)	Order Part No.	Package
12	IS61C1024AL-12T	TSOP (Type I)

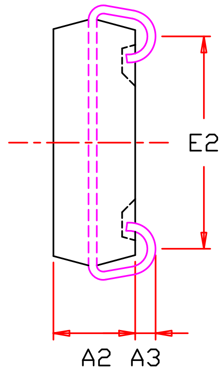
ORDERING INFORMATION: IS61C1024AL
Industrial Range: –40°C to +85°C

Speed (ns)	Order Part No.	Package
12	IS61C1024AL-12JLI	300-mil Plastic SOJ, Lead-free
	IS61C1024AL-12KI	400-mil Plastic SOJ
	IS61C1024AL-12KLI	400-mil Plastic SOJ, Lead-free
	IS61C1024AL-12HI	sTSOP (Type I)
	IS61C1024AL-12HLI	sTSOP (Type I), Lead-free
	IS61C1024AL-12TI	TSOP (Type I)
	IS61C1024AL-12TLI	TSOP (Type I), Lead-free

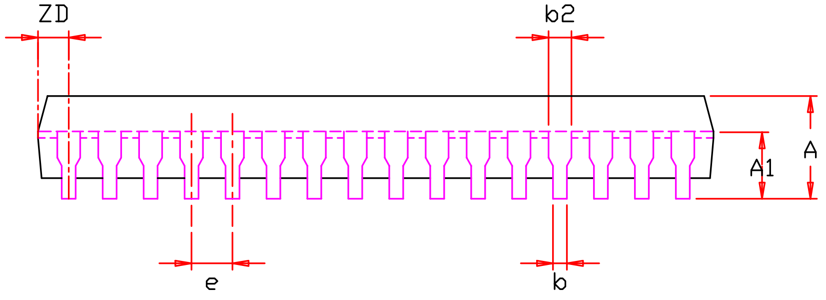
ORDERING INFORMATION: IS64C1024AL
Automotive Range: –40°C to +125°C

Speed (ns)	Order Part No.	Package
15	IS64C1024AL-15KA3	400-mil Plastic SOJ
	IS64C1024AL-15TA3	TSOP (Type I)





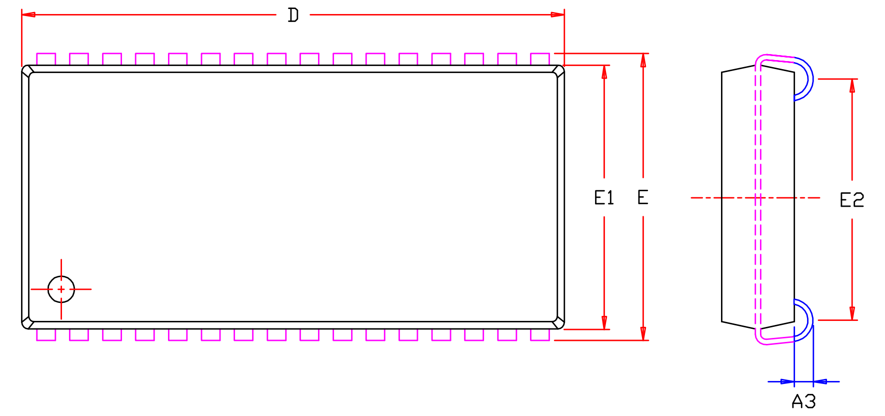
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.05		3.76	0.120		0.148
A1	2.08		2.41	0.082		0.095
A2	2.41	2.54	2.67	0.095	0.100	0.105
A3	0.64		1.09	0.025		0.043
b	0.41		0.51	0.016		0.020
b2	0.66		0.81	0.026		0.032
D	20.82		21.09	0.820		0.830
E	8.38	8.51	8.64	0.330	0.335	0.340
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.48		6.99	0.255		0.275
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF.			0.037 REF.		

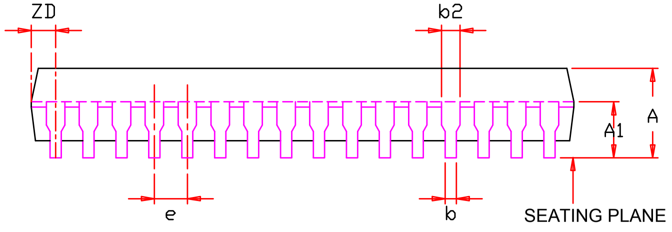


NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	32L 300mil SOJ Package Outline	REV.	C	DATE	08/14/2009



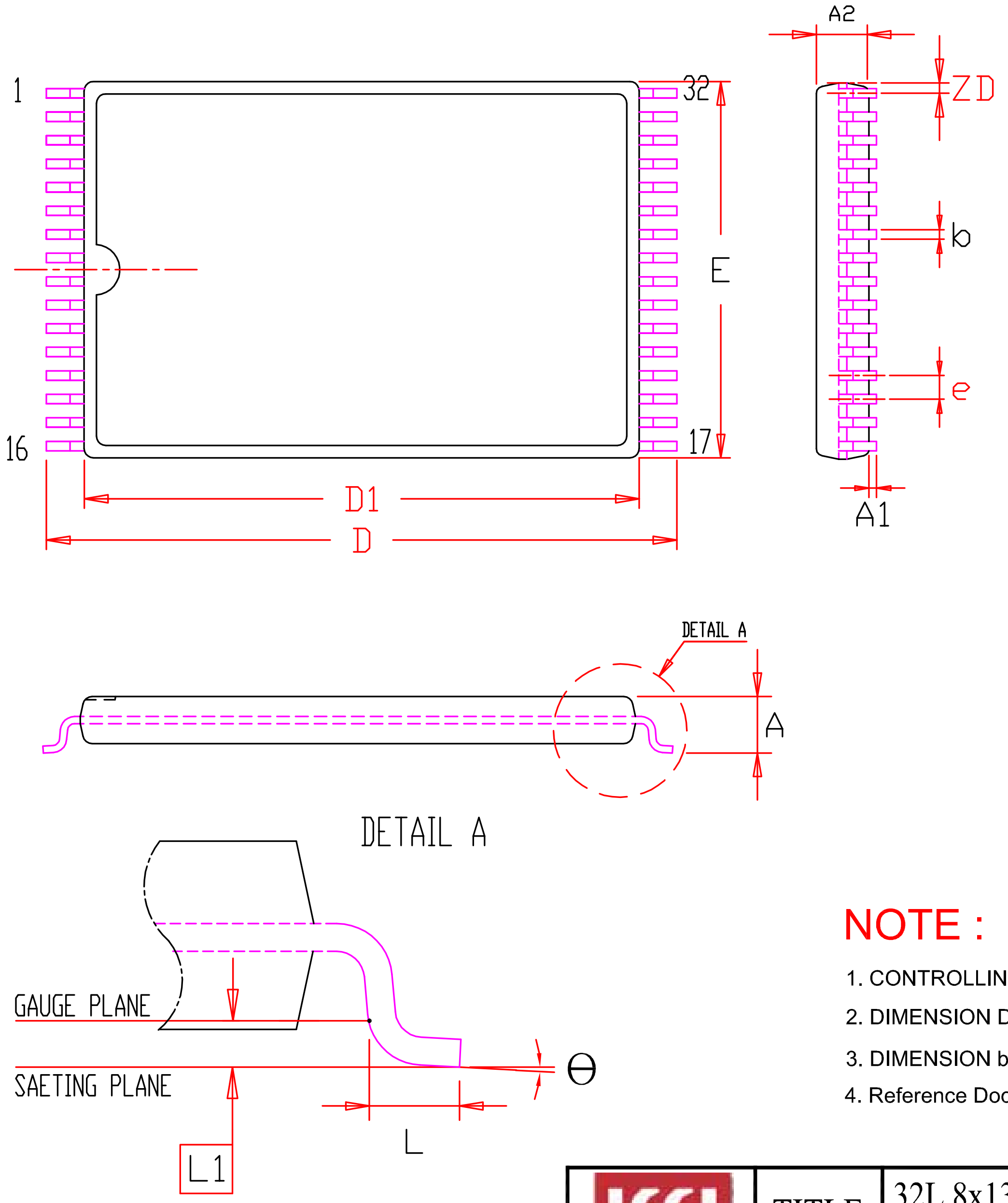


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	—	3.76	0.128	—	0.148
A1	2.08	—	—	0.082	—	—
A3	0.635	—	—	0.025	—	—
b	0.38	—	0.51	0.015	—	0.020
b2	0.66	0.71	0.81	0.026	0.028	0.032
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.16	10.29	0.395	0.400	0.405
E2	9.40 BSC			0.370 BSC		
e	1.27 BSC.			0.050 BSC.		
ZD	0.95 REF			0.037 REF		

NOTE :

1. Controlling dimension : mm
2. Dimension D and E1 do not include mold protrusion .
3. Dimension b2 does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.
5. Reference document : JEDEC SPEC MS-027.

ISSI	TITLE	32L 400mil SOJ Package Outline	REV.	E	DATE	12/19/2007

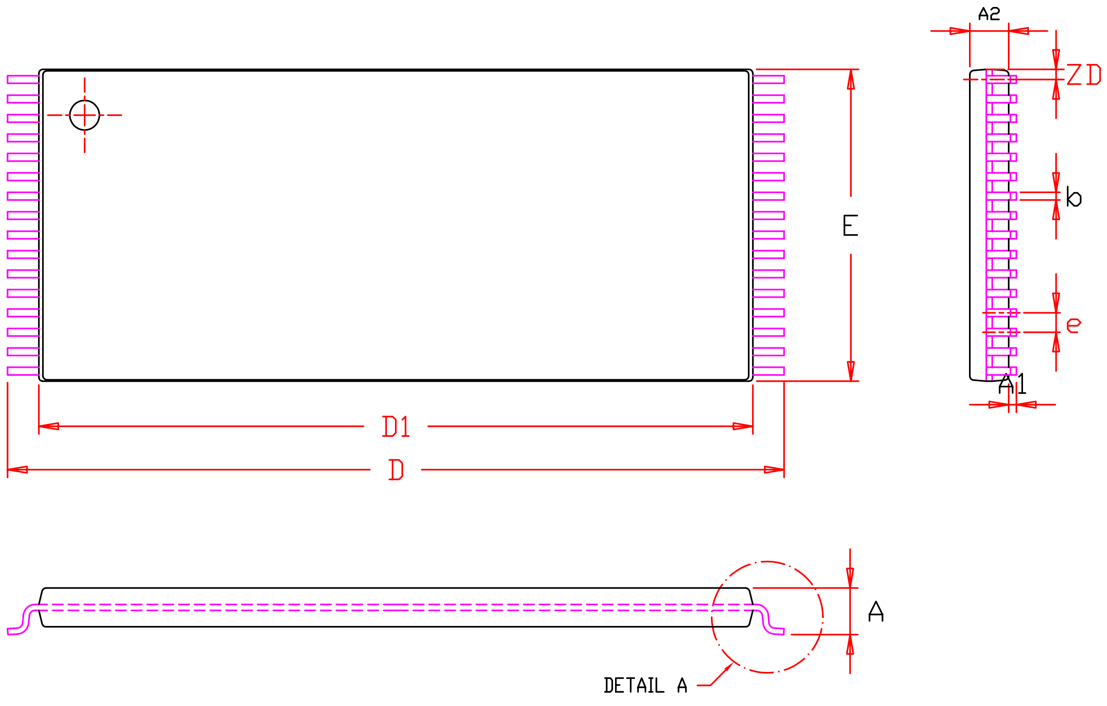


SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.95		1.25	0.037		0.049
A1	0.05		0.15	0.002		0.008
A2	0.90		1.05	0.035		0.041
b	0.16		0.27	0.006		0.011
D	13.10	13.40	13.70	0.516	0.528	0.539
D1	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	0.50 BSC.			0.020 BSC.		
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.25 BSC.			0.010 BSC.		
ZD	0.25 REF.			0.010 REF.		
Θ	0	3°	5°	0	3°	5°

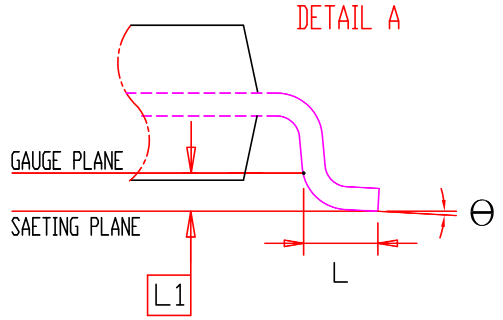
NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D1 AND E DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
4. Reference Document : JEDEC MO-183

TITLE	32L 8x13.4mm TSOP-1 Package Outline	REV.	E	DATE	04/24/2009



SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A	1.00		1.20
A1	0.05		0.20
A2	0.95	1.00	1.05
b	0.17		0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	7.80	8.00	8.20
e	0.50 BSC.		
L	0.40		0.70
L1	0.25 BSC.		
ZD	0.25 REF.		
Θ	0	5°	8°



NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

ISSI®	TITLE	32L 8x20mm TSOP-1 Package Outline	REV.	E	DATE	06/08/2006

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.