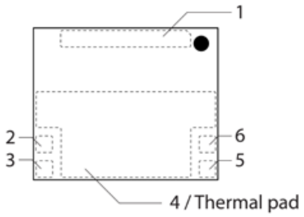
GS66516B
Bottom-side cooled 650 V E-mode GaN transistor
Preliminary Datasheet

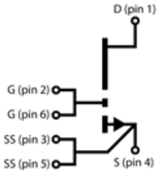
Features

- 650 V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)} = 25\ m\Omega$
- $I_{DS(max)} = 60\ A$
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 / +10 V)
- Very high switching frequency (> 10 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 11 x 9 mm^2 PCB footprint
- Source Sense (SS) pads for optimized gate drive
- Dual gate and source sense pads for optimal board layout
- RoHS 6 compliant

Package Outline



Circuit Symbol



Applications

- High efficiency power conversion
- High density power conversion
- AC-DC Converters
- Bridgeless Totem Pole PFC
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Single and 3Φ inverter legs
- Solar and Wind Power
- Fast Battery Charging
- DC-DC converters
- On Board Battery Chargers
- Traction Drive

Description

The GS66516B is an enhancement mode gallium nitride (GaN) on silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The GS66516B is a bottom-side cooled transistor that offers very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	**Symbol**	**Value**	**Unit**
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	650	V
Transient Drain-to-Source Voltage (note 1)	$V_{DS(transient)}$	750	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C) (note 2)	I_{DS}	60	A
Continuous Drain Current (T_{case}=100 °C) (note 2)	I_{DS}	47	A

(1) Pulse $\leq$ 1 µs.

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	**Symbol**	**Value**	**Units**
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	0.27	°C /W
Thermal Resistance (junction-to-top)	$R_{\Theta JT}$	5.5	°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$	23	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	**Package type**	**Packing method**	**Qty**	**Reel Diameter**	**Reel Width**
GS66516B-TR	GaN*PX*® Bottom-Side Cooled	Tape-and-Reel	2000	13” (330mm)	24mm
GS66516B-MR	GaN*PX*® Bottom-Side Cooled	Mini-Reel	250	7” (180mm)	24mm

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}	650			V	V_{GS} = 0 V, I_{DSS} = 100 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		25	32	mΩ	V_{GS} = 6 V, T_J = 25 °C I_{DS} = 18 A
Drain-to-Source On Resistance	$R_{DS(on)}$		65		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 18 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS}, I_{DS} = 14 mA
Gate-to-Source Current	I_{GS}		320		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3.0		V	V_{DS} = 400 V, I_{DS} = 60 A
Drain-to-Source Leakage Current	I_{DSS}		4	100	µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 25 °C
Drain-to-Source Leakage Current	I_{DSS}		800		µA	V_{DS} = 650 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		0.34		Ω	f = 25MHz, open drain
Input Capacitance	C_{ISS}		520		pF	V_{DS} = 400 V, V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		130		pF	
Reverse Transfer Capacitance	C_{RSS}		4		pF	
Effective Output Capacitance Energy Related (note 4)	$C_{O(ER)}$		177		pF	V_{GS} = 0 V, V_{DS} = 0 to 400 V
Effective Output Capacitance Time Related (note 5)	$C_{O(TR)}$		284		pF	
Total Gate Charge	Q_G		12.1		nC	V_{GS} = 0 to 6 V, V_{DS} = 400 V
Gate-to-Source Charge	Q_{GS}		4.4		nC	
Gate-to-Drain Charge	Q_{GD}		3.4		nC	
Output Charge	Q_{OSS}		113		nC	V_{GS} = 0 V, V_{DS} = 400 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

Electrical Characteristics cont'd (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		4.6		ns	V_{DD} = 400 V V_{GS} = 0 - 6 V I_D = 16 A, $R_{G(ext)}$ = 5 Ω T_J = 25 °C (note 6)
Rise Time	t_R		12.4		ns	
Turn-Off Delay	$t_{D(off)}$		14.9		ns	
Fall Time	t_F		22		ns	
Output Capacitance Stored Energy	E_{OSS}		14.1		µJ	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz
Switching Energy during turn-on	E_{on}		134.1		µJ	V_{DS} = 400 V, I_{DS} = 20 A V_{GS} = 0-6 V, $R_{G(on)}$ = 10 Ω $R_{G(off)}$ = 1 Ω L = 120 µH L_P = 10 nH (notes 7, 8)
Switching Energy during turn-off	E_{off}		14.7		µJ	

(6) See Figure 12 for timing test circuit diagram and definition waveforms.

(7) L_P is the switching circuit parasitic inductance.

(8) See Figure 13 for switching test circuit.

Electrical Performance Graphs

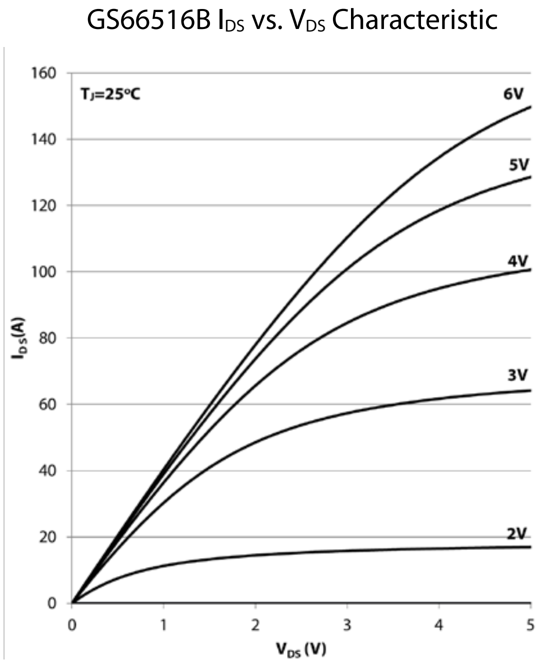


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 ^{0}C

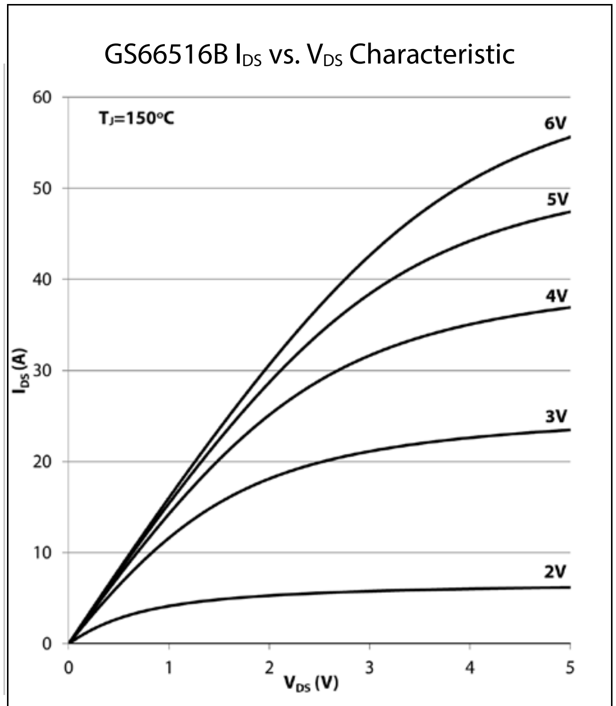


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 ^{0}C

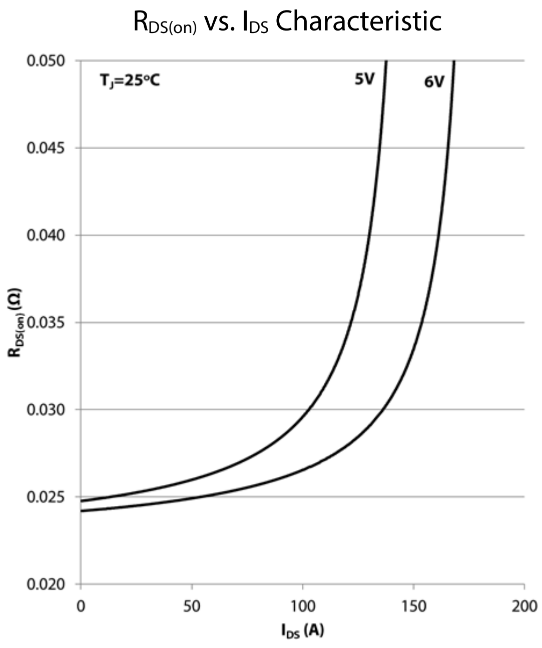


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 ^{0}C

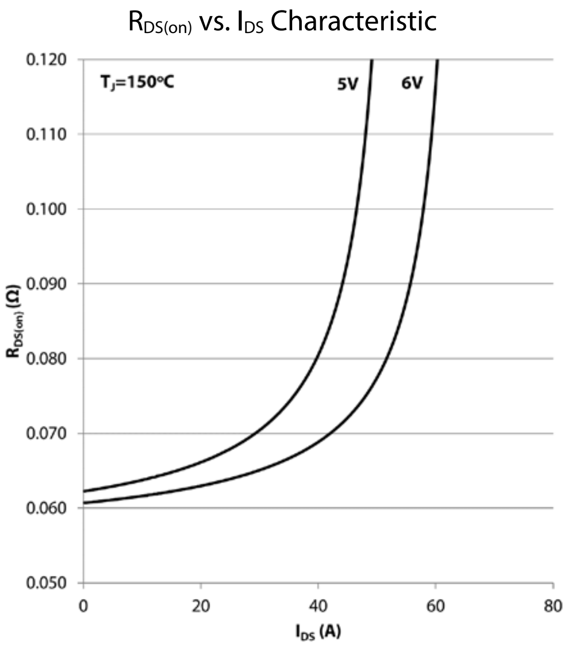


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150^{0}C

Electrical Performance Graphs

GS66516B I_{DS} vs. V_{DS}, T_J dependence

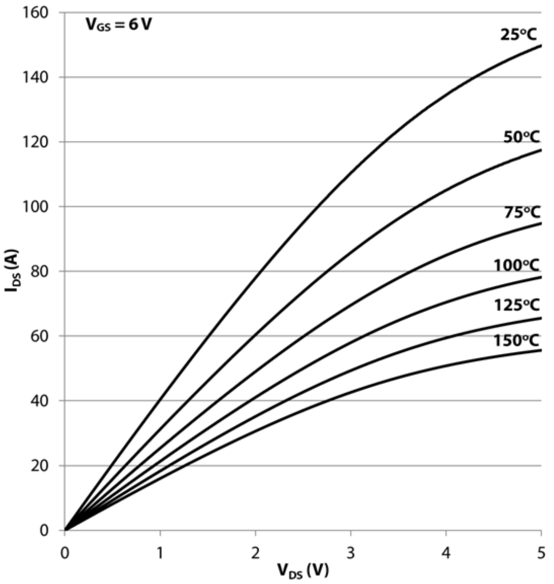


Figure 5: Typical I_{DS} vs. V_{DS} @ $V_{GS} = 6$ V

GS66516B Gate Charge, Q_G Characteristic

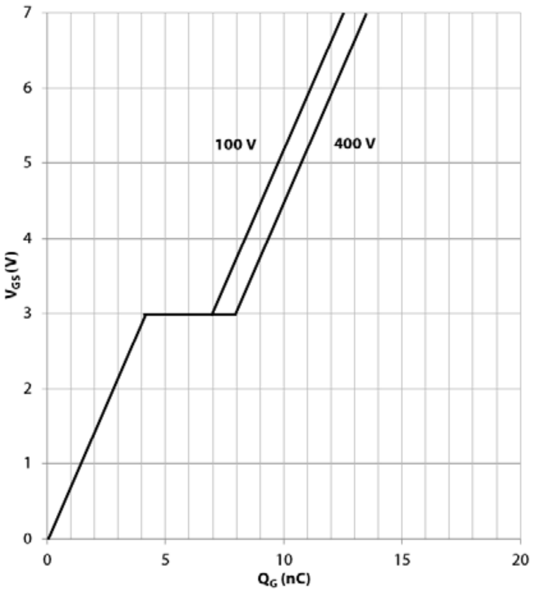


Figure 6: Typical V_{GS} vs. Q_G @ $V_{DS} = 100, 400$ V

GS66516B Capacitance Characteristics

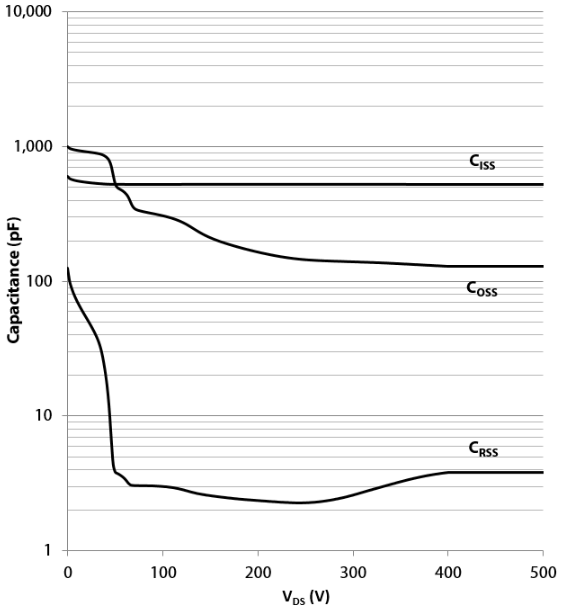


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

GS66516B Stored Energy Characteristic

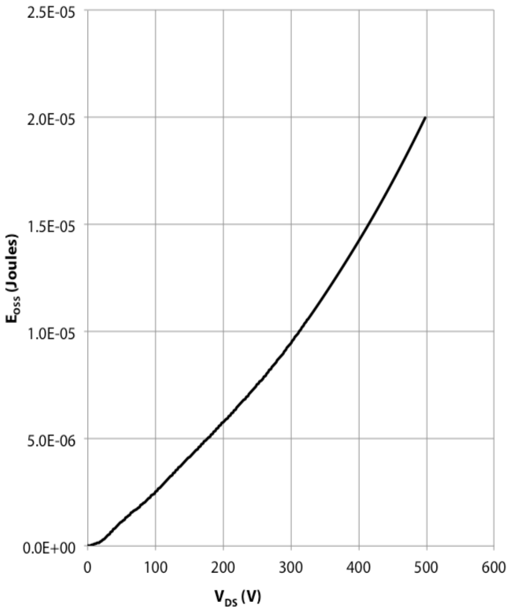


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

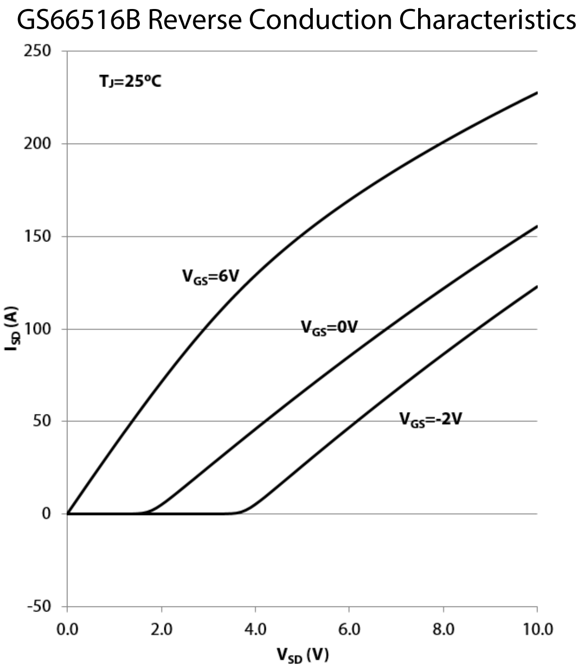

GS66516B Reverse Conduction Characteristics

Figure 9: Typical I_{SD} vs. V_{SD}

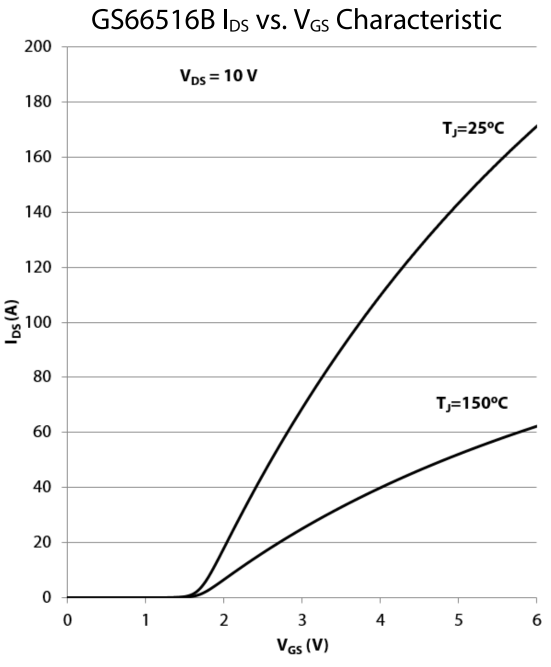

GS66516B I_{DS} vs. V_{GS} Characteristic

Figure 10: Typical I_{DS} vs. V_{GS}

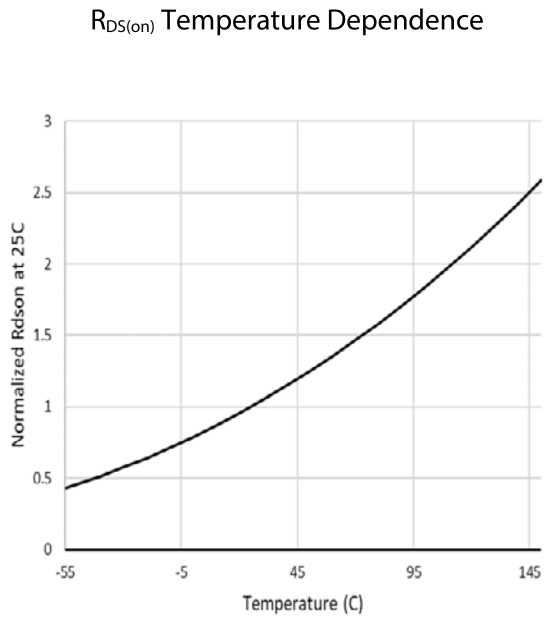

$R_{DS(on)}$ Temperature Dependence

Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

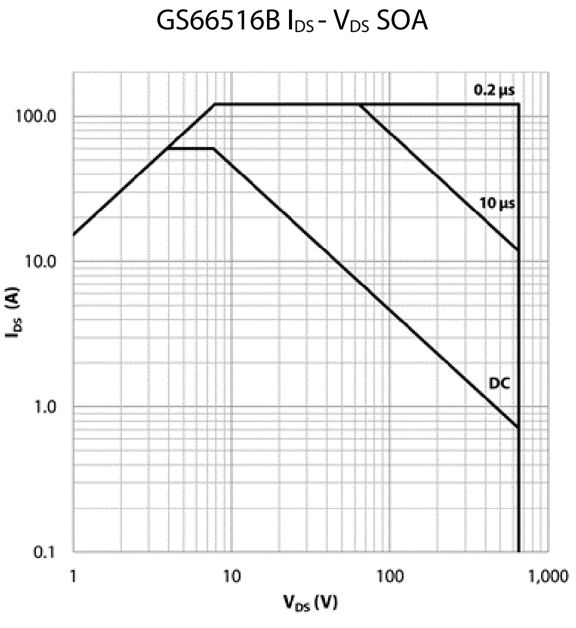

GS66516B I_{DS} - V_{DS} SOA

Figure 12: Safe Operating Area @ T_{case} = 25 °C

Electrical Performance Graphs

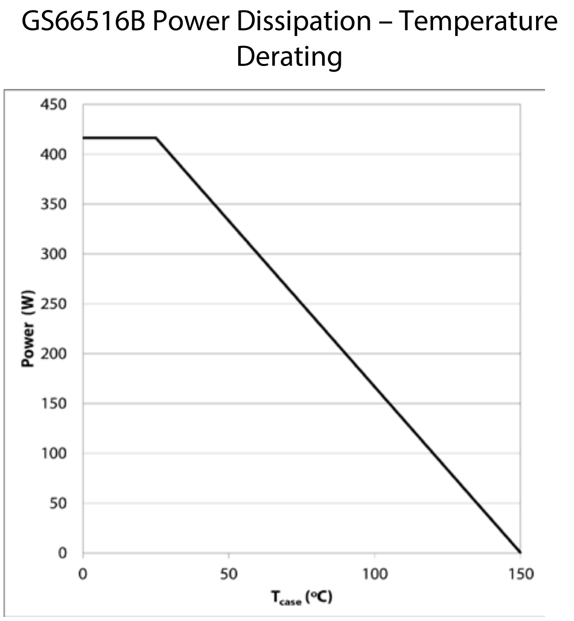

GS66516B Power Dissipation – Temperature Derating

Figure 13: Derating vs. Case Temperature

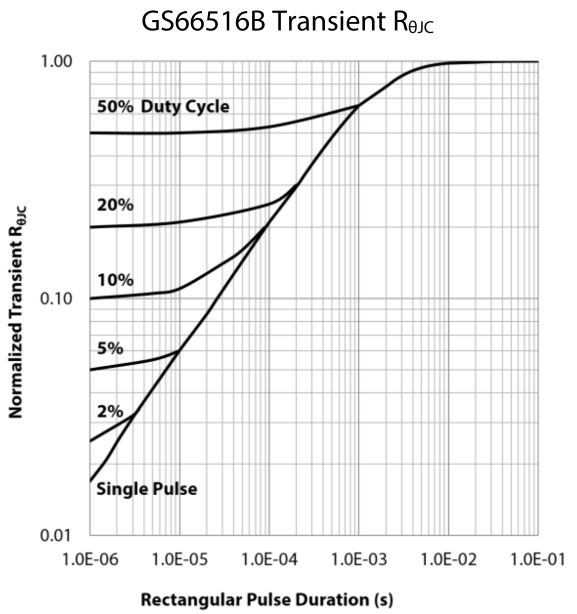

GS66516B Transient $R_{\theta JC}$

Figure 14: Transient Thermal Impedance

Test Circuits

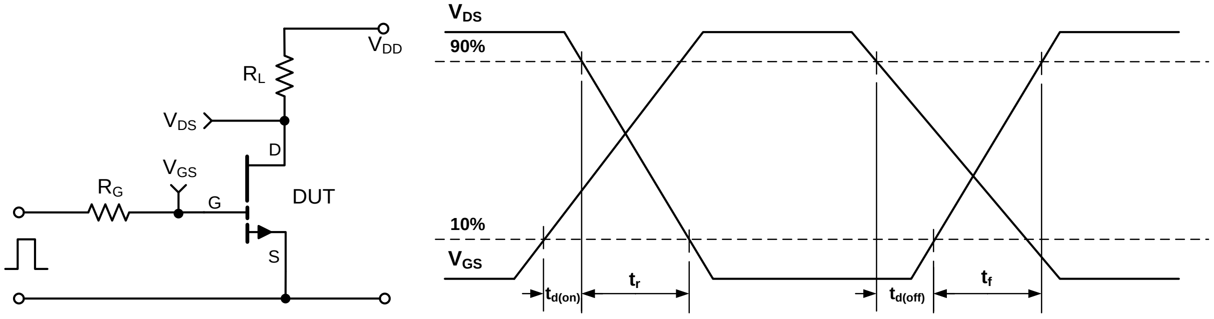


Figure 15: GS66516B switching time test circuit and waveforms

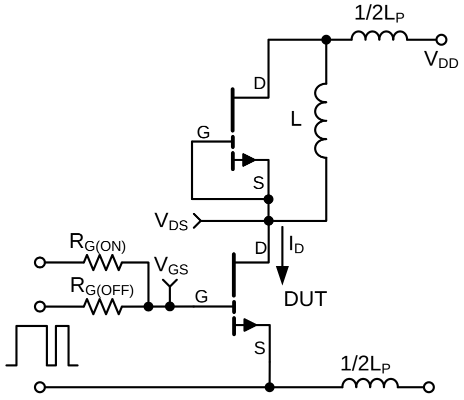


Figure 16: GS66516B Switching Loss Test Circuit

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note GN001, Application Guide – Design with GaN Enhancement Mode HEMT" at www.gansystems.com

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight enough tolerance on the gate voltage. Therefore, special care should be taken when you select and use half bridge drivers. Please see the gate driver application note, (GN001), for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very high speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate's parasitic oscillation.

Source Sensing

The GS66516B has two dedicated source sense pads. The GaN*PX*® packaging utilizes no wire bonds so the source connection is very low inductance. The dedicated source sense pin will further enhance performance by eliminating the common source inductance if a dedicated gate drive signal kelvin connection is created. This can be achieved by connecting the gate drive signal from the driver to the gate pad on the GS66516B and returning from the source sense pad on the GS66516B to the driver ground reference.

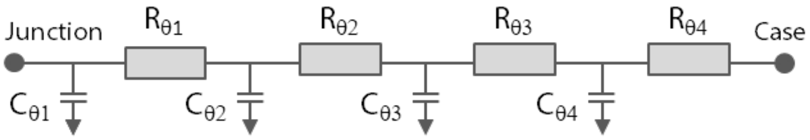
Thermal

The substrate is internally connected to the source/thermal pad on the bottom-side of the GS66516B. The transistor is designed to be cooled using the printed circuit board. The Drain pad is not as thermally conductive as the thermal pad. However, adding more copper under the Drain pad will improve thermal performance by reducing the package temperature.

Thermal Modeling

RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

GS66516B RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta1}$ = 0.008	$C_{\theta1}$ = 1.48E-04
$R_{\theta2}$ = 0.124	$C_{\theta2}$ = 1.37E-03
$R_{\theta3}$ = 0.130	$C_{\theta3}$ = 12.0E-03
$R_{\theta4}$ = 0.008	$C_{\theta4}$ = 3.7E-03

For more detail, please refer to Application Note GN007 “Modeling Thermal Behavior of GaN Systems’ GaN*PX*™ Using RC Thermal SPICE Models” available at www.gansystems.com

Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.
Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, V_{GD}, exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, $BV_{DS,}$ is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and doesn't change with negative gate voltage. A transient drain-to-source voltage of 750 V for 1 µs is acceptable.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS66516B device to be specified to 150 °C. The device can handle at least 3 reflow cycles.

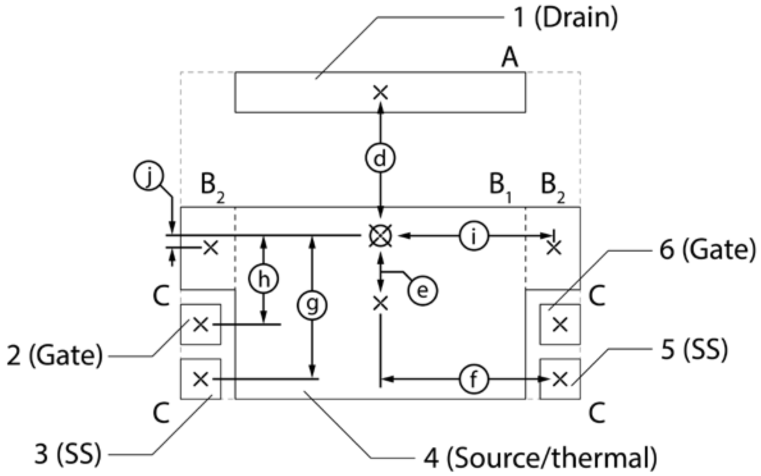
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 - 120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues.

Recommended Minimum Footprint for Printed Circuit Board



Pad sizes

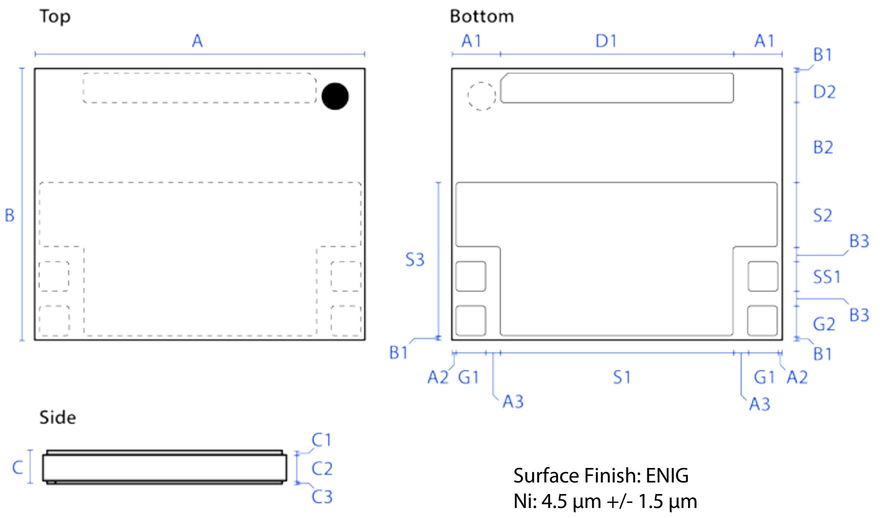
	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	7.97	1.10	0.314	0.043
B_1	7.97	5.27	0.314	0.207
B_2	1.50	2.27	0.059	0.089
C	1.10	1.10	0.043	0.043

Dimensions

	mm	Inches
d	3.94	0.155
e	1.85	0.073
f	4.94	0.194
g	3.94	0.155
h	2.44	0.096
i	4.735	0.186
j	0.35	0.014

☐ PCB pad opennings
⬚ Package outline

Package Dimensions

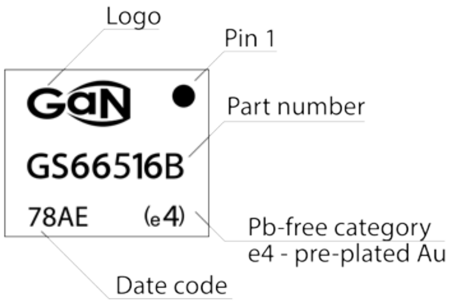


	mm	Inches	
A	11.0	0.433	± 0.10 mm (0.004”)
A1	1.565	0.062	± 0.05 mm (0.002”)
A2	0.065	0.003	± 0.05 mm (0.002”)
A3	0.50	0.020	
B	9.00	0.354	± 0.10 mm (0.004”)
B1	0.065	0.003	± 0.05 mm (0.002”)
B2	2.70	0.106	
B3	0.50	0.020	
C	0.54	0.021	± 15%
C1	0.07	0.003	
C2	0.43	0.017	
C3	0.04	0.002	
D1	7.87	0.310	
D2	1.00	0.039	
G1	1.00	0.039	
G2	1.00	0.039	
S1	7.87	0.310	
S2	2.17	0.085	
S3	5.17	0.204	
SS1	1.00	0.039	

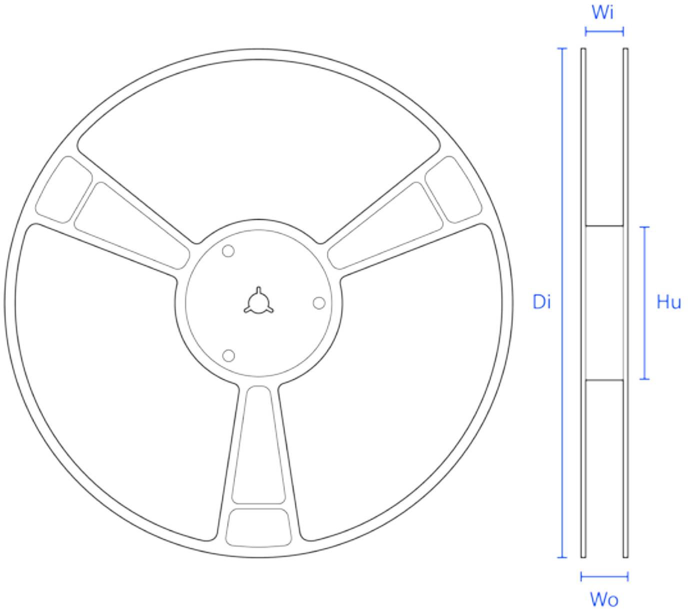
Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

Note: Inch measurements are approximate values

GaN*PX*® Part Marking

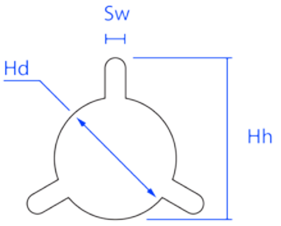


GS660516B GaN*PX*® Tape and Reel Information

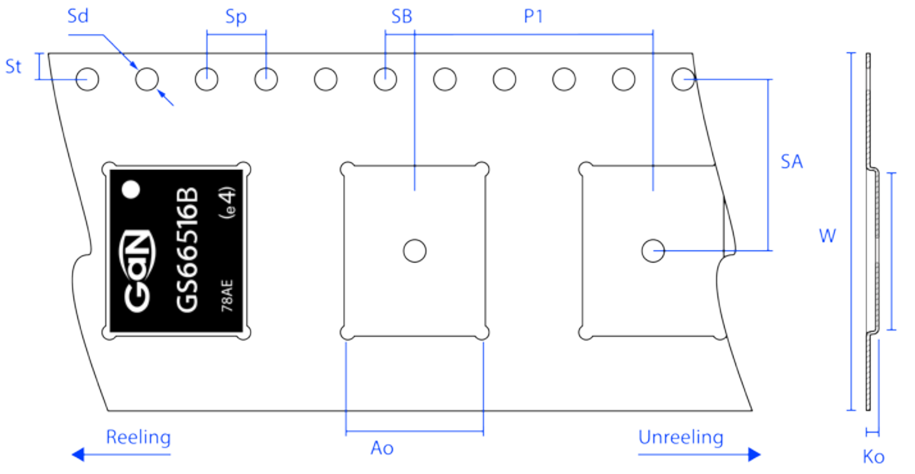


Dimensions (mm)

	13” reel (330 mm)		7” mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	178.0	+ 1.0 / - 0.0
Wo	30.4	MAX	27.7	+/-1.0
Wi	24.4	+ 2.0 / - 0.0	25.0	+ 1.0 / - 0.0
Hu	100.0	+/- 1.5	60.0	+ 1.0 / - 0.0
Hh	17.2	+/- 0.2	17.0	+/- 0.5
Sw	2.2	+/- 0.2	2.0	+/- 0.5
Hd	13.0	+ 0.5 / - 0.2	13.0	+/- 0.2



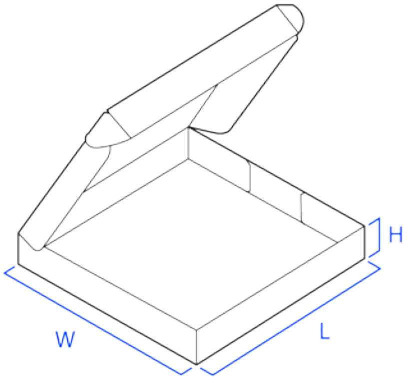
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	16.00	+/- 0.1
W	24.00	+ 0.3 / - 0.1
Ko	1.14	+/- 0.1
Ao	9.48	+/- 0.1
Bo	11.43	+/- 0.1
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	11.50	+/- 0.1
SB	2.00	+/- 0.1

Tape and Reel Box Dimensions



Outside dimensions (mm)

	7” mini-reel	13” tape-reel
W	197	342
L	204	355
H	32	53

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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