

## 150-mA, 30-V, UltraLow $I_Q$ , Low-Dropout Regulators with Enable

### FEATURES

- UltraLow  $I_Q$ : 1  $\mu$ A
- Reverse Current Protection
- Low  $I_{SHUTDOWN}$ : 150 nA
- Input Voltage Range: 2.5 V to 30 V
- Supports 200-mA Peak Output
- Low Dropout: 300 mV at 50 mA
- 2% Accuracy Over Temperature
- Available in Fixed-Output Voltages: 1.5 V to 6.5 V
- Thermal Shutdown and Overcurrent Protection
- Packages: SOT23-5

### APPLICATIONS

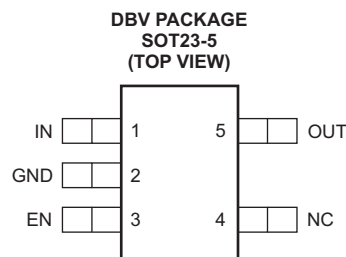
- Zigbee™ Networks
- Home Automation
- Metering
- Weighing Scales
- Portable Power Tools
- Remote Control Devices
- Wireless Handsets, Smart Phones, PDAs, WLAN and Other PC Add-On Cards
- White Goods

### DESCRIPTION

The TPS709xx series of low-dropout (LDO) linear regulators are ultralow quiescent current devices that are designed for power-sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. Quiescent current of only 1  $\mu$ A makes the devices ideal solutions for battery-powered, always ON systems that require very little idle state power dissipation. All devices have a thermal shutdown and current limit for safety.

The LDO can be put into shutdown mode by pulling the EN pin low. The leakage current in this mode goes down to less than 150 nA.

The TPS709xx series is available in an SOT23-5 package.



PRODUCT PREVIEW



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### AVAILABLE OPTIONS<sup>(1)</sup>

PRODUCT	V <sub>OUT</sub>
TPS709xxyyyz	<b>XX</b> is nominal output voltage (for example 28 = 2.8 V). <b>E</b> is TBD <b>YYY</b> is package designator <b>Z</b> is package quantity; <b>R</b> is for reel (3000 pieces), <b>T</b> is for tape (250 pieces)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Specified at T<sub>J</sub> = –40°C to +125°C, unless otherwise noted. All voltages are with respect to GND.

		VALUE		UNIT
		MIN	MAX	
Voltage	V <sub>IN</sub>	–0.3	+30	V
	V <sub>EN</sub>	–0.3	+7	V
	V <sub>OUT</sub>	–0.3	+7	V
Maximum output current	I <sub>OUT</sub>	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P <sub>DISS</sub>	See the <a href="#">Thermal Information</a> table		
Temperature	Junction, T <sub>J</sub>	–55	+150	°C
	Storage, T <sub>stg</sub>	–55	+150	°C
Electrostatic discharge (ESD) rating	Human body model (HBM)		2	kV
	Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS709xx	UNITS
		DBV (SOT23)	
		5 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	212.1	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	78.5	
θ <sub>JB</sub>	Junction-to-board thermal resistance	39.5	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.86	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	38.7	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

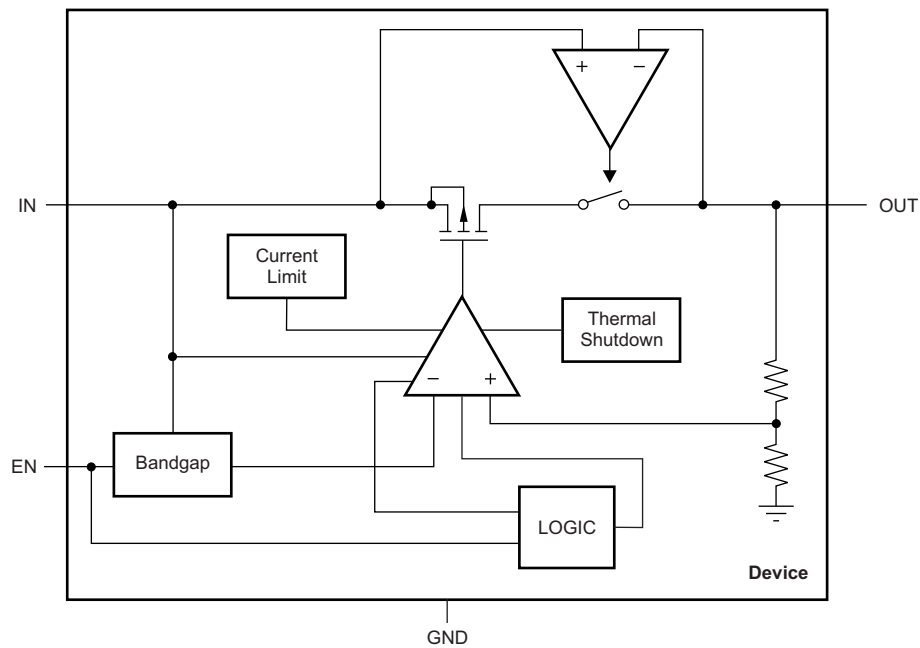
## ELECTRICAL CHARACTERISTICS

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{IN} = V_{OUT(\text{typ})} + 1\text{ V}$  or  $2.5\text{ V}$  (whichever is greater),  $I_{OUT} = 1\text{ mA}$ ,  $V_{EN} = 2\text{ V}$ , and  $C_{IN} = C_{OUT} = 2.2\text{-}\mu\text{F}$  ceramic, unless otherwise noted. Typical values are at  $T_A = +25^{\circ}\text{C}$ .

PARAMETER	TEST CONDITIONS	TPS709xx			UNIT
		MIN	TYP	MAX	
$V_{IN}$	Input voltage range	2.5		28	V
$V_{OUT}$	Output voltage range	1.5		6.5	V
$V_O$	DC output accuracy	–2		2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(\text{NOM})} + 1\text{ V}$ , $2.5\text{ V} \leq V_{IN} \leq 24\text{ V}$			mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	$0\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$			mV
$V_{DO}$	Dropout voltage <sup>(1)</sup>	$I_{OUT} = 150\text{ mA}$			mV
		$I_{OUT} = 50\text{ mA}$			mV
$I_{CL}$	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(\text{NOM})}$			mA
$I_{GND}$	Ground pin current	$I_{OUT} = 0\text{ mA}$			$\mu\text{A}$
		$I_{OUT} = 100\text{ mA}$			$\mu\text{A}$
		$I_{OUT} = 150\text{ mA}$			$\mu\text{A}$
$I_{SHUTDOWN}$	Shutdown pin current	$V_{EN} \leq 0.4\text{ V}$ , $V_{IN} = 2.0\text{ V}$			nA
PSRR	Power-supply rejection ratio	$f = 10\text{ Hz}$			dB
		$f = 100\text{ Hz}$			dB
		$f = 1\text{ kHz}$			dB
$V_N$	Output noise voltage	BW = 100 Hz to 100 kHz, $I_{OUT} = 10\text{ mA}$ , $V_{IN} = 2.3\text{ V}$ , $V_{OUT} = 1.8\text{ V}$			$\mu\text{V}_{\text{RMS}}$
$t_{STR}$	Startup time <sup>(2)</sup>	150			$\mu\text{s}$
$V_{EN(\text{HI})}$	Enable pin high (enabled)	0.9		5.5	V
$V_{EN(\text{HI})}$	Enable pin high (disabled)	0		0.4	V
$I_{EN}$	EN pin current	EN = 5.5 V, $I_{OUT} = 10\text{ }\mu\text{A}$			nA
$t_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing			$^{\circ}\text{C}$
		Reset, temperature decreasing			$^{\circ}\text{C}$
$T_J$	Operating junction temperature	–40		+125	$^{\circ}\text{C}$

(1)  $V_{DO}$  is measured for devices with  $V_{IN} = 0.98 \times V_{OUT(\text{NOM})}$ .

(2) Startup time = time from EN assertion to  $0.95 \times V_{OUT(\text{NOM})}$ .

**FUNCTIONAL BLOCK DIAGRAM****Figure 1. Fixed-Voltage Version**

## TYPICAL CHARACTERISTICS

Over operating temperature range ( $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ),  $I_{\text{OUT}} = 10\text{ mA}$ ,  $V_{\text{EN}} = 1.0\text{ V}$ ,  $C_{\text{OUT}} = 2.2\text{ }\mu\text{F}$ , and  $V_{\text{IN}} = V_{\text{OUT(TYP)}} + 1\text{ V}$  or  $2.5\text{ V}$  (whichever is greater), unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ .

PRODUCT PREVIEW

## APPLICATION INFORMATION

The TPS709xx are a series of devices that belong to a new family of next-generation, low-dropout (LDO) voltage regulators. They consume low quiescent current and deliver excellent line and load transient performance. This performance, combined with low noise, very good PSRR with little ( $V_{IN} - V_{OUT}$ ) headroom, makes these devices ideal for RF portable applications, current limit, and thermal protection. The TPS709xx are specified from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance (such as PSRR, output noise, and transient response), it is recommended that the board be designed with separate ground planes for  $V_{IN}$  and  $V_{OUT}$ , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the device GND pin.

### INTERNAL CURRENT LIMIT

The TPS709xx internal current limit helps to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and can be measured as  $V_{OUT} = I_{LIMIT} \times R_{LOAD}$ . The PMOS pass transistor dissipates  $[(V_{IN} - V_{OUT}) \times I_{LIMIT}]$  until a thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the [Thermal Information](#) section for more details.

The TPS709xx is characterized over the recommended operating output current range up to 150 mA. The internal current limit begins to limit the output current at a minimum of 260 mA of output current. The TPS709xx continues to operate for output currents between 150 mA and 260 mA but some data sheet parameters may not be met, resulting in increased power dissipation.

### DROPOUT VOLTAGE

The TPS709xx uses a PMOS pass transistor to achieve low dropout. When  $(V_{IN} - V_{OUT})$  is less than the dropout voltage ( $V_{DO}$ ), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the  $R_{DS(ON)}$  of the PMOS pass element.  $V_{DO}$  approximately scales with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as  $(V_{IN} - V_{OUT})$  approaches dropout. This effect is shown in the [Typical Characteristics](#).

### TRANSIENT RESPONSE

As with any regulator, increasing the output capacitor size reduces over- and undershoot magnitude, but increases transient response duration.

### UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS709xx uses an undervoltage lockout (UVLO) circuit to keep the output shut off until the internal circuitry operates properly.

### REVERSE CURRENT PROTECTION

The TPS709xx have integrated reverse current protection. Reverse current protection prevents current from flowing from the OUT pin to the IN pin when output voltage is higher than input voltage. The reverse current protection circuitry places the power path in high impedance when it detects that the output voltage is higher than the input voltage. This setting reduces leakage current from the output to the input to TBD nA, typical. The reverse current protection is always active regardless of the enable pin logic state or if the OUT pin voltage is greater than 2.0 V. Reverse current can flow if the output voltage is less than 2.0 V and if input voltage is less than the output voltage.

## THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C, maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The TPS709xx internal protection circuitry is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS709xx into thermal shutdown degrades device reliability.

## POWER DISSIPATION

The ability to remove heat from the die is different for each package type, which presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC low and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation ( $P_D$ ) is equal to the product of the output current and the voltage drop across the output pass element, as shown in [Equation 1](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (1)$$

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS70912DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70912DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS709135DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS709135DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70916DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70916DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70918DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70918DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70919DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70919DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70925DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70925DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70927DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70927DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70928DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70928DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70930DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70930DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	
TPS70933DBVR	PREVIEW	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70933DBVT	PREVIEW	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS70950DBVR	PREVIEW	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	
TPS70950DBVT	PREVIEW	SOT-23	DBV	5	250	TBD	Call TI	Call TI	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



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<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

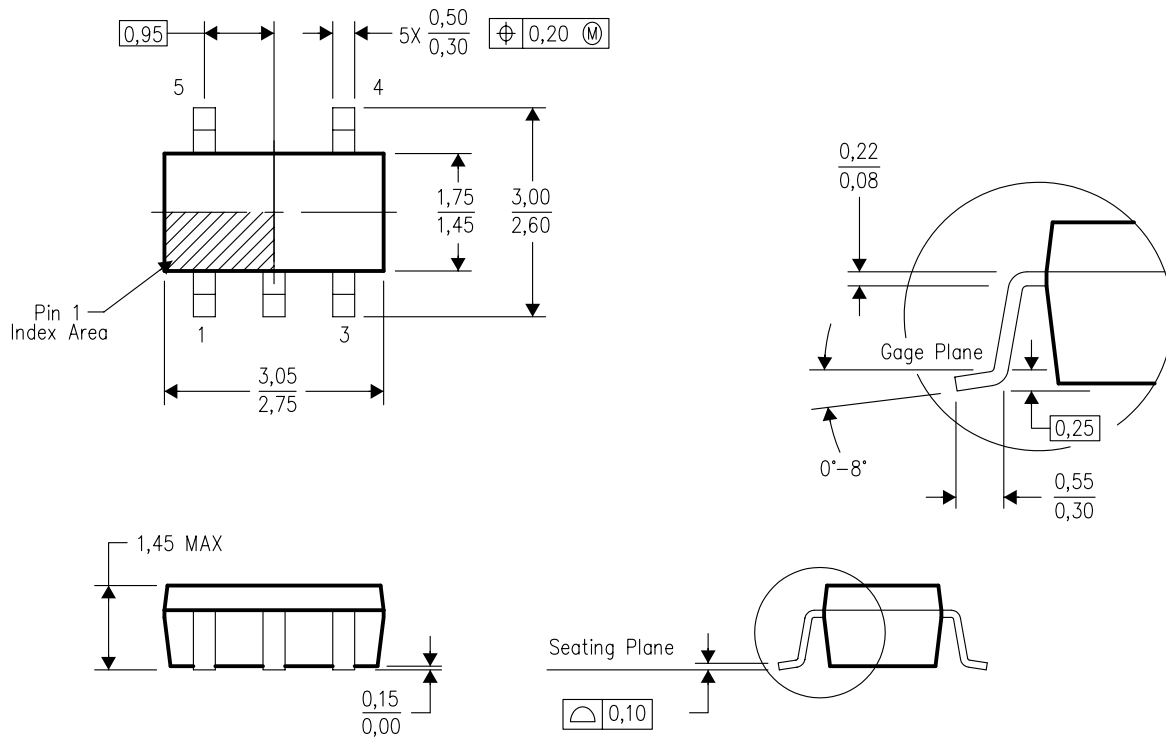
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4073253-4/K 03/2006

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.

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Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
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