

ON Semiconductor®



KAF-1001 IMAGE SENSOR

1024 (H) X 1024 (V) FULL FRAME CCD IMAGE SENSOR



JUNE 18, 2014

DEVICE PERFORMANCE SPECIFICATION

REVISION 1.1 PS-0033



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Summary Specification

KAF-1001 Image Sensor

DESCRIPTION

The KAF-1001 Image Sensor is a high-performance charge-coupled device (CCD) designed for a wide range of image sensing applications.

The sensor incorporates true two-phase CCD technology, simplifying the support circuits required to drive the sensor as well as reducing dark current without compromising charge capacity. The sensor also utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode.

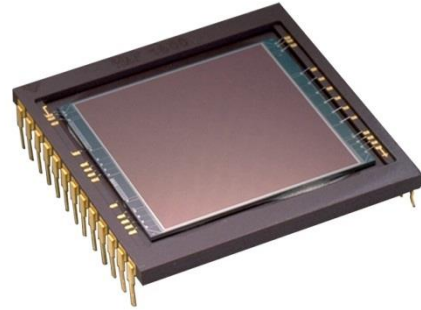
Selectable on-chip output amplifiers allow operation to be optimized for different imaging needs: Low Noise (when using the high-sensitivity output) or Maximum Dynamic Range (when using the low-sensitivity output).

FEATURES

- True Two Phase Full Frame Architecture
- TRUESENSE Transparent Gate Electrode for high sensitivity
- 100% Fill Factor
- Low Dark Current
- Single Readout Register
- User-selectable outputs allow either Low Noise or High Dynamic Range operation

APPLICATIONS

- Scientific
- Medical



Parameter	Typical Value
Architecture	Full Frame CCD
Pixel Count	1024 (H) x 1024 (V)
Pixel Size	24 μm (H) x 24 μm (V)
Active Image Size	24.6 mm (H) x 24.6 mm (V)
Chip Size	28.6 mm (H) x 25.5 mm (V)
Optical Fill-Factor	100%
Saturation Signal	240,000 electrons
High Sensitivity Output	650,000 electrons
High Dynamic Range	
Output Sensitivity	
High Sensitivity Output	11 $\mu\text{V}/\text{electron}$
High Dynamic Range	2 $\mu\text{V}/\text{electron}$
Readout Noise (1 MHz)	15 electrons rms
Dark Current	<30 pA/cm ²
(25 °C, Accumulation Mode)	
Dark Current Doubling Rate	5–6 °C
Dynamic Range (Sat Sig/Dark Noise)	
High Sensitivity Output	83 dB
High Dynamic Range	97 dB
Quantum Efficiency	40%, 55%, 65%
(450, 550, 650 nm)	
Maximum Data Rate	
High Sensitivity Output	5 MHz
High Dynamic Range	2 MHz
Transfer Efficiency (2 MHz, to –40 °C)	>0.99997
Package	CERDIP Package (sidebrazed)
Cover Glass	Clear



Ordering Information

Catalog Number	Product Name	Description	Marking Code
4H0016	KAF- 1001-AAA-CP-B1	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 1	KAF-1001-AAA [Serial Number]
4H0017	KAF- 1001-AAA-CP-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Grade 2	
4H0019	KAF- 1001-AAA-CP-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Taped Clear Cover Glass, no coatings, Engineering Sample	
4H0842	KAF- 1001-AAA-CB-AE	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Engineering Sample	
4H0847	KAF- 1001-AAA-CB-B2	Monochrome, No Microlens, CERDIP Package (sidebrazed), Clear Cover Glass (no coatings), Grade 2	
4H0080	KEK-4H0080-KAF-1001-12-5	Evaluation Board (Complete Kit)	N/A

See Application Note *Product Naming Convention* for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.truesenseimaging.com.

Please address all inquiries and purchase orders to:

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Device Description

ARCHITECTURE

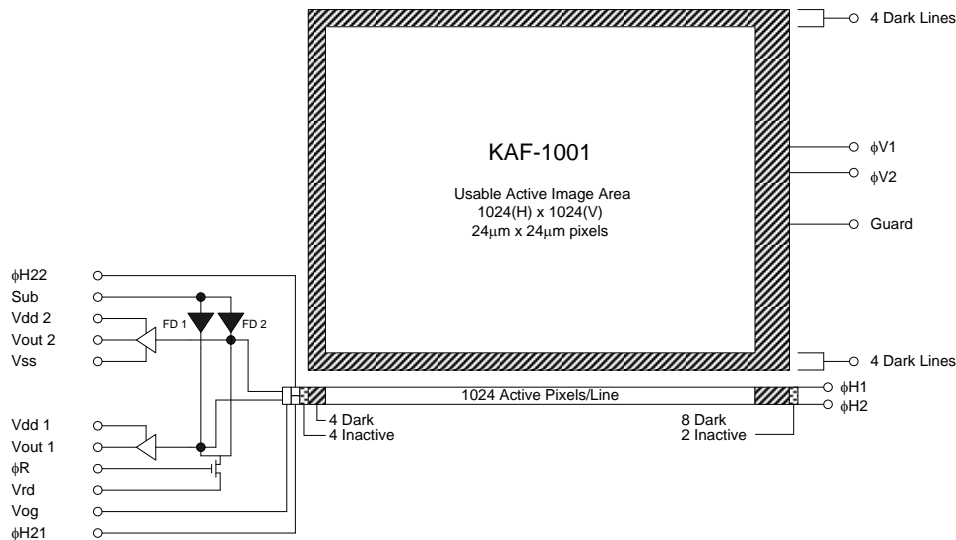


Figure 1: Block Diagram

Notes:

1. Shaded areas represent 4 non-imaging pixels at the beginning and 8 non-imaging pixels at the end of each line. There are also 4 non-imaging lines at the top and bottom of each frame.

Refer to the block diagram in Figure 1. The KAF-1001 consists of one vertical (parallel) CCD shift register, one horizontal (serial) CCD shift register and a selectable high or low gain output amplifier. Both registers incorporate true two-phase buried channel technology. The vertical register consists of 24 µm x 24 µm photo-capacitor sensing elements (pixels) which also serves as the transport mechanism. The pixels are arranged in a 1024 (H) x 1024 (V) array; an additional 12 columns (4 at the left and 8 at the right) and 8 rows (4 each at top and bottom) of non-imaging pixels are added as dark reference. Because there is no storage array, this device must be synchronized with strobe illumination or shuttered during readout.

Output Structure

The final gate of the horizontal register is split into two sections, φH21 and φH22. The split gate structure allows the user to select either of the two output amplifiers. To use the high dynamic range single-stage output (Vout1), tie φH22 to a negative voltage to block charge transfer, and tie φH21 to φH2 to transfer charge. To use the high sensitivity two-stage output (Vout2), tie φH21 to a negative voltage and φH22 to φH2. The charge packets are then dumped onto the appropriate floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the simple expression $\Delta V_{fd} = \Delta Q / C_{fd}$. The translation from electrons to voltages is called the output sensitivity or charge-to-voltage conversion. After the output has been sensed off-chip, the reset clock (φR) removes the charge from the floating diffusion via the reset drain (VRD). This, in turn, returns the floating diffusion potential to the reference level determined by the reset drain voltage.

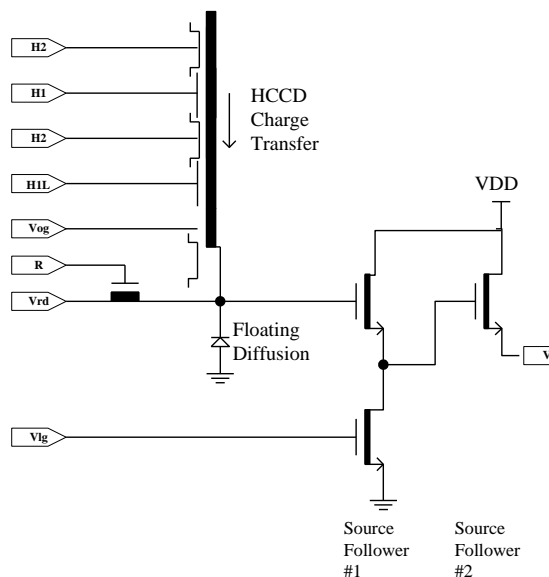


Figure 2: Output Schematic

IMAGE ACQUISITION

An image is acquired when incident light, in the form of photons, falls on the array of pixels in the vertical CCD register and creates electron-hole pairs (or simply electrons) within the silicon substrate. This charge is collected locally by the formation of potential wells created at each pixel site by induced voltages on the vertical register clock lines ($\phi V1$, $\phi V2$). These same clock lines are used to implement the transport mechanism as well. The amount of charge collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength until the potential well capacity is exceeded. At this point charge will 'bloom' into vertically adjacent pixels.

CHARGE TRANSPORT

Integrated charge is transported to the output in a two-step process. Rows of charge are first shifted line by line into the horizontal CCD. 'Lines' of charge are then shifted to the output pixel by pixel. Referring to the timing diagram, integration of charge is performed with $\phi V1$ and $\phi V2$ held low. Transfer to horizontal CCD begins when $\phi V1$ is brought high causing charge from the $\phi V1$ and $\phi V2$ gates to combine under the $\phi V1$ gate.

$\phi V1$ and $\phi V2$ now reverse their polarity causing the charge packets to 'spill' forward under the $\phi V2$ gate of the next pixel. The rising edge of $\phi V2$ also transfers the first line of charge into the horizontal CCD. A second phase transition places the charge packets under the $\phi V1$ electrode of the next pixel. The sequence completes when $\phi V1$ is brought low. Clocking of the vertical register in this way is known as accumulation mode clocking. Next, the horizontal CCD reads out the first line of charge using traditional complementary clocking (using $\phi H1$ and $\phi H2$ pins) as shown. The falling edge of $\phi H2$ forces a charge packet over the output gate (OG) onto one of the output nodes (floating diffusion) which controls the output amplifier. The cycle repeats until all lines are read.



PHYSICAL DESCRIPTION

Pin Description and Device Orientation

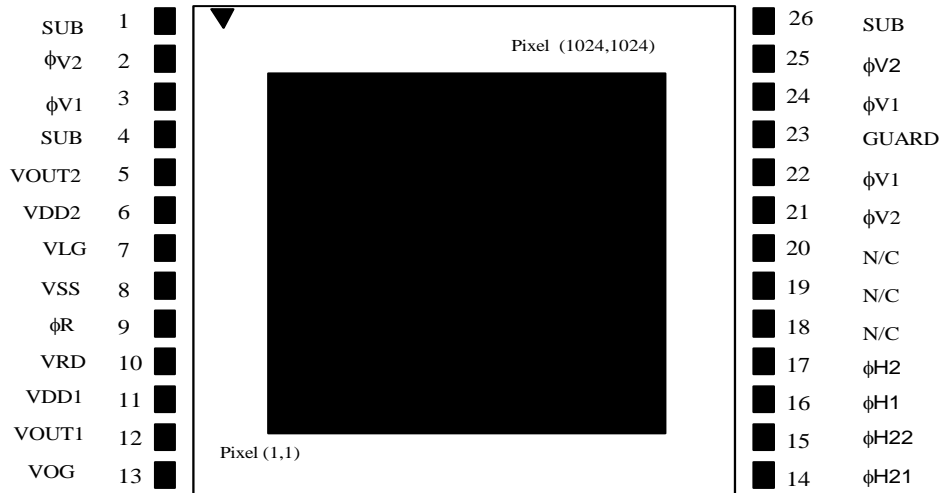


Figure 3: Pinout Diagram



Pin	Name	Description
1	Substrate	Substrate
2	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
3	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
4	Substrate	Substrate
5	VOUT2	Video Output from High Sensitivity Two-Stage Amplifier
6	VDD2	High Sensitivity Two-Stage Amplifier Supply
7	VLG	First Stage Load Transistor Gate for Two-Stage Amplifier
8	VSS	Output Amplifier Return
9	ϕR	Reset Clock
10	VRD	Reset Drain
11	VDD1	High Dynamic Range Single-Stage Amplifier Supply
12	VOUT1	Video Output from High Dynamic Range Single-Stage Amplifier
13	OG	Output Gate

Pin	Name	Description
14	$\phi H21$	Last Horizontal (Serial) CCD Phase - Split Gate
15	$\phi H22$	Last Horizontal (Serial) CCD Phase - Split Gate
16	$\phi H1$	Horizontal (Serial) CCD Clock - Phase 1
17	$\phi H2$	Horizontal (Serial) CCD Clock - Phase 2
18	N/C	No Connection
19	N/C	No Connection
20	N/C	No Connection
21	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
22	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
23	Guard	Guard Ring
24	$\phi V1$	Vertical (Parallel) CCD Clock – Phase 1
25	$\phi V2$	Vertical (Parallel) CCD Clock – Phase 2
26	Substrate	Substrate

Notes:

1. Pins 3, 22, and 24 must be connected together - only one Phase 1 clock driver is required.
2. Pins 2, 21, and 25 must be connected together - only one Phase 2 clock driver is required.



Imaging Performance

TYPICAL OPERATIONAL CONDITIONS

All values derived using nominal operating conditions with the recommended timing. Correlated doubling sampling of the output is assumed and recommended. Many units are expressed in electrons: to convert to voltage, multiply by the amplifier sensitivity.

SPECIFICATIONS

Electro-Optical

Description	Symbol	Min	Nom	Max	Units	Notes	Verification Plan
Optical Fill Factor	FF		100		%		
Photoresponse Non-uniformity	PRNU			5	% rms	Full Array	die ¹⁰
Quantum Efficiency (450, 550, 650 nm)	QE						design ¹¹

CCD Parameters Common to Both Outputs

Description	Symbol	Min	Nom	Max	Units	Notes	Verification Plan
Sat. Signal - Vccd Register	$N_{e\text{-sat}}$	450	500		ke^-	2	design ¹¹
Dark Current	Jd		15.3 550	30 1080	$\mu A/cm^2$ $e^-/pixel/sec$	25 °C (mean of all pixels)	die ¹⁰
Dark Current Doubling Temp	DCDR	5	6	7	°C		design ¹¹
Dark Signal Non-uniformity	DSNU			1080	$e^-/pix/sec$	4	die ¹⁰
Charge Transfer Efficiency	CTE		.99997			5	die ¹⁰
V-H CCD Transfer Time	t_{VH}		32		μs	6,7	design ¹¹
Blooming Suppression	Bs		none				

CCD Parameters Specific to High Output Amplifier

Description	Symbol	Min	Nom	Max	Units	Notes	Verification Plan
Output Sensitivity	V_{out}/Ne^-	9	11		$\mu V/electron$		design ¹¹
Sat. Signal	$N_{e\text{-sat}}$	180	200	240	ke^-	1	design ¹¹
Total Sensor Noise	$n_{e\text{-total}}$		13	20	$e^- rms$	8	design ¹¹
Horizontal CCD Frequency:	f_H		2	5	MHz	6	design ¹¹
Dynamic Range:	DR	79	83		dB	9	design ¹¹

CCD Parameters Specific to Low Gain (High Dynamic Range) Output Amplifier

Description	Symbol	Min	Nom	Max	Units	Notes	Verification Plan
Output Sensitivity	V_{out}/Ne^-	1.7	2		$\mu V/electron$		die ¹⁰
Sat. Signal	$N_{e\text{-sat}}$	1400	1500	1800	ke^-	3	design ¹¹
Total Sensor Noise	$n_{e\text{-total}}$		22	30	$e^- rms$	8	die ¹⁰
Horizontal CCD Frequency:	f_H		0.5	2	MHz	6	design ¹¹
Dynamic Range :	DR	93	97		dB	9	design ¹¹



Notes:

1. Point where the output saturates when operated with nominal voltages.
2. Signal level at the onset of blooming in the vertical (parallel) CCD register
3. Maximum signal level at the output of the high dynamic range output. This signal level will only be achieved when binning pixels containing large signals.
4. None of 64 sub arrays (128 x 128) exceed the maximum dark current specification.
5. For 2 MHz data rate and T = 30 °C to -40 °C.
6. Using maximum CCD frequency and/or minimum CCD transfer times may compromise performance
7. Time between the rising edge of $\phi V1$ and the first falling edge of $\phi H1$
8. At $T_{\text{integration}} = 0$; data rate = 1 MHz; temperature = -30 °C
9. Uses $20\text{LOG}(N_{e_{\text{sat}}}^- / n_{e_{\text{total}}}^-)$ where $N_{e_{\text{sat}}}^-$ refers to the amplifier saturation signal.
10. A parameter that is measured on every sensor during production testing.
11. A parameter that is quantified during the design verification activity.



Typical Performance Curves

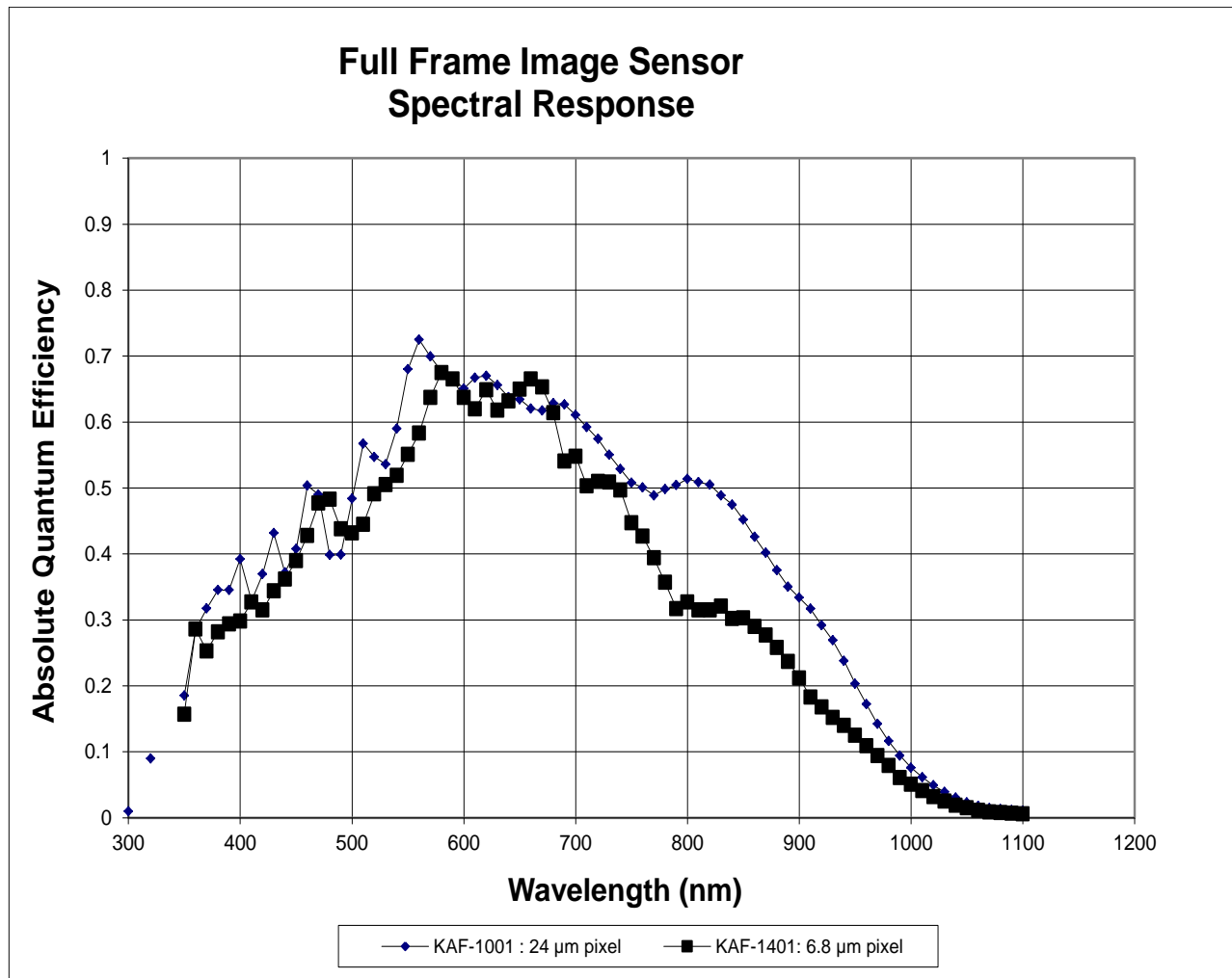


Figure 4: Typical Spectral Response

Figure 4 shows a representative spectral response of front side illuminated transparent gate full frame image sensors. The KAF-1001 with 24 μm pixels has higher response than the 6.8 μm pixel sensor at wavelengths greater than 750 nm because it is constructed on a lower resistivity silicon substrate. The resulting collection volume of each pixel more efficiently collects signal generated deeper within the silicon.

Most of the two phase CCD pixels are designed so that each of the electrodes occupies half of the pixel area. The KAF-1001 was not designed this way but instead is designed with the transparent electrode occupying greater than half the pixel area. This further improves the benefits of the transparent gate.



KAF-1001 Dark Current

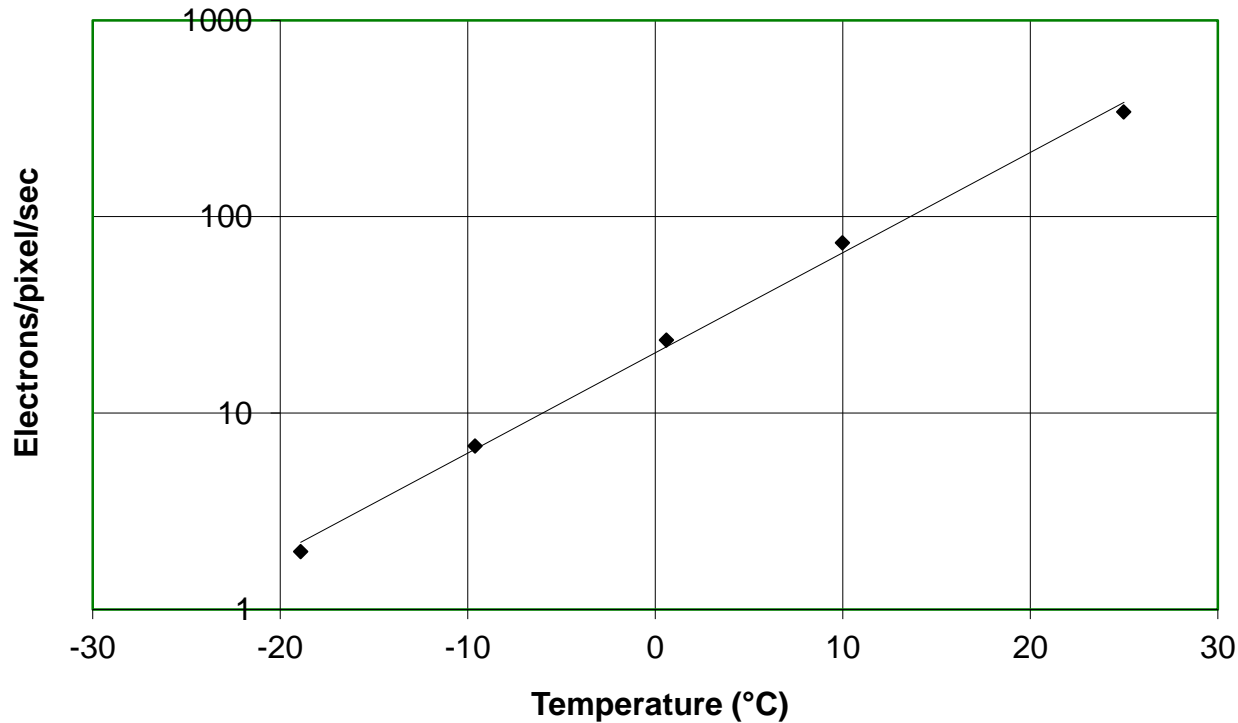


Figure 5: Dark Current as a Function of Temperature



Operation

ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	-100	+80	C	At Device
Operating Temperature	T_{OP}	-50	+50	C	At Device
Voltage	All Clocks	-16	+16	V	VSUB = 0 V
Voltage	OG	0	+8	V	VSUB = 0 V
Voltage	VRD, VSS, VDD, GUARD	0	+20	V	VSUB = 0 V
Current	Output Bias Current (IDD)		10	mA	
Capacitance	Output Load Capacitance (CLOAD)		10	pF	
Frequency/Time	$\phi V1$, $\phi V2$ Pulse Width	8		μs	
Frequency/Time	$\phi H1$, $\phi H2$		5	MHz	
Frequency/Time	ϕR Pulse Width	20		ns	

Warning:

For maximum performance, built-in gate protection has been added only to the OG pin. These devices require extreme care during handling to prevent electrostatic discharge (ESD) induced damage.

DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Pin Impedance	Notes
Substrate	VSUB	0.0	0.0	0.0	V	Common	
Output Amplifier Supply	VDD	15.0	+17.0	17.5	V	5 pF, 2 K Ω	1
Output Amplifier Return	VSS	1.4	+2.0	2.1	V	5 pF, 2 K Ω	
Reset Drain	VRD	11.5	+12	12.5	V	5 pF, 1 M Ω	
Output Gate	OG	3.0	+4.0	4.5	V	5 pF, 10 M Ω	
Guard Ring	GUARD	7.0	+10.0	15.0	V	350 pF, 10 M Ω	
Load Gate	VLG	VSS - 0.5	VSS + 0.0	VSS + 1.0	V		

Notes:

1. Vdd = 17 volts for applications where the expected output voltage > 2.0 volts. For applications where the expected useable output voltage is < 2 volts, Vdd can be reduced to 15 volts.



AC OPERATING CONDITIONS

Clock Levels

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Pin Impedance
Vertical Clock - Phase 1	$\phi V1$	Low	-10.25	-10	-9.8	V	200 nF, 10 M Ω
Vertical Clock - Phase 1	$\phi V1$	High	0.0	0	1.0	V	
Vertical Clock - Phase 2	$\phi V2$	Low	-10.25	-10.0	-9.8	V	200 nF, 10 M Ω
Vertical Clock - Phase 2	$\phi V2$	High	0.0	0	1.0	V	C $\phi V1-V2$ = 100 nF
Horizontal Clock - Phase 1	$\phi H1$	Low	-2.2	-2.0	-1.8	V	400 pF, 10 M Ω
Horizontal Clock - Phase 1	$\phi H1$	High	7.8	+8.0	8.2	V	
Horizontal Clock - Phase 2	$\phi H2$	Low	-2.2	-2.0	-1.8	V	250 pF, 10 M Ω
Horizontal Clock - Phase 2	$\phi H2$	High	7.8	+8.0	8.2	V	C $\phi H1-H2$ = 200 pF
Reset Clock	ϕR	Low	2.0	3.0	3.5	V	10 pF, 10 M Ω
Reset Clock	ϕR	High	9.5	10.0	11.0	V	

Description	Symbol	Level	Using the High Gain Output (Vout2)			Using the High Dynamic Range Output (Vout1)			Units	Pin Impedance
			Min	Nom	Max	Min	Nom	Max		
Horizontal Clock - Phase 1	$\phi H21$	Low	-4	$\phi H2$ low	$\phi H2$ low		$\phi H2$		V	10 pF, 10 M Ω
Horizontal Clock - Phase 1	$\phi H21$	High	-4	$\phi H2$ low	$\phi H2$ low		$\phi H2$		V	
Horizontal Clock - Phase 2	$\phi H22$	Low		$\phi H2$			$\phi H2$ low	$\phi H2$ low	V	10 pF, 10 M Ω
Horizontal Clock - Phase 2	$\phi H22$	High		$\phi H2$			$\phi H2$ low	$\phi H2$ low	V	

Notes:

When using Vout1, $\phi H21$ is clocked identically with $\phi H2$ while $\phi H22$ is held at a static level. When using Vout2, $\phi H21$ and $\phi H22$ are exchanged so that $\phi H22$ is identical to $\phi H2$ and $\phi H21$ is held at a static level. The static level should be the same voltage as $\phi H2$ low.

The AC and DC operating levels are for room temperature operation. Operation at other temperatures may require adjustments of these voltages. Pins shown with impedances greater than 1 MOhm are expected resistances. These pins are only verified to 1 MOhm.

$\phi V1, 2$ capacitances are accumulated gate oxide capacitance, and are an over-estimate of the capacitance.

This device is suitable for a wide range of applications requiring a variety of different operating conditions. Consult Truesense Imaging in those situations in which operating conditions meet or exceed minimum or maximum levels.



Timing

REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
ϕ H1, ϕ H2 Clock Frequency	f_H		4	5	MHz	1, 2, 3
ϕ V1, ϕ V2 Clock Frequency	f_V		100	125	kHz	1, 2, 3
Pixel Period (1 Count)	t_{pix}	200	250		ns	
ϕ H1, ϕ H2 Setup Time	$t_{\phi HS}$	500	1000		ns	
ϕ V1, ϕ V2 Clock Pulse Width	$t_{\phi V}$	4	5		μ s	2
Reset Clock Pulse Width	$t_{\phi R}$	20	60		ns	4
Readout Time	$t_{readout}$	226	286		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	219	277		μ s	7

Notes:

1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10 / 90% levels) should be limited to 5-10% of clock period. Crossover of register clocks should be between 40-60% of amplitude.
4. ϕ R should be clocked continuously
5. $t_{readout} = (1032 * t_{line})$
6. Integration time (t_{int}) is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3 * t_{\phi V}) + t_{\phi HS} + 1044 * t_{pix} + t_{pix}$



NORMAL READOUT

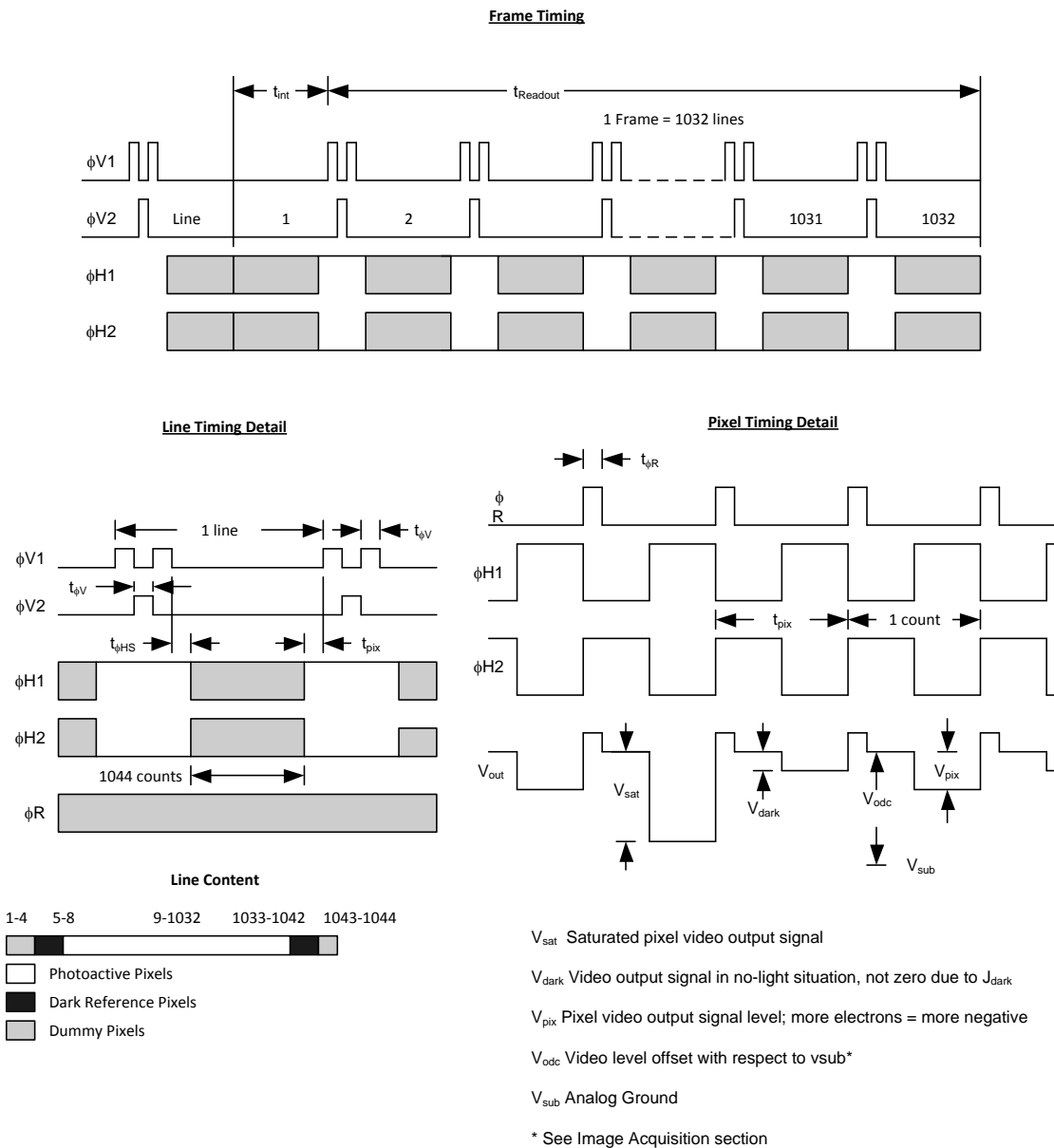


Figure 7: Timing Diagram

Notes:

1. This device is suitable for a wide range of applications requiring a variety of different timing frequencies. Therefore, only maximum and minimum values are shown above. Consult Truesense Imaging in those situations that require special consideration.



Storage and Handling

STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T _{ST}	-100	+80	°C	At Device
Operating Temperature	T _{OP}	-50	+50	°C	

ESD

1. This device contains limited protection against Electrostatic Discharge (ESD). ESD events may cause irreparable damage to a CCD image sensor either immediately or well after the ESD event occurred. Failure to protect the sensor from electrostatic discharge may affect device performance and reliability.
2. Devices should be handled in accordance with strict ESD procedures for Class 0 (<250 V per JESD22 Human Body Model test), or Class A (<200 V JESD22 Machine Model test) devices. Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
3. See Application Note *Image Sensor Handling Best Practices* for proper handling and grounding procedures. This application note also contains workplace recommendations to minimize electrostatic discharge.
4. Store devices in containers made of electro-conductive materials.

COVER GLASS CARE AND CLEANLINESS

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided.
3. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image Sensor Handling Best Practices*.

ENVIRONMENTAL EXPOSURE

1. Extremely bright light can potentially harm CCD image sensors. Do not expose to strong sunlight for long periods of time, as the color filters and/or microlenses may become discolored. In addition, long time exposures to a static high contrast scene should be avoided. Localized changes in response may occur from color filter/microlens aging. For Interline devices, refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible lighting Conditions*.
2. Exposure to temperatures exceeding maximum specified levels should be avoided for storage and operation, as device performance and reliability may be affected.
3. Avoid sudden temperature changes.
4. Exposure to excessive humidity may affect device characteristics and may alter device performance and reliability, and therefore should be avoided.
5. Avoid storage of the product in the presence of dust or corrosive agents or gases, as deterioration of lead solderability may occur. It is advised that the solderability of the device leads be assessed after an extended period of storage, over one year.

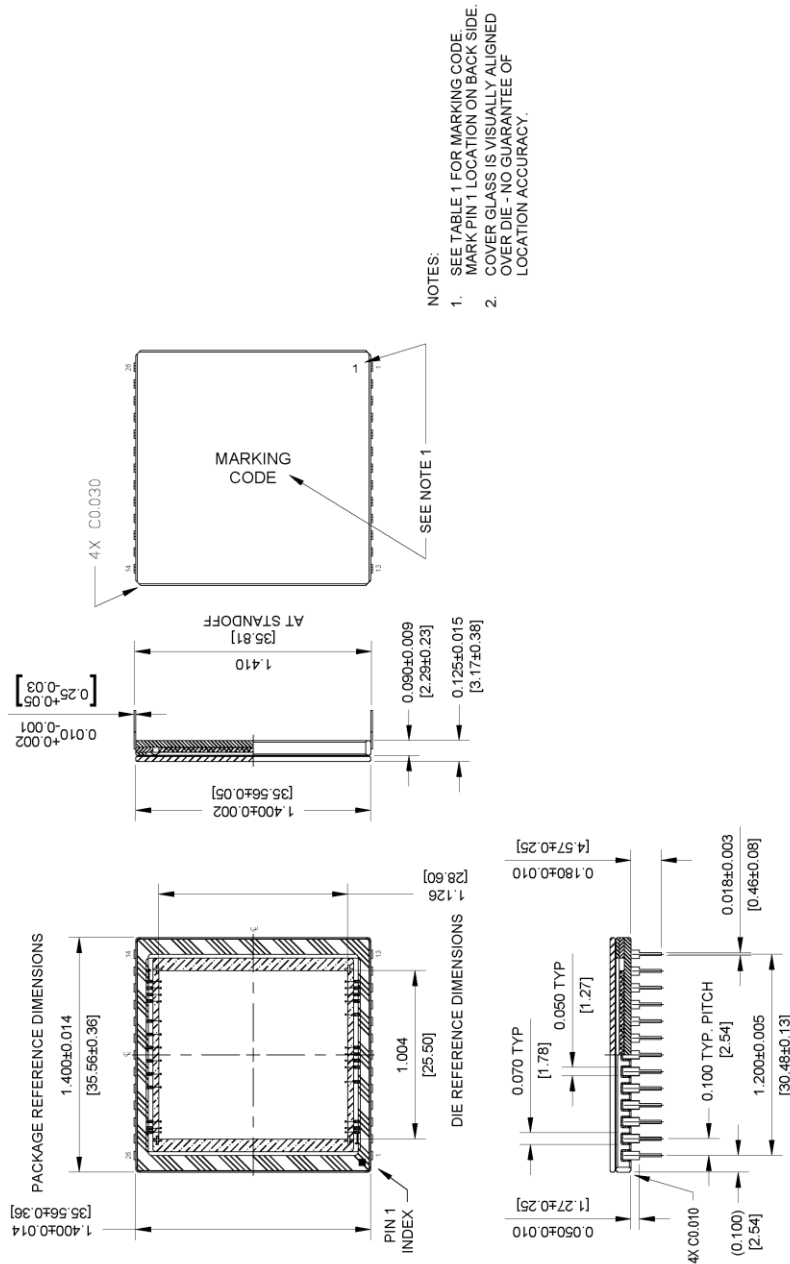
SOLDERING RECOMMENDATIONS

1. The soldering iron tip temperature is not to exceed 370 °C. Higher temperatures may alter device performance and reliability.
2. Flow soldering method is not recommended. Solder dipping can cause damage to the glass and harm the imaging capability of the device. Recommended method is by partial heating using a grounded 30 W soldering iron. Heat each pin for less than 2 seconds duration.



Mechanical Information

COMPLETED ASSEMBLY



NOTES:

1. SEE TABLE 1 FOR MARKING CODE. MARK PIN 1 LOCATION ON BACK SIDE.
2. COVER GLASS IS VISUALLY ALIGNED OVER DIE - NO GUARANTEE OF LOCATION ACCURACY.

Figure 8: Completed Assembly (1 of 2)

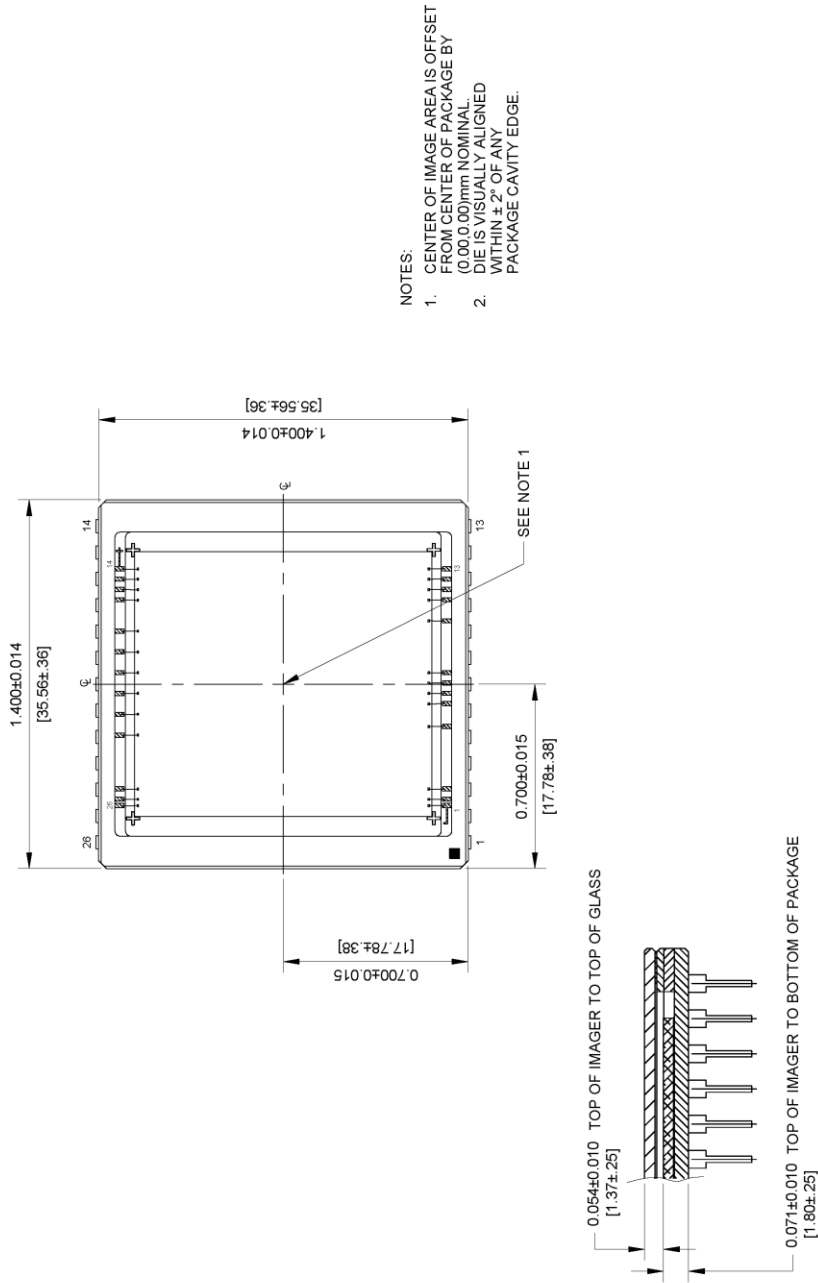


Figure 9: Completed Assembly (2 of 2)



Quality Assurance and Reliability

QUALITY AND RELIABILITY

All image sensors conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and visual inspection and electrical testing at key points of the manufacturing process, using industry standard methods. Information concerning the quality assurance and reliability testing procedures and results are available from ON Semiconductor upon request. For further information refer to Application Note *Quality and Reliability*.

REPLACEMENT

All devices are warranted against failure in accordance with the *Terms of Sale*. Devices that fail due to mechanical and electrical damage caused by the customer will not be replaced.

LIABILITY OF THE SUPPLIER

A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer. Product liability is limited to the cost of the defective item, as defined in the *Terms of Sale*.

LIABILITY OF THE CUSTOMER

Damage from mishandling (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated operating or storage limits, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

TEST DATA RETENTION

Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

MECHANICAL

The device assembly drawing is provided as a reference.

ON Semiconductor reserves the right to change any information contained herein without notice. All information furnished by ON Semiconductor is believed to be accurate.

Life Support Applications Policy

ON Semiconductor image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of ON Semiconductor.



Revision Changes

MTD/PS-0195

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> Initial Release.
2.0	<ul style="list-style-type: none"> Section 4.1, CCD Parameters Common to both Outputs: <ul style="list-style-type: none"> N_{e-sat} (Sat. Signal – Vccd) Register: <ul style="list-style-type: none"> Minimum changed from 550 to 450 ke^- Nominal changed from 650 to 500 ke^- Eliminated Appendix 1 - Available Part Numbers Added Section 6.1: Revision Changes Section 4.2 Cosmetic Grades <ul style="list-style-type: none"> Eliminate Grade 3 Remove UV grade Allow 2 columns in Grade 2 Section 5. Quality and Reliability <ul style="list-style-type: none"> Revised descriptions.
3.0	<ul style="list-style-type: none"> Updated format. Removed part numbers.
4.0	<ul style="list-style-type: none"> Pg 14 - Corrected Column and Point Defect Table Headings
5.0	<ul style="list-style-type: none"> Changed wavelength band to 400 nm to 1100 nm Changed High Sensitivity Output to 11 $\mu V/electron$ Changed Dynamic Range (Sat Sig/Dark Noise) High Sensitivity Output to 83 dB High Dynamic Range to 97 dB Changed CCD Parameters Common to Both Outputs - Dark Current to $pA/cm^2 e^-/pixel/sec$ Changed CCD Parameters Specific to Low Gain (High Dynamic Range) Output Amplifier - Dynamic Range to Min. 93, Nom. 97 Updated Defect Specification Changed Note 9 on p 11 to amplifier saturation signal
6.0	<ul style="list-style-type: none"> Pg 7 – Added Output amplifier schematic. Pg 15 – Updated DC Operating Conditions.

PS-0033

Revision Number	Description of Changes
1.0	<ul style="list-style-type: none"> Initial release with new document number, updated branding and document template Updated <i>Storage and Handling</i> and <i>Quality Assurance and Reliability</i> sections
1.1	<ul style="list-style-type: none"> Updated branding

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