PCA9512A; PCA9512B

Level shifting hot swappable I²C-bus and SMBus bus buffer

Rev. 6 — 1 March 2013 Product data sheet

1. General description

The PCA9512A/B is a hot swappable I²C-bus and SMBus buffer that allows I/O card insertion into a live backplane without corruption of the data and clock buses and includes two dedicated supply voltage pins to provide level shifting between 3.3 V and 5 V systems while maintaining the best noise margin for each voltage level. Either pin may be powered with supply voltages ranging from 2.7 V to 5.5 V with no constraints on which supply voltage is higher. Control circuitry prevents the backplane from being connected to the card until a stop bit or bus idle occurs on the backplane without bus contention on the card. When the connection is made, the PCA9512A/B provides bidirectional buffering, keeping the backplane and card capacitances isolated.

Both the PCA9512A and PCA9512B use identical silicon (PCN201012007F dated 13 Dec 2010), so the PCA9512B will be discontinued in the near future and is not recommended for new designs.

The PCA9512A/B rise time accelerator circuitry allows the use of weaker DC pull-up currents while still meeting rise time requirements. The PCA9512A/B incorporates a digital input pin that enables and disables the rise time accelerators on all four SDAn and SCLn pins.

During insertion, the PCA9512A/B SDAn and SCLn pins are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip.

The incremental offset design of the PCA9510A/11A/12A/12B/13A/14A I/O drivers allows them to be connected to another PCA9510A/11A/12A/12B/13A/14A device in series or in parallel and to the I²C compliant side of static offset bus buffers, but not to the static offset side of those bus buffers.

2. Features and benefits

- Bidirectional buffer for SDA and SCL lines increases fan-out and prevents SDA and SCL corruption during live board insertion and removal from multipoint backplane systems
- Compatible with I²C-bus Standard mode, I²C-bus Fast mode, and SMBus standards
- Built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines (0.6 V threshold) with ability to disable $\Delta V/\Delta t$ rise time accelerator through the ACC pin for lightly loaded systems, requires the bus pull-up voltage and respective supply voltage (V_{CC} or V_{CC2}) to be the same
- 5 V to 3.3 V level translation with optimum noise margin
- High-impedance SDAn and SCLn pins for V_{CC} or V_{CC2} = 0 V
- 1 V precharge on all SDAn and SCLn pins
- Supports clock stretching and multiple master arbitration and synchronization

- Operating power supply voltage range: 2.7 V to 5.5 V
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8)

3. Applications

- cPCI, VME, AdvancedTCA cards and other multipoint backplane cards that are required to be inserted or removed from an operating system

4. Feature selection

Table 1. Feature selection chart

Feature	PCA9510A	PCA9511A	PCA9512A/B	PCA9513A	PCA9514A
Idle detect	yes	yes	yes	yes	yes
High-impedance SDAn, SCLn pins for V_{CC} = 0 V	yes	yes	yes	yes	yes
Rise time accelerator circuitry on SDAn and SCLn pins	-	yes	yes	yes	yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	-	-	yes	-	-
Rise time accelerator threshold 0.8 V versus 0.6 V improves noise margin	-	-	-	yes	yes
Ready open-drain output	yes	yes	-	yes	yes
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	-	-	yes	-	-
1 V precharge on all SDAn and SCLn pins	in only	yes	yes	-	-
92 μA current source on SCLIN and SDAIN for PICMG applications	-	-	-	yes	-

5. Ordering information

Table 2. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9512AD	PA9512A	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9512BD	PA9512B			
PCA9512ADP	9512A	TSSOP8[1]	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9512BDP	9512B			

[1] Also known as MSOP8.

5.1 Ordering options

Table 3. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature range
PCA9512AD	PCA9512AD,112	SO8	standard marking * IC's tube - DSC bulk pack	2000	T_{amb} = –40 °C to +85 °C
	PCA9512AD,118	SO8	reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
PCA9512BD	PCA9512BD,118	SO8	reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
PCA9512ADP	PCA9512ADP,118	TSSOP8	reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = –40 °C to +85 °C
PCA9512BDP	PCA9512BDP,118	TSSOP8	reel 13" Q1/T1 *standard mark SMD	2500	T_{amb} = –40 °C to +85 °C

6. Block diagram

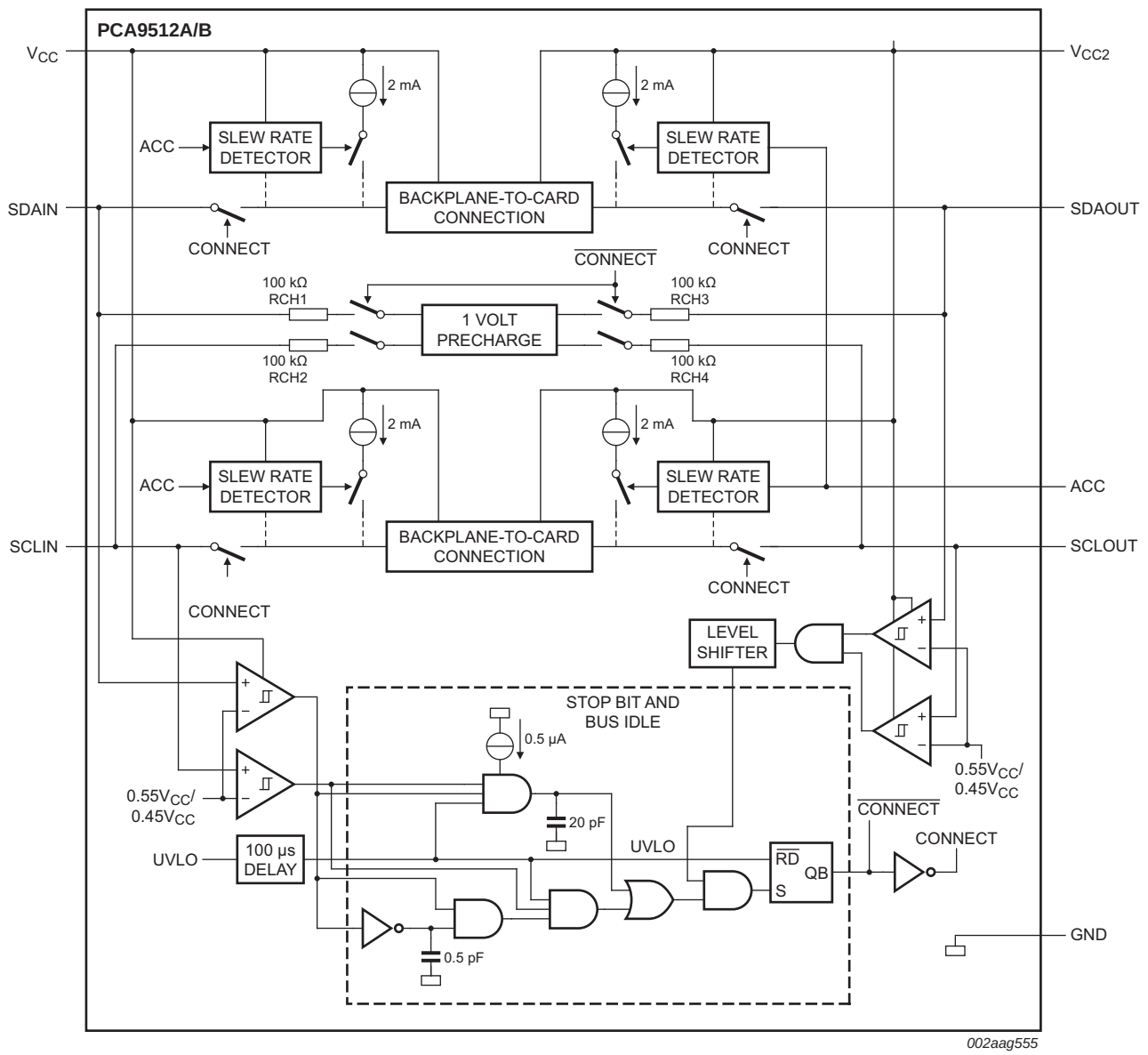


Fig 1. Block diagram of PCA9512A/B

7. Pinning information

7.1 Pinning

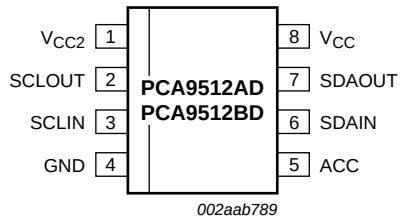


Fig 2. Pin configuration for SO8

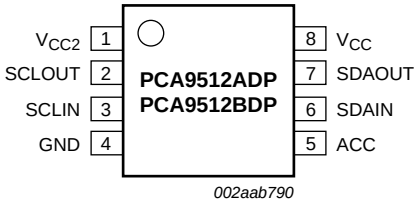


Fig 3. Pin configuration for TSSOP8

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
V_{CC2}	1	Supply voltage for devices on the card I²C-bus. Connect pull-up resistors from SDAOUT and SCLOUT to this pin.
SCLOUT	2	serial clock output to and from the SCL bus on the card
SCLIN	3	serial clock input to and from the SCL bus on the backplane
GND	4	ground supply; connect this pin to a ground plane for best results.
ACC	5	CMOS threshold digital input pin that enables and disables the rise time accelerators on all four SDAn and SCLn pins. ACC enables all accelerators when set to V_{CC2}, and turns them off when set to GND.
SDAIN	6	serial data input to and from the SDA bus on the backplane
SDAOUT	7	serial data output to and from the SDA bus on the card
V_{CC}	8	supply voltage; from the backplane, connect pull-up resistors from SDAIN and SCLIN to this pin.

8. Functional description

Refer to Figure 1 “Block diagram of PCA9512A/B”.

Both the PCA9512A and PCA9512B use identical silicon (PCN201012007F dated 13 Dec 2010), so the PCA9512B will be discontinued in the near future and is not recommended for new designs. Customers should continue using the PCA9512A or move to the PCA9512A during the next refresh if they are currently using the PCA9512B. Description of the PCA9512A operation applies equally to the PCA9512B for the remainder of this data sheet.

8.1 Start-up

When the PCA9512A is powered up, either V_{CC} or V_{CC2} may rise first, within a short time of each other and either may be more positive or they may be equal, however the PCA9512A will not leave the undervoltage lockout or initialization state until both V_{CC} and V_{CC2} have gone above 2.5 V. If either V_{CC} or V_{CC2} drops below 2.0 V it will return to the undervoltage lockout state.

In the undervoltage lockout state the connection circuitry is disabled, the rise time accelerators are disabled, and the precharge circuitry is also disabled. After both V_{CC} and V_{CC2} are valid, independent of which is higher, the PCA9512A/B enters the initialization state; during this state the 1 V precharge circuitry is activated and pulls up the SDAn and SCLn pins to 1 V through individual 100 kΩ nominal resistors. At the end of the initialization state the 'Stop bit and bus idle' detect circuit is enabled. When all the SDAn and SCLn pins have been HIGH for the bus idle time or when all pins are HIGH and a STOP condition is seen on the SDAIN and SCLIN pins, the connect circuitry is activated, connecting SDAIN to SDAOUT and SCLIN to SCLOUT. The 1 V precharge circuitry is disabled when the connection is made, unless the ACC pin is LOW; the rise time accelerators are enabled at this time also.

8.2 Connect circuitry

Once the connection circuitry is activated, the behavior of SDAIN and SDAOUT as well as SCLIN and SCLOUT become identical, with each acting as a bidirectional buffer that isolates the input bus capacitance from the output bus capacitance while communicating. If $V_{CC} \neq V_{CC2}$, then a level shifting function is performed between input and output. A LOW forced on either SDAIN or SDAOUT will cause the other pin to be driven to a LOW by the PCA9512A/B. The same is also true for the SCLn pins. Noise between $0.7V_{CC}$ and V_{CC} on the SDAIN and SCLIN pins, and $0.7V_{CC2}$ and V_{CC2} on the SDAOUT and SCLOUT pins is generally ignored because a falling edge is only recognized when it falls below $0.7V_{CC}$ for SDAIN and SCLIN (or $0.7V_{CC2}$ for SDAOUT and SCLOUT pins) with a slew rate of at least 1.25 V/μs. When a falling edge is seen on one pin, the other pin in the pair turns on a pull-down driver that is referenced to a small voltage above the falling pin. The driver will pull the pin down at a slew rate determined by the driver and the load. The first falling pin may have a fast or slow slew rate; if it is faster than the pull-down slew rate, then the initial pull-down rate will continue until it is LOW. If the first falling pin has a slow slew rate, then the second pin will be pulled down at its initial slew rate only until it is just above the first pin voltage then they will both continue down at the slew rate of the first.

Once both sides are LOW they will remain LOW until all the external drivers have stopped driving LOWs. If both sides are being driven LOW to the same (or nearly the same) value by external drivers, which is the case for clock stretching and is typically the case for acknowledge, and one side external driver stops driving, that pin will rise and rise above the nominal offset voltage until the internal driver catches up and pulls it back down to the offset voltage. This bounce is worst for low capacitances and low resistances, and may become excessive. When the last external driver stops driving a LOW, that pin will bounce up and settle out just above the other pin as both rise together with a slew rate determined by the internal slew rate control and the RC time constant. As long as the slew rate is at least 1.25 V/μs, when the pin voltage exceeds 0.6 V, the rise time accelerator circuits are turned on and the pull-down driver is turned off. If the ACC pin is LOW, the rise time accelerator circuits will be disabled, but the pull-down driver will still turn off.

8.3 Maximum number of devices in series

Each buffer adds about 0.1 V dynamic level offset at 25 °C with the offset larger at higher temperatures. Maximum offset (V_{offset}) is 0.150 V with a 10 kΩ pull-up resistor. The LOW level at the signal origination end (master) is dependent upon the load and the only specification point is the I²C-bus specification of 3 mA will produce $V_{OL} < 0.4$ V, although if lightly loaded the V_{OL} may be ~0.1 V. Assuming $V_{OL} = 0.1$ V and $V_{offset} = 0.1$ V, the level after four buffers would be 0.5 V, which is only about 0.1 V below the threshold of the

rising edge accelerator (about 0.6 V). With great care a system with four buffers may work, but as the V_{OL} moves up from 0.1 V, noise or bounces on the line will result in firing the rising edge accelerator thus introducing false clock edges. Generally it is recommended to limit the number of buffers in series to two, and to keep the load light to minimize the offset.

The PCA9510A (rise time accelerator is permanently disabled) and the PCA9512A (rise time accelerator can be turned off) are a little different with the rise time accelerator turned off because the rise time accelerator will not pull the node up, but the same logic that turns on the accelerator turns the pull-down off. If the V_{IL} is above ~0.6 V and a rising edge is detected, the pull-down will turn off and will not turn back on until a falling edge is detected.

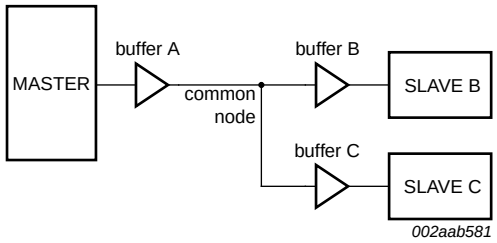


Fig 4. System with 3 buffers connected to common node

Consider a system with three buffers connected to a common node and communication between the Master and Slave B that are connected at either end of buffer A and buffer B in series as shown in Figure 4. Consider if the V_{OL} at the input of buffer A is 0.3 V and the V_{OL} of Slave B (when acknowledging) is 0.4 V with the direction changing from Master to Slave B and then from Slave B to Master. Before the direction change you would observe V_{IL} at the input of buffer A of 0.3 V and its output, the common node, is ~0.4 V. The output of buffer B and buffer C would be ~0.5 V, but Slave B is driving 0.4 V, so the voltage at Slave B is 0.4 V. The output of buffer C is ~0.5 V. When the Master pull-down turns off, the input of buffer A rises and so does its output, the common node, because it is the only part driving the node. The common node will rise to 0.5 V before buffer B's output turns on, if the pull-up is strong the node may bounce. If the bounce goes above the threshold for the rising edge accelerator ~0.6 V the accelerators on both buffer A and buffer C will fire contending with the output of buffer B. The node on the input of buffer A will go HIGH as will the input node of buffer C. After the common node voltage is stable for a while the rising edge accelerators will turn off and the common node will return to ~0.5 V because the buffer B is still on. The voltage at both the Master and Slave C nodes would then fall to ~0.6 V until Slave B turned off. This would not cause a failure on the data line as long as the return to 0.5 V on the common node (~0.6 V at the Master and Slave C) occurred before the data setup time. If this were the SCL line, the parts on buffer A and buffer C would see a false clock rather than a stretched clock, which would cause a system error.

8.4 Propagation delays

The delay for a rising edge is determined by the combined pull-up current from the bus resistors and the rise time accelerator current source and the effective capacitance on the lines. If the pull-up currents are the same, any difference in rise time is directly proportional to the difference in capacitance between the two sides. The t_{PLH} may be negative if the output capacitance is less than the input capacitance and would be positive if the output capacitance is larger than the input capacitance, when the currents are the same.

The t_{PHL} can never be negative because the output does not start to fall until the input is below $0.7V_{CC}$ (or $0.7V_{CC2}$ for SDAOUT and SCLOUT), and the output turn-ON has a non-zero delay, and the output has a limited maximum slew rate, and even if the input slew rate is slow enough that the output catches up it will still lag the falling voltage of the input by the offset voltage. The maximum t_{PHL} occurs when the input is driven LOW with zero delay and the output is still limited by its turn-on delay and the falling edge slew rate. The output falling edge slew rate is a function of the internal maximum slew rate which is a function of temperature, V_{CC} or V_{CC2} and process, as well as the load current and the load capacitance.

8.5 Rise time accelerators

During positive bus transactions, a 2 mA current source is switched on to quickly slew the SDA and SCL lines HIGH once the input level of 0.6 V for the PCA9512A is exceeded. The rising edge rate should be at least 1.25 V/µs to guarantee turn on of the accelerators. The built-in $\Delta V/\Delta t$ rise time accelerators on all SDA and SCL lines requires the bus pull-up voltage and respective supply voltage (V_{CC} or V_{CC2}) to be the same. The built-in $\Delta V/\Delta t$ rise time accelerators can be disabled through the ACC pin for lightly loaded systems.

8.6 ACC boost current enable

Users having lightly loaded systems may wish to disable the rise time accelerators. Driving this pin to ground turns off the rise time accelerators on all four SDAn and SCLn pins. Driving this pin to the V_{CC2} voltage enables normal operation of the rise time accelerators.

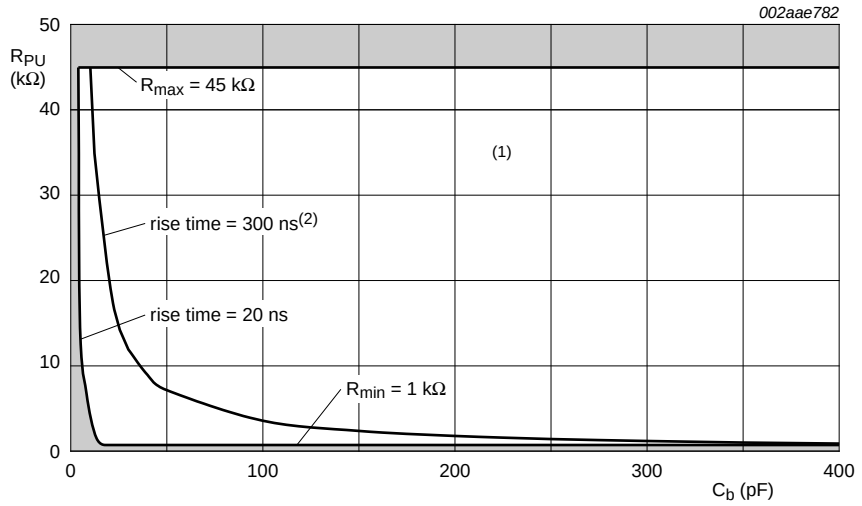
8.7 Resistor pull-up value selection

The system pull-up resistors must be strong enough to provide a positive slew rate of 1.25 V/µs on the SDAn and SCLn pins, in order to activate the boost pull-up currents during rising edges. Choose maximum resistor value using the formula given in Equation 1:

$$R_{PU} \leq 800 \times 10^{3}\left(\frac{V_{CC(min)} - 0.6}{C}\right) \quad (1)$$

where R_{PU} is the pull-up resistor value in Ω, $V_{CC(min)}$ is the minimum V_{CC} voltage in volts, and C is the equivalent bus capacitance in picofarads.

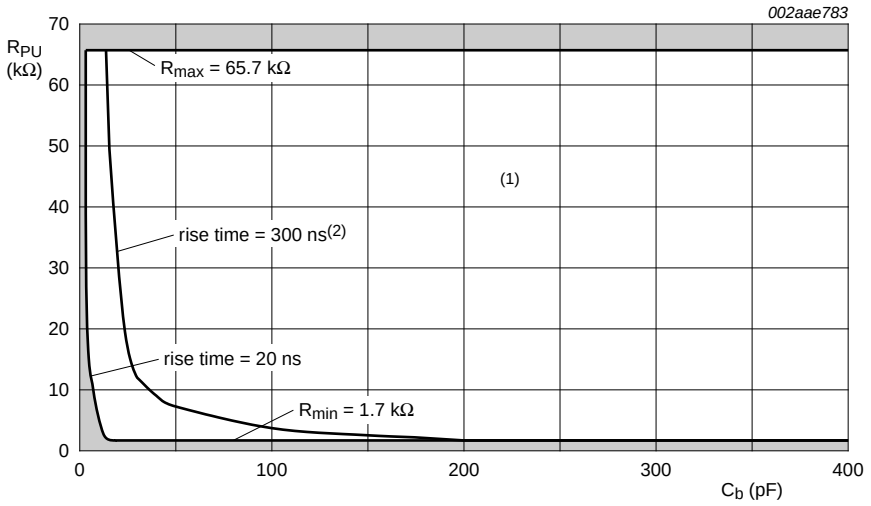
In addition, regardless of the bus capacitance, always choose $R_{PU} \leq 65.7\ k\Omega$ for $V_{CC} = 5.5$ V maximum, $R_{PU} \leq 45\ k\Omega$ for $V_{CC} = 3.6$ V maximum. The start-up circuitry requires logic HIGH voltages on SDAOUT and SCLOUT to connect the backplane to the card, and these pull-up values are needed to overcome the precharge voltage. See the curves in Figure 5 and Figure 6 for guidance in resistor pull-up selection.



(1) Unshaded area indicates recommended pull-up, for rise time < 300 ns, with rise time accelerator turned on.

(2) Rise time accelerator off.

Fig 5. Bus requirements for 3.3 V systems



(1) Unshaded area indicates recommended pull-up, for rise time < 300 ns, with rise time accelerator turned on.

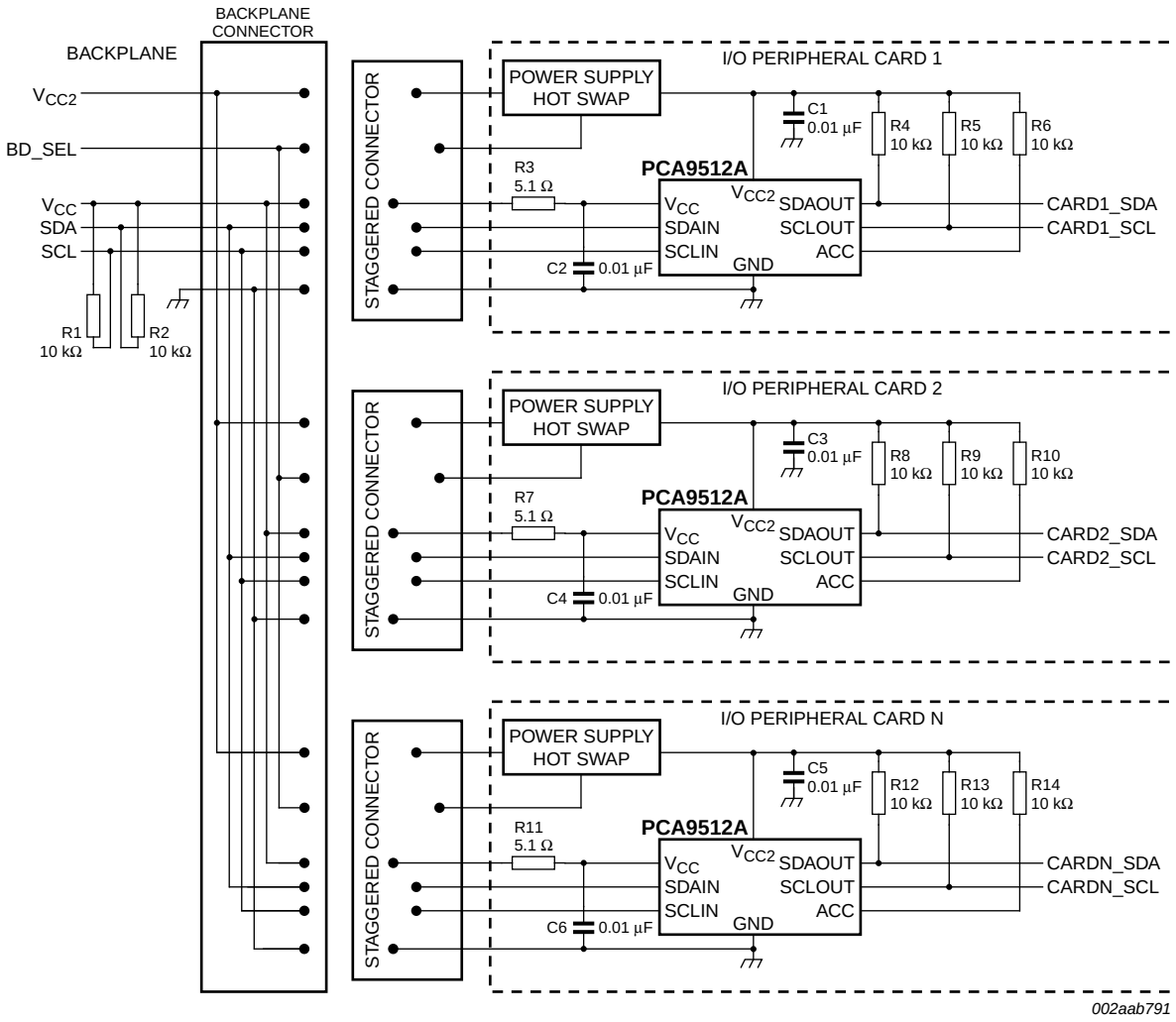
(2) Rise time accelerator off.

Fig 6. Bus requirements for 5 V systems

8.8 Hot swapping and capacitance buffering application

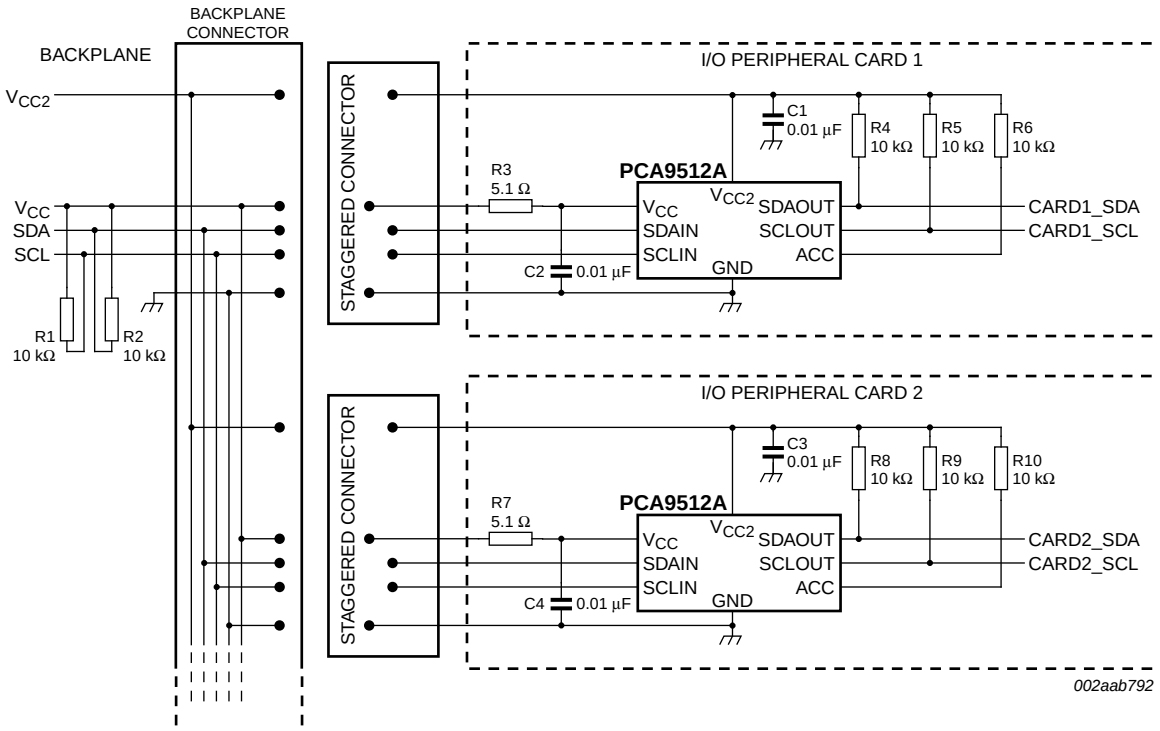
Figure 7 through Figure 9 illustrate the usage of the PCA9512A in applications that take advantage of both its hot swapping and capacitance buffering features. In all of these applications, note that if the I/O cards were plugged directly into the backplane, all of the backplane and card capacitances would add directly together, making rise time and fall time requirements difficult to meet. Placing a bus buffer on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the PCA9512A drives the capacitance of everything on the card and the backplane must drive only the capacitance of the bus buffer, which is less than 10 pF, the connector, trace, and all additional cards on the backplane.

See *Application Note AN10160, 'Hot Swap Bus Buffer'* for more information on applications and technical assistance.



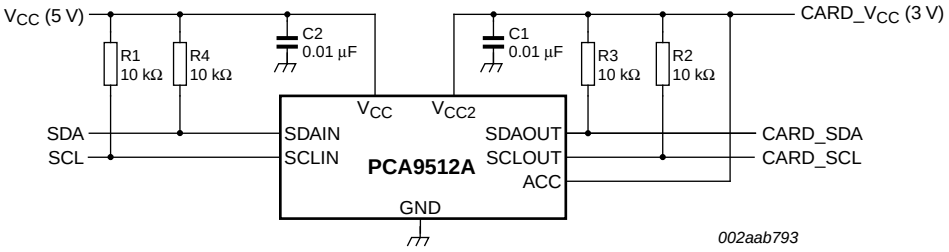
Remark: Application assumes bus capacitance within 'proper operation' region of Figure 5 and Figure 6.

Fig 7. Hot swapping multiple I/O cards into a backplane using the PCA9512A in a cPCI, VME, and AdvancedTCA system



Remark: Application assumes bus capacitance within 'proper operation' region of Figure 5 and Figure 6.

Fig 8. Hot swapping multiple I/O cards into a backplane using the PCA9512A with a custom connector



Remark: Application assumes bus capacitance within 'proper operation' region of Figure 5 and Figure 6.

Fig 9. 5 V to 3.3 V level translator and bus buffer

8.9 Voltage level translator discussion

8.9.1 Summary

There are two popular configurations for the interface of low voltage logic (i.e., core processor with 3.3 V supply) to standard bus levels (i.e., I²C-bus with 5 V supply). A single FET transistor and two additional resistors may be used effectively, or an application-specific IC part requiring no external components and no additional resistors.

The FET solution becomes problematic as the low voltage logic levels trend downwards. The FET solution will stop working completely when the FET specification is no longer matched to the LOW level logic supply voltage requirements.

The dominant advantage of the FET solution is cost, but the IC part provides additional advantages to the design, which increases reliability to the end user.

8.9.2 Why do level translation?

Advances in processing technology require lower supply voltages, due to reduced clearances in the fabrication technology. Lower supply voltages drive down signal swings, or require that on die high voltage I/O sections are added, creating larger die area, or greater I/O pin count. Existing standards for interoperability of equipment connected by cables or between subsystems require higher voltage signal swings (typically 5 V).

An external voltage level translator solves these problems, but requires additional parts.

8.10 Limitations of the FET voltage level translator

8.10.1 V_{GSth}, gate-source threshold voltage

When the VA input is logic LOW, the FET is turned on, pulling VB output LOW. This can only occur when the threshold voltage of the FET is less than the VA supply voltage minus the maximum level of the VA signal, VAIL. Using CMOS logic thresholds of 0.3 and 0.7 times the supply, and a 1.1 V VA gives a worst-case of just 330 mV, much less than V_{GSth} of the popular 2N7002 FET.

V_{GSth}; I_D = 250 μA; V_{DS} = V_{GS}; 1.1 V (min.)/1.6 V (typ.)/2.1 V (max.)

Additionally, the FET threshold voltage is specified in the linear region of the FET, with weak conduction. Ideally the FET should have very low ON-resistance. For the 2N7002, this is specified at 5 V V_{GS} (not the 1 V available in this application). Note that the ON-resistance decreases rapidly as V_{GS} is increased beyond the V_{GSth} specification. Unintended operation in the linear region further compromises logic level noise immunity.

8.10.2 FET body diode voltage

The FET is required to conduct in both directions, as the I2C-bus is bidirectional. When the VB input is logic LOW, the body diode of the FET conducts first, pulling the FET source LOW along with the FET drain, until the FET conducts. During this transition the forward voltage drop of the body diode reduces the available FET gain to source bias. The body diode is specified:

V_{SD}, source-drain voltage; I_S = 115 mA; V_{GS} = 0 V; 0.47 V (min.)/0.75 V (typ.)/1.1 V (max.)

Conduction of the FET body diode impacts both the delay time and logic transition speed.

8.11 Additional system compromises

- Additional parts
- Additional assembly cost
- Reduced system reliability due to complexity
- Reduced logic level noise margin (immunity)
- Sensitivity to ground offsets between sub-systems (cable links, for example)
- Increased loading on the low voltage side (must carry the high voltage side sink current)
- ESD robustness

9. Application design-in information

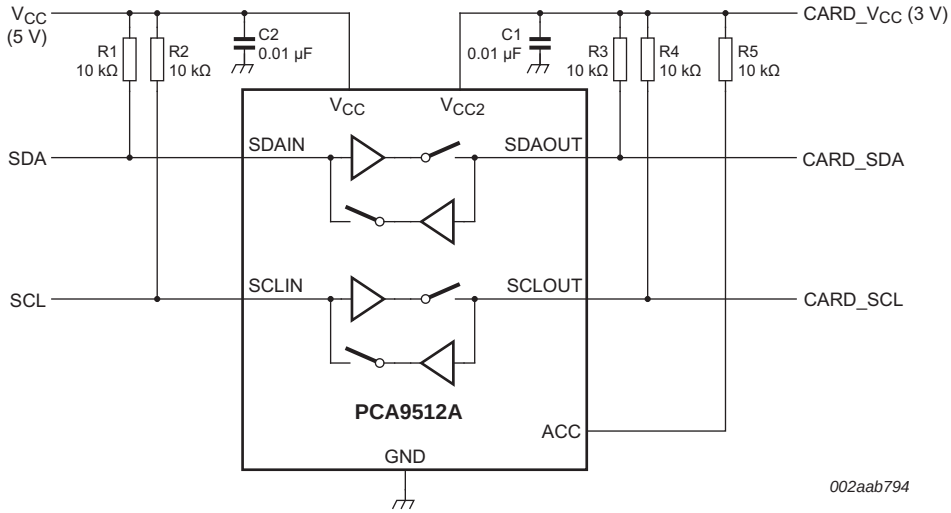


Fig 10. Typical application

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
V_{CC2}	supply voltage 2		[1]	−0.5	+7	V
V_n	voltage on any other pin			−0.5	+7	V
I_I	input current		[2]	-	±20	mA
$I_{I/O}$	input/output current		[3]	-	±50	mA
T_{oper}	operating temperature			−40	+85	°C
T_{stg}	storage temperature			−65	+125	°C
T_{sp}	solder point temperature	10 s maximum		-	300	°C
$T_{j(max)}$	maximum junction temperature			-	125	°C

[1] Card side supply voltage.

[2] Maximum current for inputs.

[3] Maximum current for I/O pins.

11. Characteristics

Table 6. Characteristics

V_{CC} = 2.7 V to 5.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Power supply							
V_{CC}	supply voltage		[1]	2.7	-	5.5	V
V_{CC2}	supply voltage 2		[1]	2.7	-	5.5	V
I_{CC}	supply current	V_{CC} = 5.5 V; V_{SDAIN} = V_{SCLIN} = 0 V		-	1.8	3.6	mA
I_{CC2}	supply current 2	V_{CC} = 5.5 V; V_{SDAOUT} = V_{SCLOUT} = 0 V		-	1.7	2.9	mA
Start-up circuitry							
V_{pch}	precharge voltage	SDA, SCL floating	[1]	0.8	1.1	1.2	V
t_{en}	enable time	on power-up	[3]	-	180	-	µs
t_{idle}	idle time		[1][4]	50	140	250	µs
Rise time accelerators							
$I_{trt(pu)}$	transient boosted pull-up current	positive transition on SDA, SCL; V_{ACC} = 0.7 × V_{CC2}; V_{CC} = 2.7 V; slew rate = 1.25 V/µs	[5][6]	1	2	-	mA
$V_{th(dis)(ACC)}$	disable threshold voltage on pin ACC			0.3V_{CC2}	0.5V_{CC2}	-	V
$V_{th(en)(ACC)}$	enable threshold voltage on pin ACC			-	0.5V_{CC2}	0.7V_{CC2}	V
$I_{I(ACC)}$	input current on pin ACC			−1	±0.1	+1	µA
$t_{PD(on/off)(ACC)}$	on/off propagation delay on pin ACC			-	5	-	ns

Table 6. Characteristics *...continued*

V_{CC} = 2.7 V to 5.5 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input-output connection							
V_{offset}	offset voltage	10 kΩ to V_{CC} on SDA, SCL; V_{CC} = 3.3 V; V_{CC2} = 3.3 V; V_I = 0.2 V	[1][7]	0	115	175	mV
C_i	input capacitance	digital; guaranteed by design, not subject to test		-	-	10	pF
V_{OL}	LOW-level output voltage	V_I = 0 V; SDAn, SCLn pins; I_{sink} = 3 mA; V_{CC} = 2.7 V; V_{CC2} = 2.7 V	[1]	0	0.3	0.4	V
I_{LI}	input leakage current	SDAn, SCLn pins; V_{CC} = 5.5 V; V_{CC2} = 5.5 V		−1	-	+1	µA
System characteristics							
f_{SCL}	SCL clock frequency		[8]	0	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition		[8]	1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		[8]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		[8]	0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition		[8]	0.6	-	-	µs
$t_{HD;DAT}$	data hold time		[8]	300	-	-	ns
$t_{SU;DAT}$	data set-up time		[8]	100	-	-	ns
t_{LOW}	LOW period of the SCL clock		[8]	1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		[8]	0.6	-	-	µs
t_f	fall time of both SDA and SCL signals		[8][9]	20 + 0.1 × C_b	-	300	ns
t_r	rise time of both SDA and SCL signals		[8][9]	20 + 0.1 × C_b	-	300	ns

[1] This specification applies over the full operating temperature range.

[2] Card side supply voltage.

[3] The enable time is from power-up of V_{CC} and $V_{CC2} \geq 2.7$ V to when idle or stop time begins.

[4] Idle time is from when SDAn and SCLn are HIGH after enable time has been met.

[5] $I_{trt(pu)}$ varies with temperature and V_{CC} voltage, as shown in Section 11.1 “Typical performance characteristics”.

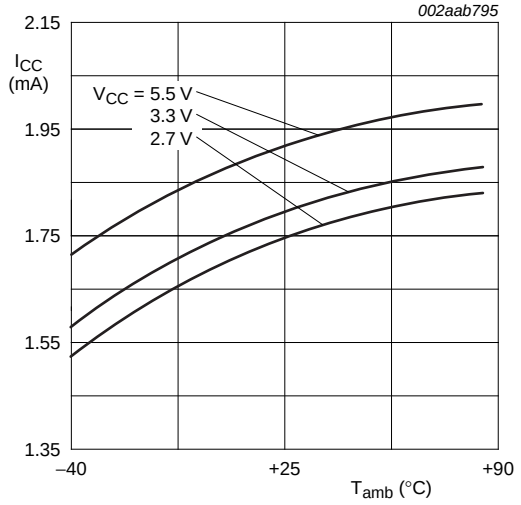
[6] Input pull-up voltage should not exceed power supply voltage in operating mode because the rise time accelerator will clamp the voltage to the positive supply rail.

[7] The connection circuitry always regulates its output to a higher voltage than its input. The magnitude of this offset voltage as a function of the pull-up resistor and V_{CC} voltage is shown in Section 11.1 “Typical performance characteristics”.

[8] Guaranteed by design, not production tested.

[9] C_b = total capacitance of one bus line in pF.

11.1 Typical performance characteristics



I_{CC2} (pin 1) typical current averages 0.1 mA less than I_{CC} on pin 8.

Fig 11. I_{CC} versus temperature

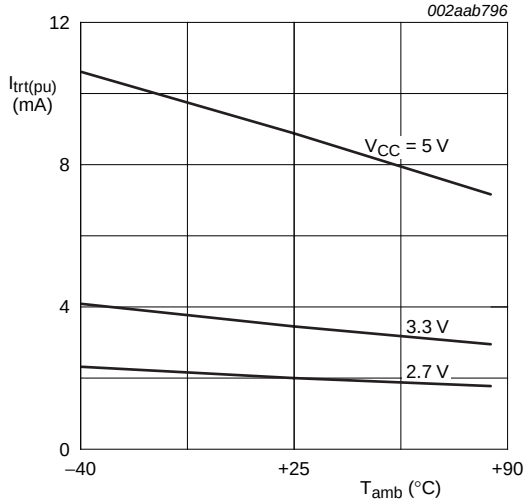
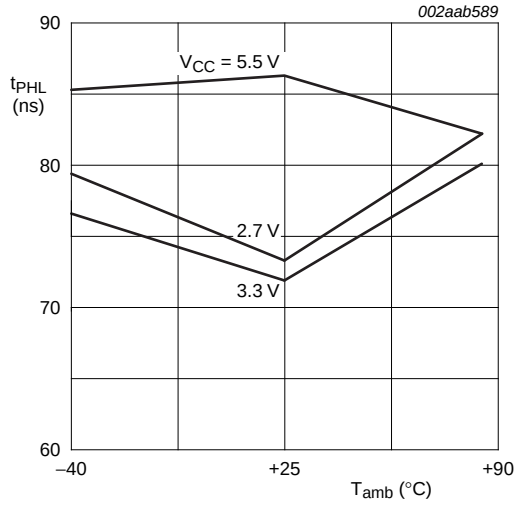
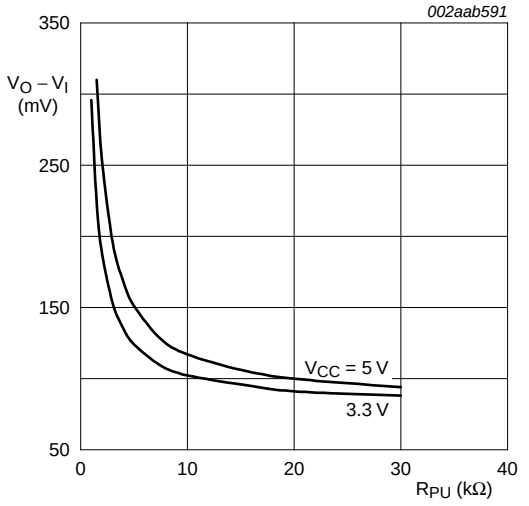


Fig 12. $I_{trt(pu)}$ versus temperature



$C_i = C_o > 100$ pF; $R_{PU(in)} = R_{PU(out)} = 10$ kΩ

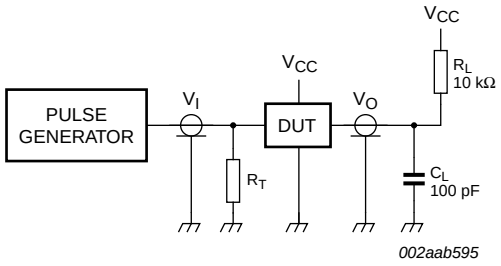
Fig 13. Input/output t_{PHL} versus temperature



V_{CC} = 3.3 V or 5.5 V

Fig 14. Connection circuitry $V_O - V_I$

12. Test information



R_L = load resistor

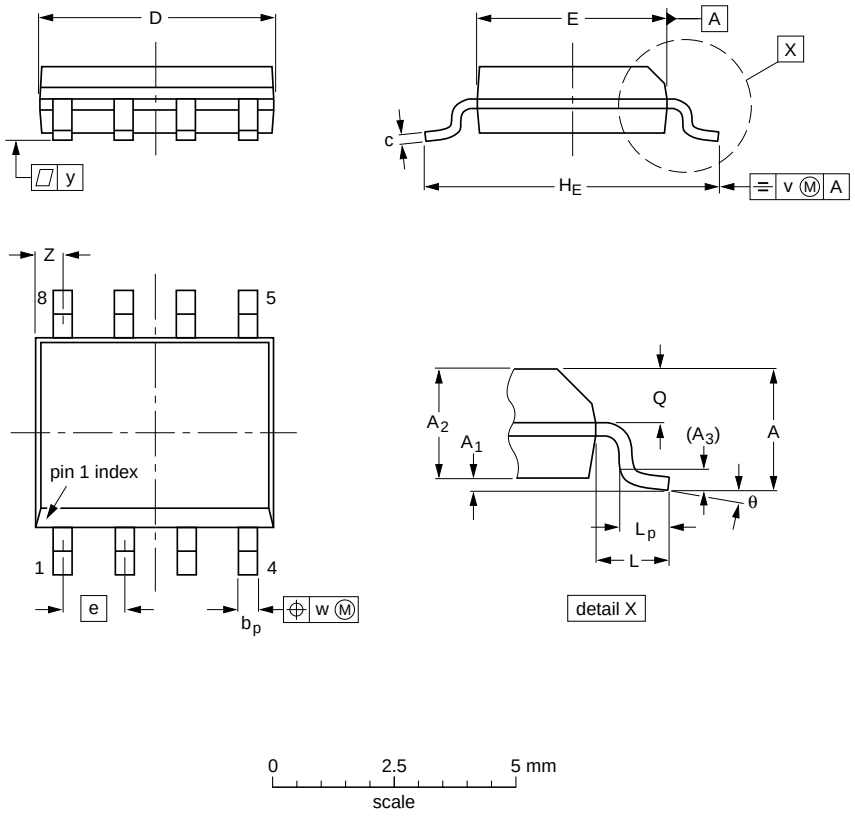
C_L = load capacitance includes jig and probe capacitance

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator

Fig 15. Test circuitry for switching times

13. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

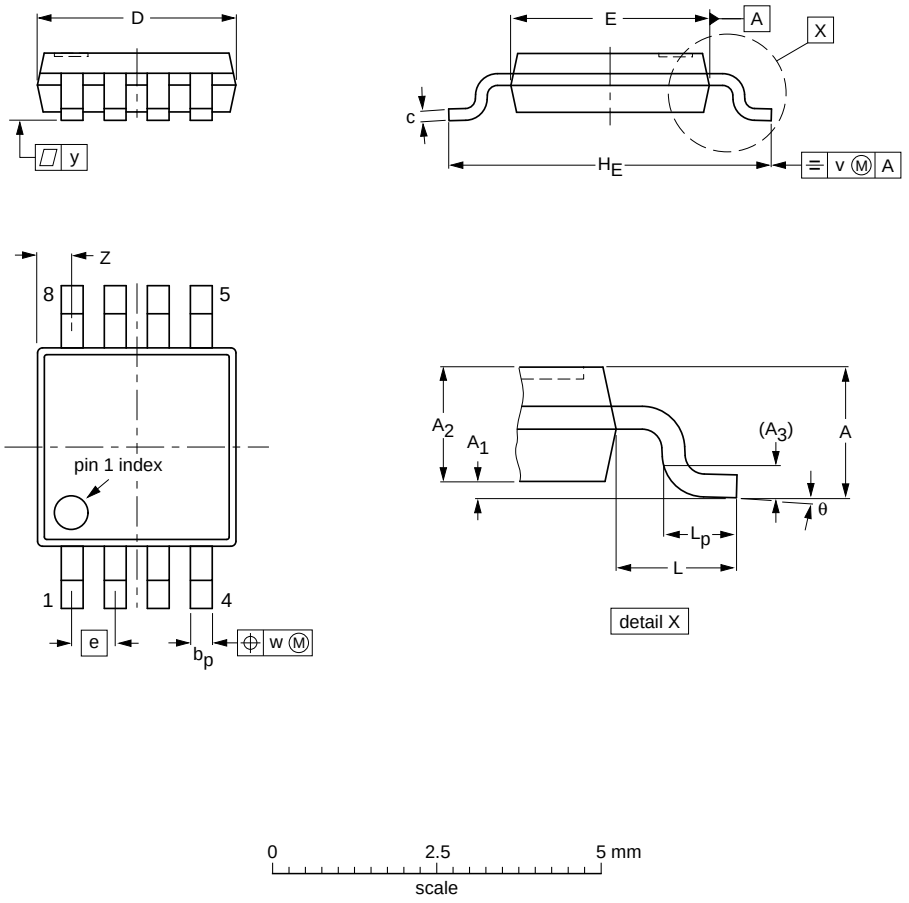
Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				~~99-12-27~~ 03-02-18

Fig 16. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 17. Package outline SOT505-1 (TSSOP8)

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020D)

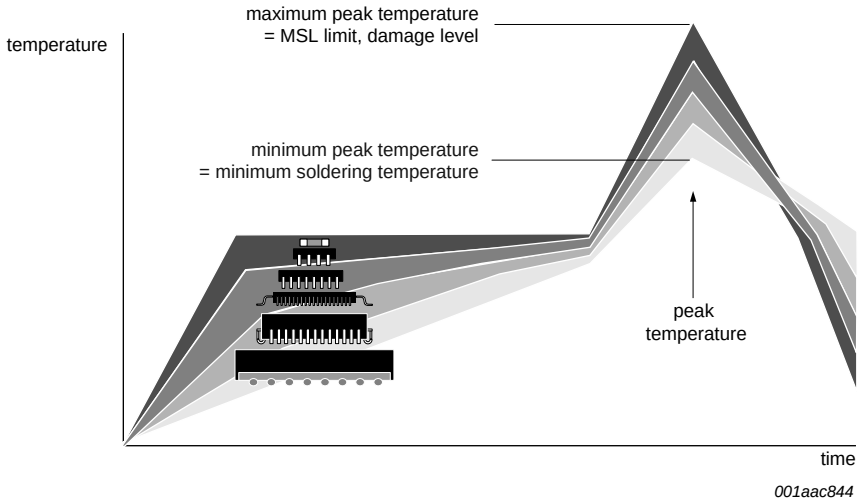
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.



MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Soldering: PCB footprints

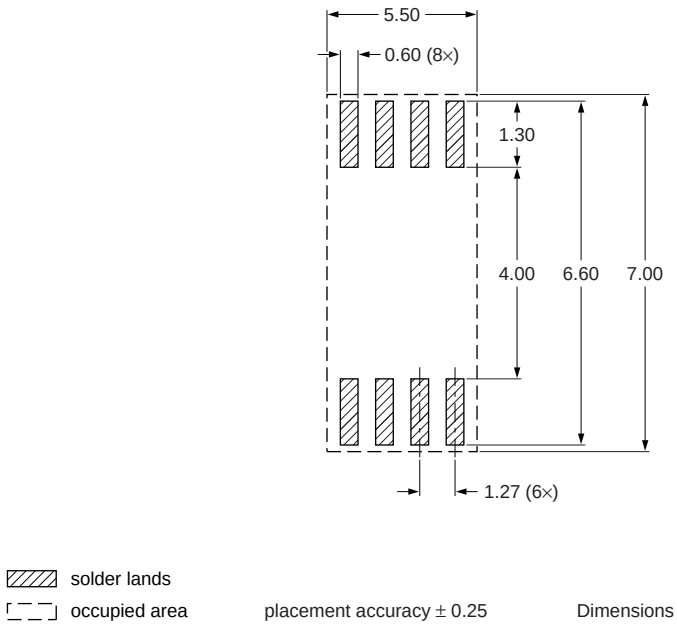


Fig 19. PCB footprint for SOT96-1 (SO8); reflow soldering

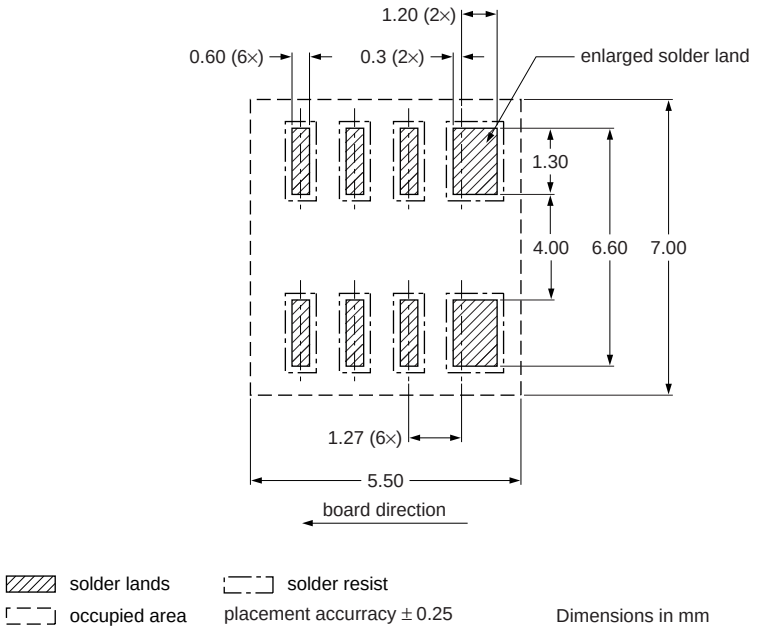


Fig 20. PCB footprint for SOT96-1 (SO8); wave soldering

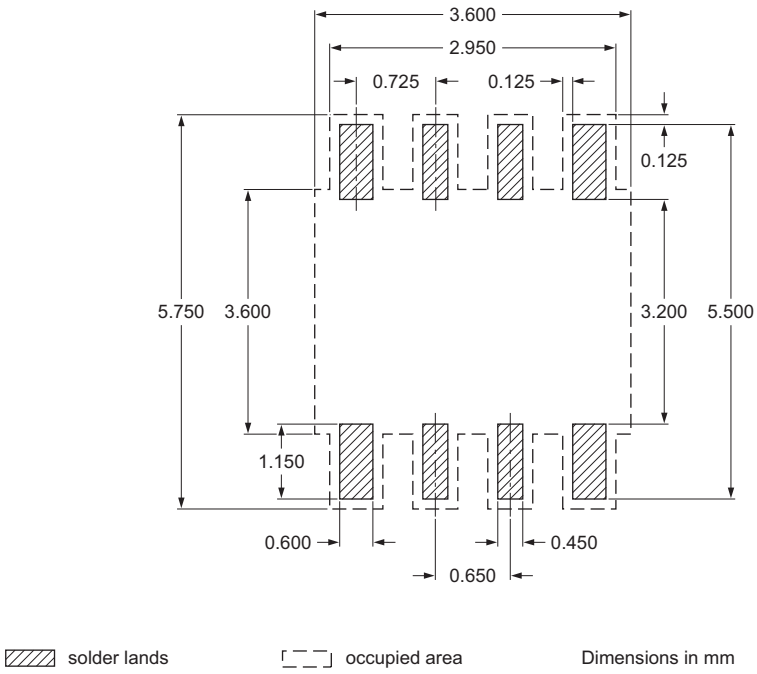


Fig 21. PCB footprint for SOT505-1 (TSSOP8); reflow soldering

16. Abbreviations

Table 9. Abbreviations

Acronym	Description
AdvancedTCA	Advanced Telecommunications Computing Architecture
AVL	Approved Vendor List
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
cPCI	compact Peripheral Component Interface
ESD	Electrostatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
I^2C-bus	Inter-Integrated Circuit bus
IC	Integrated Circuit
PCI	Peripheral Component Interface
PICMG	PCI Industrial Computer Manufacturers Group
SMBus	System Management Bus
VME	VERSAModule Eurocard

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9512A_PCA9512B v.6	20130301	Product data sheet	-	PCA9512A_PCA9512B v.5
Modifications:	• Section 1 “General description”: second paragraph re-written • Section 2 “Features and benefits”: 11th bullet item: deleted “200 V MM per JESD22-A115” • Added Section 5.1 “Ordering options” • Figure 1 “Block diagram of PCA9512A/B”: added “LEVEL SHIFTER” block • Section 8 “Functional description”: added (new) second paragraph • Figure 10 “Typical application”: changed type number from “PCA9512A/B” to “PCA9512A” • Added Section 8.9 “Voltage level translator discussion” • Added Section 8.10 “Limitations of the FET voltage level translator” • Added Section 8.11 “Additional system compromises” • Added Section 15 “Soldering: PCB footprints”			
PCA9512A_PCA9512B v.5	20110105	Product data sheet	-	PCA9512A v.4
PCA9512A v.4	20090819	Product data sheet	-	PCA9512A v.3
PCA9512A v.3	20090720	Product data sheet	-	PCA9512A v.2
PCA9512A v.2	20090528	Product data sheet	-	PCA9512A v.1
PCA9512A v.1	20051007	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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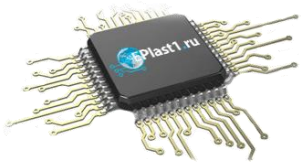

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