Zerø-Drift PROGRAMMABLE GAIN AMPLIFIER with MUX

FEATURES

- Rail-to-Rail Input/Output
- Offset: 25μV (typ), 100μV (max)
- Zerø Drift: 0.35μV/°C (typ), 1.2μV/°C (max)
- Low Noise: 12nV/√Hz
- Input Offset Current: ±5nA max (+25°C)
- Gain Error: 0.1% max (G ≤ 32), 0.3% max (G > 32)
- Binary Gains: 1, 2, 4, 8, 16, 32, 64, 128 (PGA112, PGA116)
- Scope Gains: 1, 2, 5, 10, 20, 50, 100, 200 (PGA113, PGA117)
- Gain Switching Time: 200ns
- Two Channel MUX: PGA112, PGA113
  10 Channel MUX: PGA116, PGA117
- Four Internal Calibration Channels
- Amplifier Optimized for Driving CDAC ADCs
- Output Swing: 50mV to Supply Rails
- AV_{DD} and DV_{DD} for Mixed Voltage Systems
- I_Q = 1.1mA (typ)
- Software/Hardware Shutdown: I_Q ≤ 4μA (typ)
- Temperature Range: –40°C to +125°C
- SPI™ Interface (10MHz) with Daisy-Chain Capability

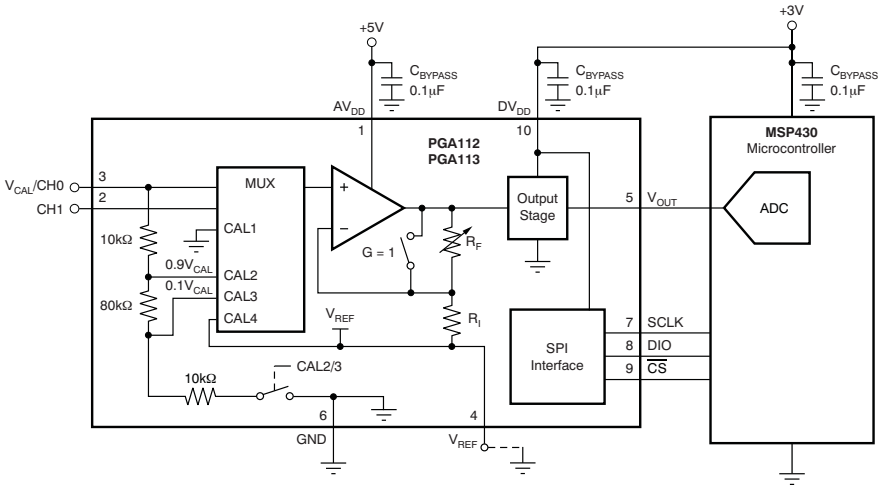
APPLICATIONS

- Remote e-Meter Reading
- Automatic Gain Control
- Portable Data Acquisition
- PC-Based Signal Acquisition Systems
- Test and Measurement
- Programmable Logic Controllers
- Battery-Powered Instruments
- Handheld Test Equipment

DESCRIPTION

The PGA112 and PGA113 (binary/scope gains) offer two analog inputs, a three-pin SPI interface, and software shutdown in an MSOP-10 package. The PGA116 and PGA117 (binary/scope gains) offer 10 analog inputs, a four-pin SPI interface with daisy-chain capability, and hardware and software shutdown in a TSSOP-20 package.

All versions provide internal calibration channels for system-level calibration. The channels are tied to GND, $0.9V_{CAL}$, $0.1V_{CAL}$, and V_{REF}, respectively. V_{CAL}, an external voltage connected to Channel 0, is used as the system calibration reference. Binary gains are: 1, 2, 4, 8, 16, 32, 64, and 128; scope gains are: 1, 2, 5, 10, 20, 50, 100, and 200.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE AND MODEL COMPARISON

DEVICE	# OF MUX INPUTS	GAINS (Eight Each)	SPI DAISY-CHAIN	SHUTDOWN		PACKAGE
				HARDWARE	SOFTWARE	
PGA112	Two	Binary	No	No	✓	MSOP-10
PGA113	Two	Scope	No	No	✓	MSOP-10
PGA116	10	Binary	✓	✓	✓	TSSOP-20
PGA117	10	Scope	✓	✓	✓	TSSOP-20

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION (Gains/Channels)	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
PGA112	Binary(2)/2 Channels	MSOP-10	DGS	P112
PGA113	Scope(3)/2 Channels	MSOP-10	DGS	P113
PGA116	Binary(2)/10 Channels	TSSOP-20	PW	PGA116
PGA117	Scope(3)/10 Channels	TSSOP-20	PW	PGA117

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Binary gains: 1, 2, 4, 8, 16, 32, 64, and 128.
(3) Scope gains: 1, 2, 5, 10, 20, 50, 100, and 200.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		PGA112, PGA113, PGA116, PGA117	UNIT
Supply Voltage		+7	V
Signal Input Terminals, Voltage(2)		GND – 0.5 to (AV_{DD}) + 0.5	V
Signal Input Terminals, Current(2)		±10	mA
Output Short-Circuit		Continuous	
Operating Temperature		–40 to +125	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings:	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	300	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less.

ELECTRICAL CHARACTERISTICS: $V_S = AV_{DD} = DV_{DD} = +5V$

Boldface limits apply over the specified temperature range, T_A = –40°C to +125°C.
At T_A = +25°C, R_L = 10kΩ//C_L = 100pF connected to $DV_{DD}/2$, and V_{REF} = GND, unless otherwise noted.

PARAMETER		CONDITIONS	PGA112, PGA113, PGA116, PGA117 MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	$AV_{DD} = DV_{DD}$ = +5V, $V_{REF} = V_{IN} = AV_{DD}/2$, V_{CM} = 2.5V		±25	±100	µV
		$AV_{DD} = DV_{DD}$ = +5V, $V_{REF} = V_{IN} = AV_{DD}/2$, V_{CM} = 4.5V		±75	±325	µV
vs Temperature, –40°C to +125°C	**dV_{OS}/dT**	**$AV_{DD} = DV_{DD}$ = +5V, V_{CM} = 2.5V**		**0.35**	**1.2**	**µV/°C**
vs Temperature, –40°C to +85°C		$AV_{DD} = DV_{DD}$ = +5V, V_{CM} = 2.5V		0.15	0.9	µV/°C
vs Temperature, –40°C to +125°C		**$AV_{DD} = DV_{DD}$ = +5V, V_{CM} = 4.5V**		**0.6**	**1.8**	**µV/°C**
vs Temperature, –40°C to +85°C		$AV_{DD} = DV_{DD}$ = +5V, V_{CM} = 4.5V		0.3	1.3	µV/°C
vs Power Supply	PSRR	$AV_{DD} = DV_{DD}$ = +2.2V to +5.5V, V_{CM} = 0.5V, $V_{REF} = V_{IN} = AV_{DD}/2$		5	20	µV/V
Over Temperature, –40°C to +125°C		**$AV_{DD} = DV_{DD}$ = +2.2V to +5.5V, V_{CM} = 0.5V, $V_{REF} = V_{IN} = AV_{DD}/2$**		**5**	**40**	**µV/V**
INPUT ON-CHANNEL CURRENT						
Input On-Channel Current (Ch0, Ch1)	I_{IN}	$V_{REF} = V_{IN} = AV_{DD}/2$		±1.5	±5	nA
Over Temperature, –40°C to +125°C		**$V_{REF} = V_{IN} = AV_{DD}/2$**	**See Typical Characteristics**			**nA**
INPUT VOLTAGE RANGE						
Input Voltage Range(1)	I_{VR}		GND – 0.1		AV_{DD} + 0.1	V
Overvoltage Input Range		No Output Phase Reversal(2)	GND – 0.3		AV_{DD} + 0.3	V
INPUT IMPEDANCE (Channel On)(3)						
Channel Input Capacitance	C_{CH}			2		pF
Channel Switch Resistance	R_{SW}			150		Ω
Amplifier Input Capacitance	C_{AMP}			3		pF
Amplifier Input Resistance	R_{AMP}	Input Resistance to GND		10		GΩ
V_{CAL}/CH0	R_{IN}	CAL1 or CAL2 Selected		100		kΩ
GAIN SELECTIONS						
Nominal Gains		Binary gains: 1, 2, 4, 8, 16, 32, 64, 128	1		128	
		Scope gains: 1, 2, 5, 10, 20, 50, 100, 200	1		200	
DC Gain Error	G = 1	V_{OUT} = GND + 85mV to DV_{DD} – 85mV		0.006	0.1	%
	1 < G ≤ 32	V_{OUT} = GND + 85mV to DV_{DD} – 85mV			0.1	%
	G ≥ 50	V_{OUT} = GND + 85mV to DV_{DD} – 85mV			0.3	%
DC Gain Drift	**G = 1**	**V_{OUT} = GND + 85mV to DV_{DD} – 85mV**		**0.5**		**ppm/°C**
	1 < G ≤ 32	**V_{OUT} = GND + 85mV to DV_{DD} – 85mV**		**2**		**ppm/°C**
	G ≥ 50	**V_{OUT} = GND + 85mV to DV_{DD} – 85mV**		**6**		**ppm/°C**
CAL2 DC Gain Error(4)		Op Amp + Input = $0.9V_{CAL}$, $V_{REF} = V_{CAL} = AV_{DD}/2$, G = 1		0.02		%
CAL2 DC Gain Drift(4)		**Op Amp + Input = $0.9V_{CAL}$, $V_{REF} = V_{CAL} = AV_{DD}/2$, G = 1**		**2**		**ppm/°C**
CAL3 DC Gain Error(4)		Op Amp + Input = $0.1V_{CAL}$, $V_{REF} = V_{CAL} = AV_{DD}/2$, G = 1		0.02		%
CAL3 DC Gain Drift(4)		**Op Amp + Input = $0.1V_{CAL}$, $V_{REF} = V_{CAL} = AV_{DD}/2$, G = 1**		**2**		**ppm/°C**
INPUT IMPEDANCE (Channel Off)(3)						
Input Impedance	C_{CH}	See Figure 1		2		pF
INPUT OFF-CHANNEL CURRENT						
Input Off-Channel Current (Ch0, Ch1)(5)	I_{LKG}	V_{REF} = GND, $V_{OFF-CHANNEL} = AV_{DD}/2$, $V_{ON-CHANNEL} = AV_{DD}/2$ – 0.1V		±0.05	±1	nA
Over Temperature, –40°C to +125°C		**V_{REF} = GND, $V_{OFF-CHANNEL} = AV_{DD}/2$, $V_{ON-CHANNEL} = AV_{DD}/2$ – 0.1V**	**See Typical Characteristics**			
Channel-to-Channel Crosstalk				130		dB

(1) Gain error is a function of the input voltage. Gain error outside of the range (GND + 85mV ≤ V_{OUT} ≤ DV_{DD} – 85mV) increases to 0.5% (typical).
(2) Input voltages beyond this range must be current limited to < |10mA| through the input protection diodes on each channel to prevent permanent destruction of the device.
(3) See Figure 1.
(4) Total V_{OUT} error must be computed using input offset voltage error multiplied by gain. Includes op amp G = 1 error.
(5) Maximum specification limitation limited by final test time and capability.

ELECTRICAL CHARACTERISTICS: $V_S = AV_{DD} = DV_{DD} = +5V$ (continued)

Boldface limits apply over the specified temperature range, $T_A = –40°C$ to $+125°C$.
At $T_A = +25°C$, $R_L = 10kΩ//C_L = 100pF$ connected to $DV_{DD}/2$, and V_{REF} = GND, unless otherwise noted.

PARAMETER		CONDITIONS	PGA112, PGA113, PGA116, PGA117 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output Swing from Rail		I_{OUT} = ±0.25mA, $AV_{DD} \geq DV_{DD}$ (6)	GND + 0.05		DV_{DD} – 0.05	V
		I_{OUT} = ±5mA, $AV_{DD} \geq DV_{DD}$ (6)	GND + 0.25		DV_{DD} – 0.25	V
DC Output Nonlinearity		V_{OUT} = GND + 85mV to DV_{DD} – 85mV (7)		0.0015		%FSR
Short-Circuit Current	I_{SC}			–30/+60		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			
NOISE						
Input Voltage Noise Density	e_n	f > 10kHz, C_L = 100pF, V_S = 5V		12		nV/√Hz
		f > 10kHz, C_L = 100pF, V_S = 2.2V		22		nV/√Hz
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz, C_L = 100pF, V_S = 5V		0.362		μV_{PP}
		f = 0.1Hz to 10Hz, C_L = 100pF, V_S = 2.2V		0.736		μV_{PP}
Input Current Density	I_n	f = 10kHz, C_L = 100pF		400		fA/√Hz
SLEW RATE						
Slew Rate	SR		See Table 1			V/µs
SETTLING TIME						
Settling Time	t_S		See Table 1			µs
FREQUENCY RESPONSE						
Frequency Response			See Table 1			MHz
THD + NOISE						
		G = 1, f = 1kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.003		%
		G = 10, f = 1kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.005		%
		G = 50, f = 1kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.03		%
		G = 128, f = 1kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.08		%
		G = 200, f = 1kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.1		%
		G = 1, f = 20kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.02		%
		G = 10, f = 20kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.01		%
		G = 50, f = 20kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.03		%
		G = 128, f = 20kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.08		%
		G = 200, f = 20kHz, $V_{OUT} = 4V_{PP}$ at $2.5V_{DC}$, C_L = 100pF		0.11		%
POWER SUPPLY						
Operating Voltage Range (6)	AV_{DD}		2.2		5.5	V
	DV_{DD}		2.2		5.5	V
Quiescent Current Analog	I_{QA}	I_O = 0, G = 1, $V_{OUT} = V_{REF}$		0.33	0.45	mA
Over Temperature, –40°C to +125°C					**0.45**	**mA**
Quiescent Current Digital (8)(9)(10)	I_{QD}	I_O = 0, G = 1, $V_{OUT} = V_{REF}$, SCLK at 10MHz, $\overline{CS}$ = Logic 0, DIO or DIN = Logic 0		0.75	1.2	mA
Over Temperature, –40°C to +125°C (8)(9)(10)		**I_O = 0, G = 1, $V_{OUT} = V_{REF}$, SCLK at 10MHz, $\overline{CS}$ = Logic 0, DIO or DIN = Logic 0**			**1.2**	**mA**
Shutdown Current Analog + Digital (8)(9)	$I_{SDA} + I_{SDD}$	I_O = 0, $V_{OUT} = V_{REF}$, G = 1, SCLK Idle		4		µA
		I_O = 0, V_{OUT} = 0, G = 1, SCLK at 10MHz, $\overline{CS}$ = Logic 0, DIO or DIN = Logic 0		245		µA
POWER-ON RESET (POR)						
POR Trip Voltage		Digital interface disabled and Command Register set to POR values for DV_{DD} < POR Trip Voltage		1.6		V

(6) When AV_{DD} is less than DV_{DD}, the output is clamped to AV_{DD} + 300mV.
(7) Measurement limited by noise in test equipment and test time.
(8) Does not include current into or out of the V_{REF} pin. Internal R_F and R_I are always connected between V_{OUT} and V_{REF}.
(9) Digital logic levels: DIO or DIN = logic 0. 10µA internal pull-down current source.
(10) Includes current from op amp output structure.

ELECTRICAL CHARACTERISTICS: $V_S = AV_{DD} = DV_{DD} = +5V$ (continued)

Boldface limits apply over the specified temperature range, $T_A = –40°C$ to $+125°C$.
At $T_A = +25°C$, $R_L = 10kΩ//C_L = 100pF$ connected to $DV_{DD}/2$, and V_{REF} = GND, unless otherwise noted.

PARAMETER	CONDITIONS	PGA112, PGA113, PGA116, PGA117 MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified Range		–40		+125	°C
Operating Range		–40		+125	°C
Thermal Resistance θ_{JA}					
MSOP-10			164		°C/W
DIGITAL INPUTS (SCLK, $\overline{CS}$, DIO, DIN)					
Logic Low		0		$0.3DV_{DD}$	V
Input Leakage Current (SCLK and $\overline{CS}$ only)		–1		+1	µA
Weak Pull-Down Current (DIO, DIN only)			10		µA
Logic High		$0.7DV_{DD}$		DV_{DD}	V
Hysteresis			700		mV
DIGITAL OUTPUT (DIO, DOUT)					
Logic High	I_{OH} = –3mA (sourcing)	DV_{DD} – 0.4		DV_{DD}	V
Logic Low	I_{OL} = +3mA (sinking)	GND		GND + 0.4	V
CHANNEL AND GAIN TIMING					
Channel Select Time			0.2		µs
Gain Select Time			0.2		µs
SHUTDOWN MODE TIMING					
Enable Time			4.0		µs
Disable Time	V_{OUT} goes high-impedance, R_F and R_I remain connected between V_{OUT} and V_{REF}		2.0		µs
POWER-ON-RESET (POR) TIMING					
POR Power-Up Time	$DV_{DD} \geq 2V$		40		µs
POR Power-Down Time	$DV_{DD} \leq 1.5V$		5		µs

Table 1. Frequency Response versus Gain ($C_L = 100pF$, $R_L = 10kΩ$)

BINARY GAIN (V/V)	TYPICAL –3dB FREQUENCY (MHz)	SLEW RATE-FALL (V/µs)	SLEW RATE-RISE (V/µs)	0.1% SETTLING TIME: $4V_{PP}$ (µs)	0.01% SETTLING TIME: $4V_{PP}$ (µs)	SCOPE GAIN (V/V)	TYPICAL –3dB FREQUENCY (MHz)	SLEW RATE-FALL (V/µs)	SLEW RATE-RISE (V/µs)	0.1% SETTLING TIME: $4V_{PP}$ (µs)	0.01% SETTLING TIME: $4V_{PP}$ (µs)
1	10	8	3	2	2.55	1	10	8	3	2	2.55
2	3.8	9	6.4	2	2.6	2	3.8	9	6.4	2	2.6
4	2	12.8	10.6	2	2.6	5	1.8	12.8	10.6	2	2.6
8	1.8	12.8	10.6	2	2.6	10	1.8	12.8	10.6	2.2	2.6
16	1.6	12.8	12.8	2.3	2.6	20	1.3	12.8	9.1	2.3	2.8
32	1.8	12.8	13.3	2.3	3	50	0.9	9.1	7.1	2.4	3.8
64	0.6	4	3.5	3	6	100	0.38	4	3.5	4.4	7
128	0.35	2.5	2.5	4.8	8	200	0.23	2.3	2	6.9	10

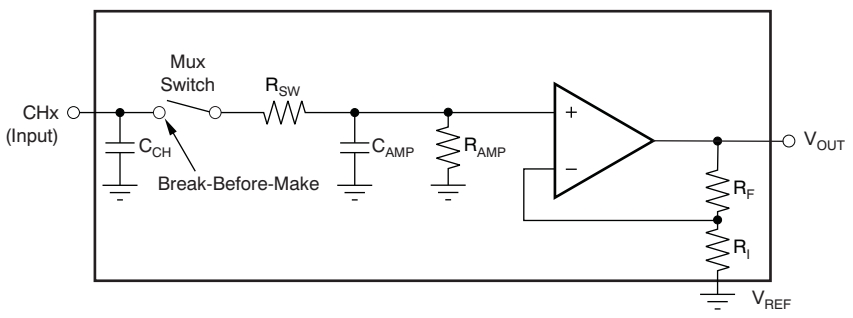


Figure 1. Equivalent Input Circuit

SPI TIMING: $V_S = AV_{DD} = DV_{DD}$ = +2.2V to +5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10kΩ//C_L = 100pF connected to $DV_{DD}/2$, and V_{REF} = GND, unless otherwise noted.

PARAMETER		TEST CONDITIONS	PGA112, PGA113, PGA116, PGA117 MIN	TYP	MAX	UNIT
Input Capacitance (SCLK, $\overline{CS}$, and DIO pins)				1		pF
Input Rise/Fall Time(1) ($\overline{CS}$, SCLK, and DIO pins)	t_{RFI}				2	µs
Output Rise/Fall Time (DIO pin)(1)	t_{RFO}	C_{LOAD} = 60pF			10	ns
$\overline{CS}$ High Time ($\overline{CS}$ pin)(1)	t_{CSH}		40			ns
SCLK Edge to $\overline{CS}$ Fall Setup Time(1)	t_{CSO}		10			ns
$\overline{CS}$ Fall to First SCLK Edge Setup Time	t_{CSSC}		10			ns
SCLK Frequency(2)	f_{SCLK}				10	MHz
SCLK High Time(3)	t_{HI}		40			ns
SCLK Low Time(3)	t_{LO}		40			ns
SCLK Last Edge to $\overline{CS}$ Rise Setup Time(1)	t_{SCCS}		10			ns
$\overline{CS}$ Rise to SCLK Edge Setup Time(1)	t_{CS1}		10			ns
DIN Setup Time	t_{SU}		10			ns
DIN Hold Time	t_{HD}		10			ns
SCLK to DOUT Valid Propagation Delay(1)	t_{DO}				25	ns
$\overline{CS}$ Rise to DOUT Forced to Hi-Z(1)	t_{SOZ}				20	ns

(1) Ensured by design; not production tested.
(2) When using devices in daisy-chain mode, the maximum clock frequency for SCLK is limited by SCLK rise/fall time, DIN setup time, and DOUT propagation delay. See Figure 63. Based on this limitation, the maximum SCLK frequency for daisy-chain mode is 9.09MHz.
(3) t_{HI} and t_{LO} must not be less than 1/SCLK (max).

SPI TIMING DIAGRAMS

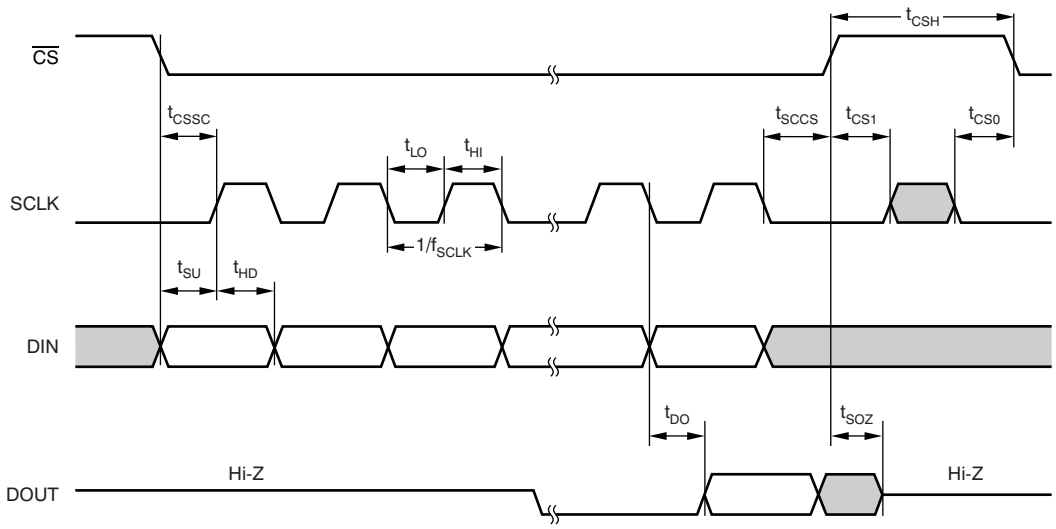


Figure 2. SPI Mode 0, 0

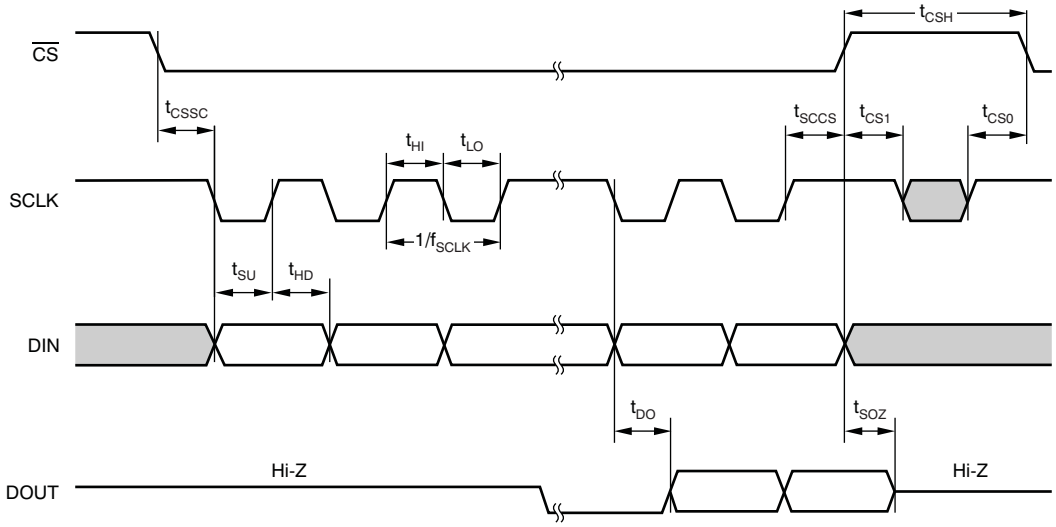
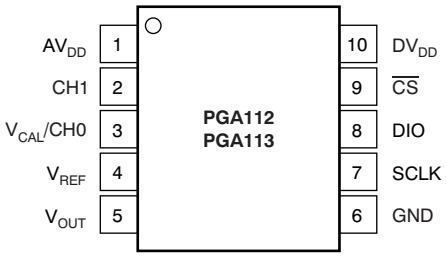


Figure 3. SPI Mode 1, 1

PIN CONFIGURATIONS

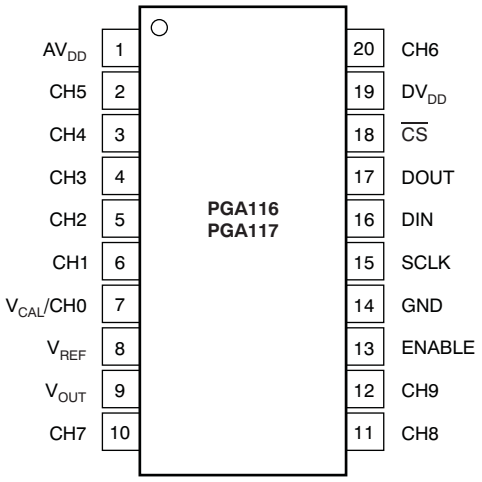
MSOP-10
DGS PACKAGE
(TOP VIEW)



PGA112, PGA113 TERMINAL FUNCTIONS

MSOP PACKAGE PIN #	NAME	DESCRIPTION
1	AV_{DD}	Analog supply voltage (+2.2V to +5.5V)
2	CH1	Input MUX channel 1
3	V_{CAL}/CH0	Input MUX channel 0 and V_{CAL} input. For system calibration purposes, connect this pin to a low-impedance external reference voltage to use internal calibration channels. The four internal calibration channels are connected to GND, $0.9V_{CAL}$, $0.1V_{CAL}$, and V_{REF}, respectively. V_{CAL} is loaded with 100kΩ (typical) when internal calibration channels CAL2 or CAL3 are selected. Otherwise, V_{CAL}/CH0 appears as high impedance.
4	V_{REF}	Reference input pin. Connect external reference for V_{OUT} offset shift or to midsupply for midsupply referenced systems. V_{REF} must be connected to a low-impedance reference capable of sourcing and sinking at least 2mA or V_{REF} must be connected to GND.
5	V_{OUT}	Analog voltage output. When $AV_{DD} < DV_{DD}$, V_{OUT} is clamped to AV_{DD} + 300mV.
6	GND	Ground pin
7	SCLK	Clock input for SPI serial interface
8	DIO	Data input/output for SPI serial interface. DIO contains a weak, 10µA internal pull-down current source.
9	$\overline{CS}$	Chip select line for SPI serial interface
10	DV_{DD}	Digital and op amp output stage supply voltage (+2.2V to +5.5V). Useful in multi-supply systems to prevent overvoltage/lockup condition on an analog-to-digital (ADC) input (for example, a microcontroller with an ADC running on +3V and the PGA powered from +5V). Digital I/O levels to be relative to DV_{DD}. DV_{DD} should be bypassed with a 0.1µF ceramic capacitor, and DV_{DD} must supply the current for the digital portion of the PGA as well as the load current for the op amp output stage.

TSSOP-20
PW PACKAGE
(TOP VIEW)



PGA116, PGA117 TERMINAL FUNCTIONS

TSSOP PACKAGE PIN #	NAME	DESCRIPTION
1	AV_{DD}	Analog supply voltage (+2.2V to +5.5V)
2	CH5	Input MUX channel 5
3	CH4	Input MUX channel 4
4	CH3	Input MUX channel 3
5	CH2	Input MUX channel 2
6	CH1	Input MUX channel 1
7	V_{CAL}/CH0	Input MUX channel 0 and V_{CAL} input. For system calibration purposes, connect this pin to a low-impedance external reference voltage to use internal calibration channels. The four internal calibration channels are connected to GND, $0.9V_{CAL}$, $0.1V_{CAL}$, and V_{REF}, respectively. V_{CAL} is loaded with 100kΩ (typical) when internal calibration channels CAL2 or CAL3 are selected. Otherwise, V_{CAL}/CH0 appears as high impedance.
8	V_{REF}	Reference input pin. Connect external reference for V_{OUT} offset shift or to midsupply for midsupply referenced systems. V_{REF} must be connected to a low-impedance reference capable of sourcing and sinking at least 2mA or to GND.
9	V_{OUT}	Analog voltage output. When $AV_{DD} < DV_{DD}$, V_{OUT} is clamped to AV_{DD} + 300mV.
10	CH7	Input MUX channel 7
11	CH8	Input MUX channel 8
12	CH9	Input MUX channel 9
13	ENABLE	Hardware enable pin. Logic low puts the part into Shutdown mode (I_Q < 1µA).
14	GND	Ground pin
15	SCLK	Clock input for SPI serial interface
16	DIN	Data input for SPI serial interface. DIN contains a weak, 10µA internal pull-down current source to allow for ease of daisy-chain configurations.
17	DOUT	Data output for SPI serial interface. DOUT goes to high-Z state when $\overline{CS}$ goes high for standard SPI interface.
18	$\overline{CS}$	Chip select line for SPI serial interface
19	DV_{DD}	Digital and op amp output stage supply voltage (+2.2V to +5.5V). Useful in multi-supply systems to prevent overvoltage/lockup condition on an ADC input (for example, a microcontroller with an ADC running on +3V and the PGA powered from +5V). Digital I/O levels to be relative to DV_{DD}. DV_{DD} should be bypassed with a 0.1µF ceramic capacitor, and DV_{DD} must supply the current for the digital portion of the PGA as well as the load current for the op amp output stage.
20	CH6	Input MUX channel 6

TYPICAL APPLICATION CIRCUITS

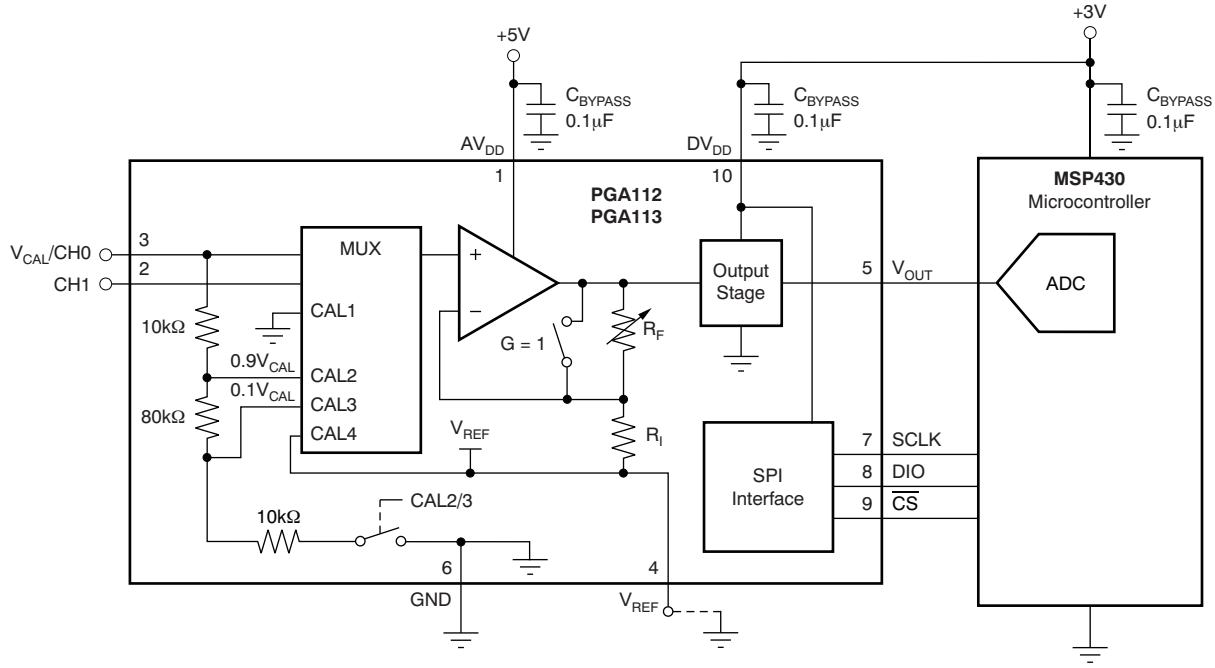


Figure 4. PGA112, PGA113 (MSOP-10)

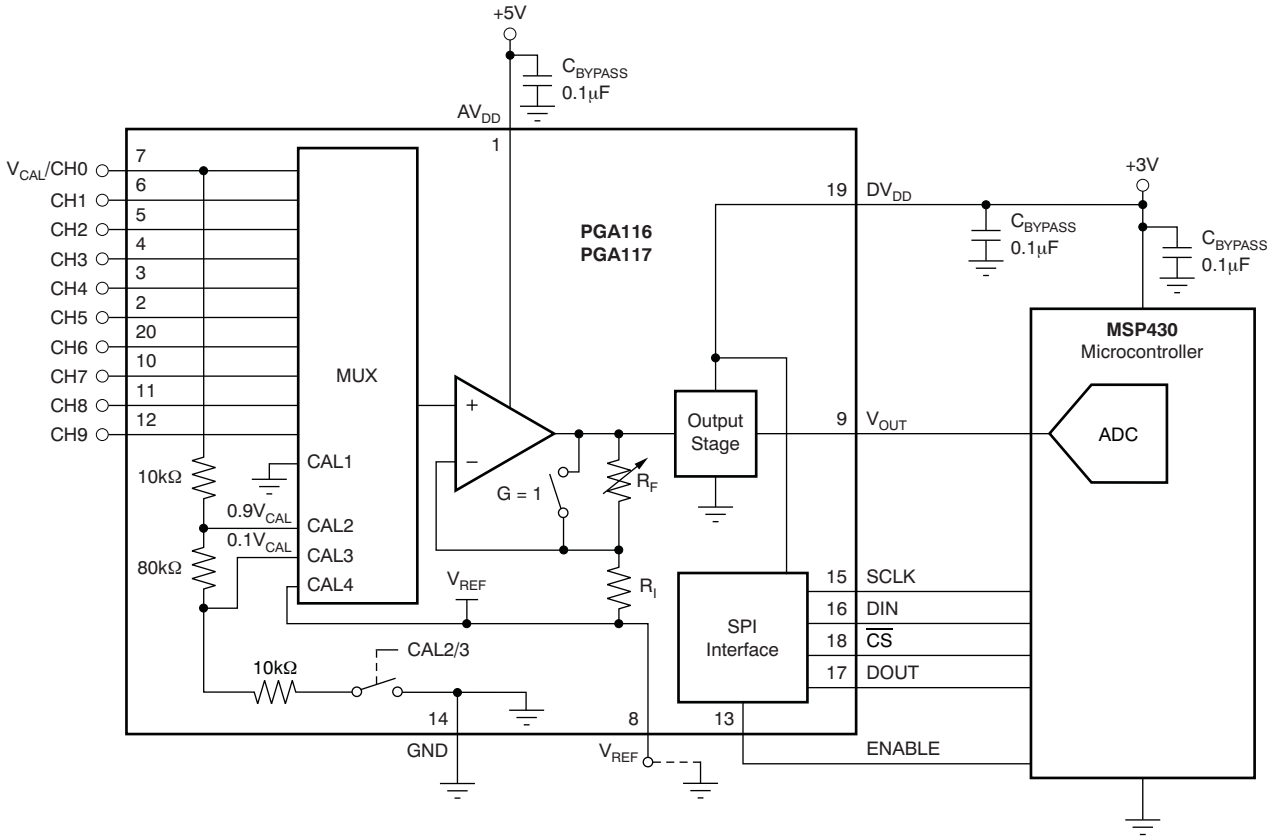


Figure 5. PGA116, PGA117 (TSSOP-20)

TYPICAL CHARACTERISTICS

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

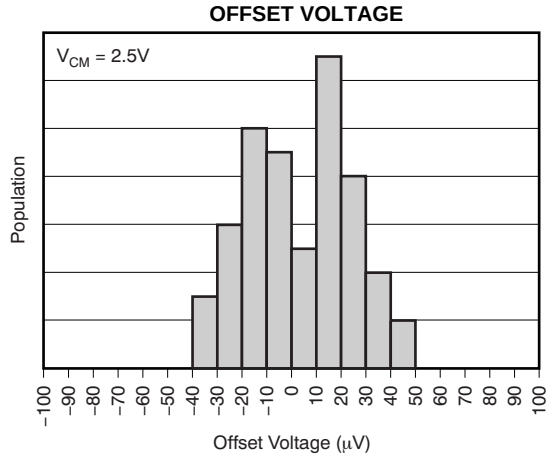


Figure 6.

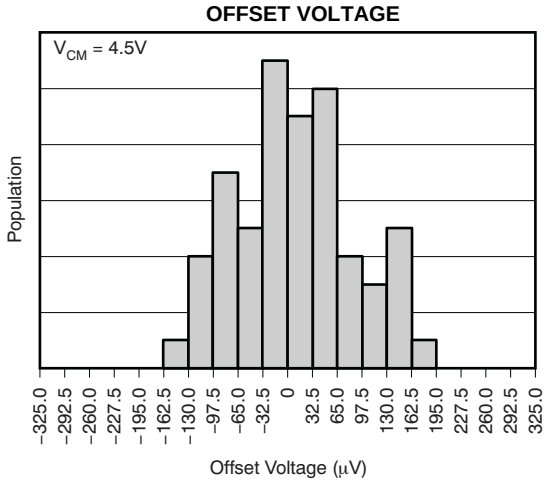


Figure 7.

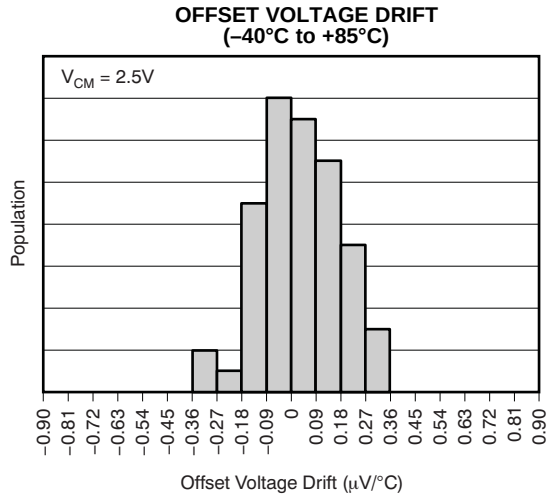


Figure 8.

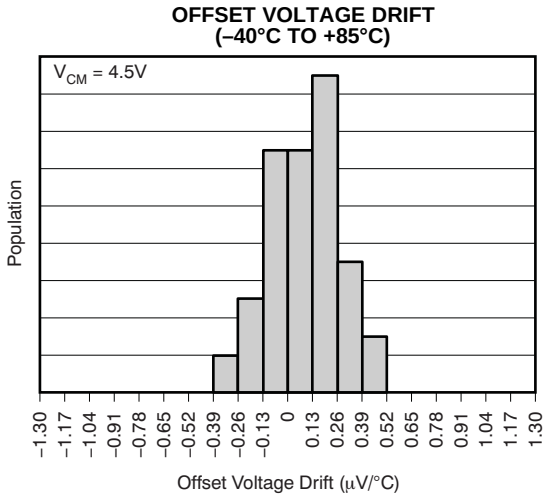


Figure 9.

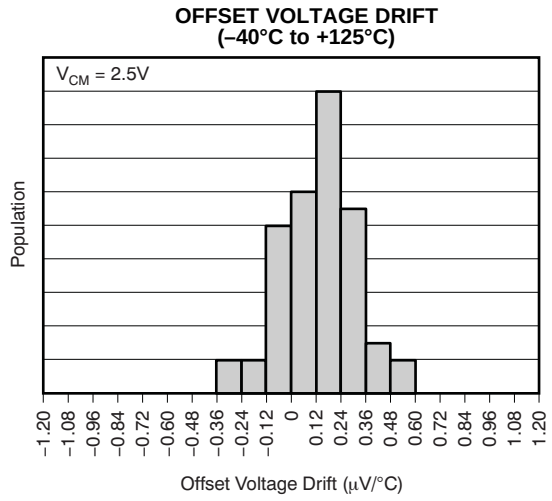


Figure 10.

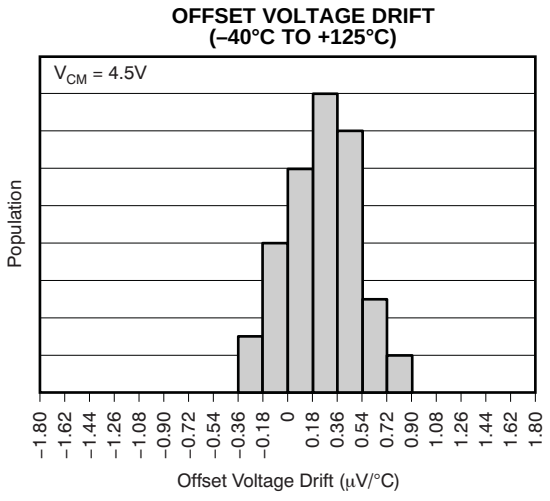


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

INPUT OFFSET VOLTAGE vs INPUT VOLTAGE

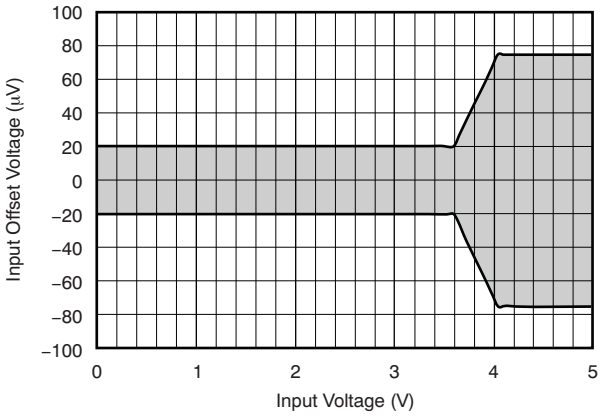


Figure 12.

PGA112/PGA116 NONLINEARITY

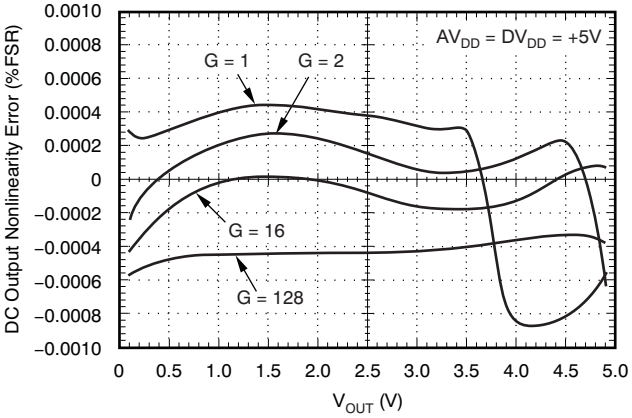


Figure 13.

GAIN ERROR (G = 1)

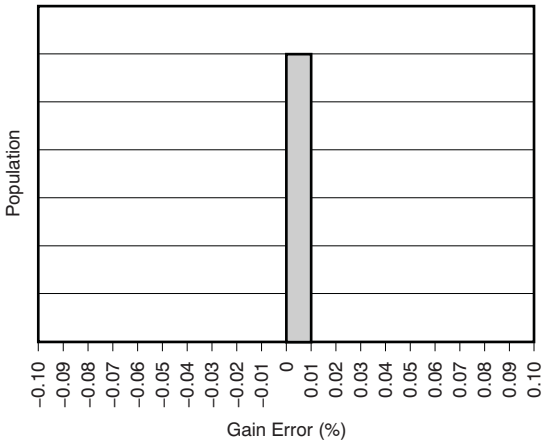


Figure 14.

GAIN ERROR (1 < G ≤ 32)

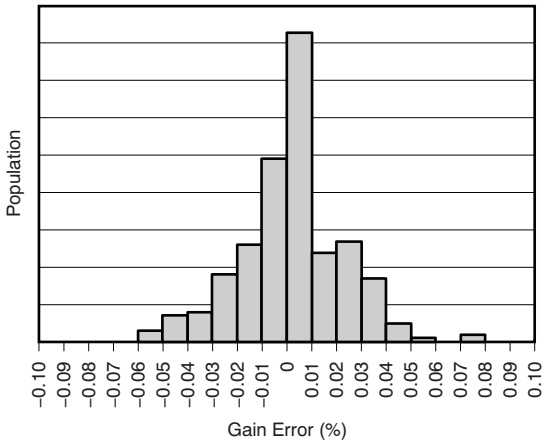


Figure 15.

GAIN ERROR (G ≥ 50)

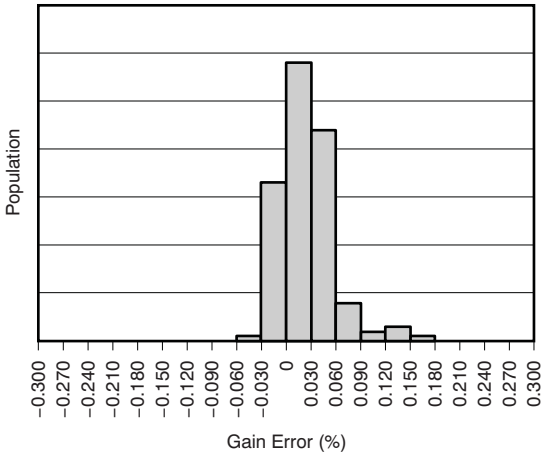


Figure 16.

GAIN ERROR DRIFT (–40°C to +125°C)

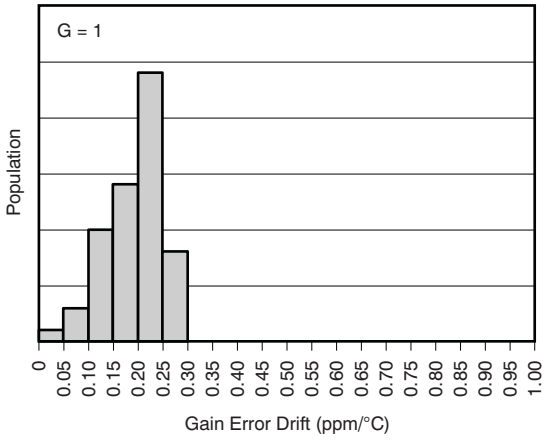


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

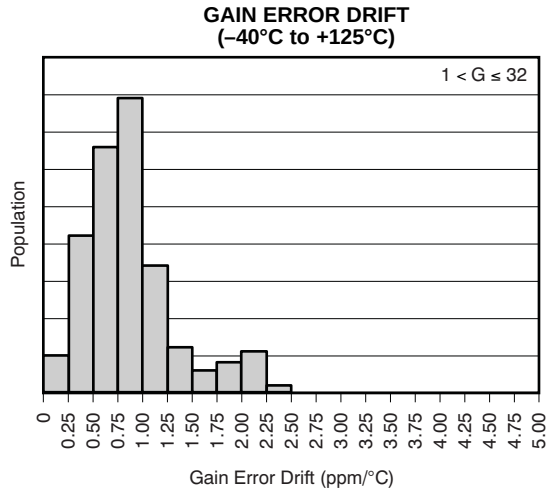


Figure 18.

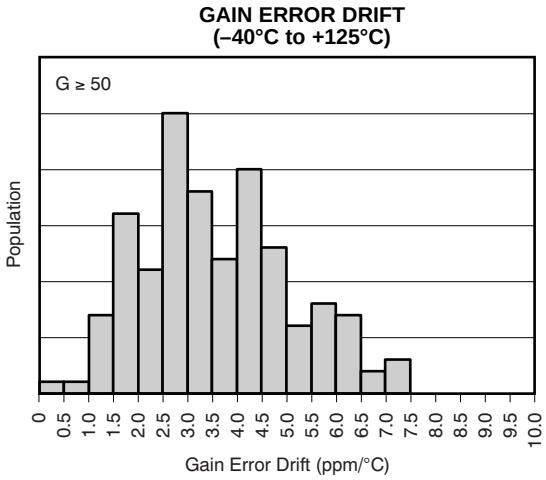


Figure 19.

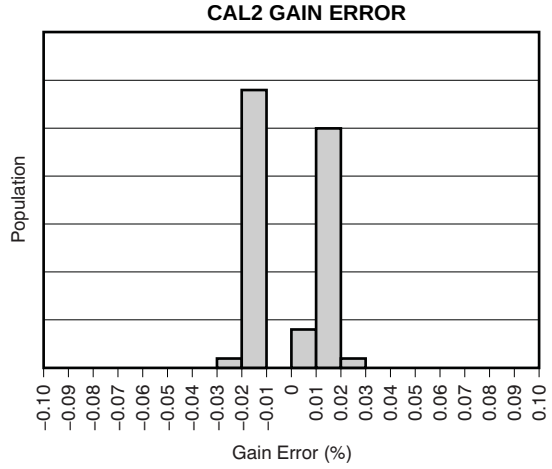


Figure 20.

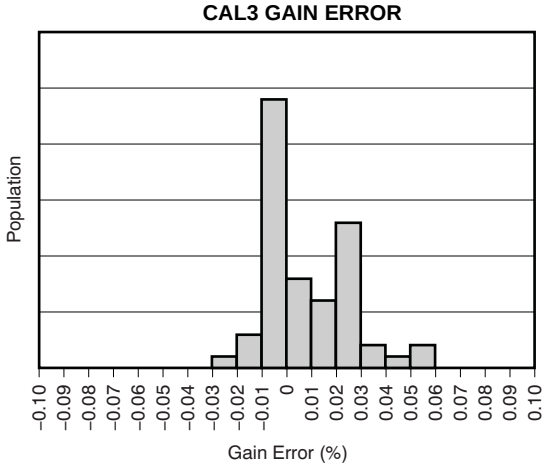


Figure 21.

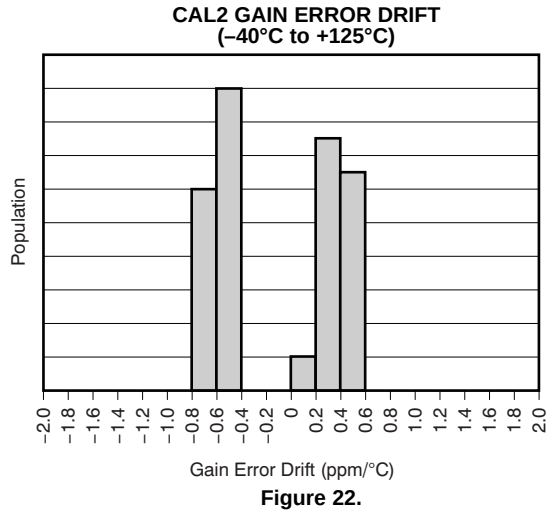


Figure 22.

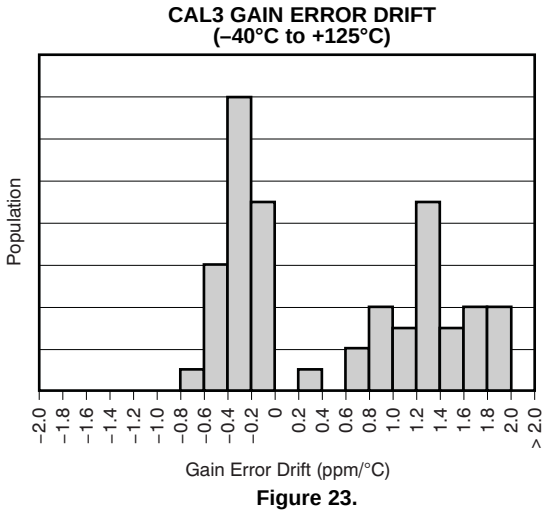


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

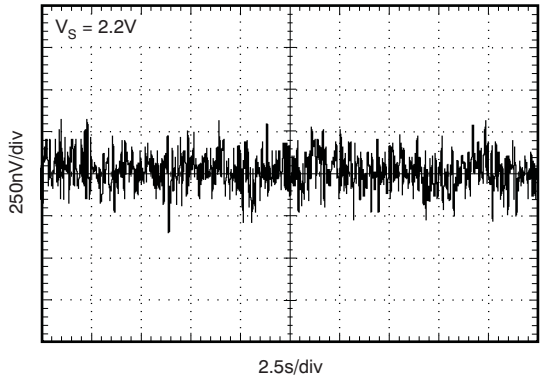


Figure 24.

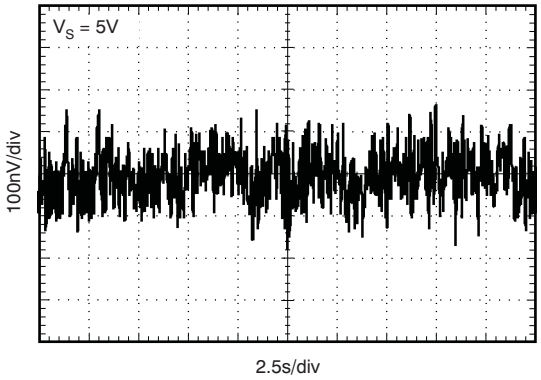


Figure 25.

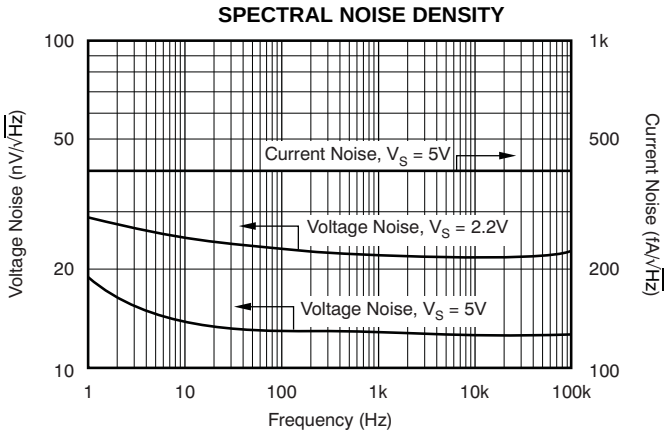


Figure 26.

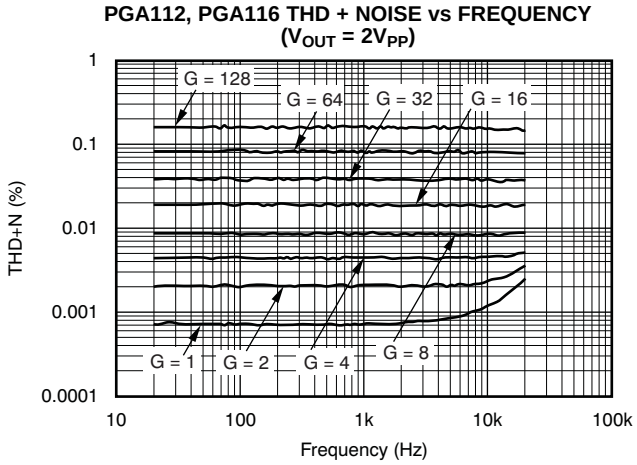


Figure 27.

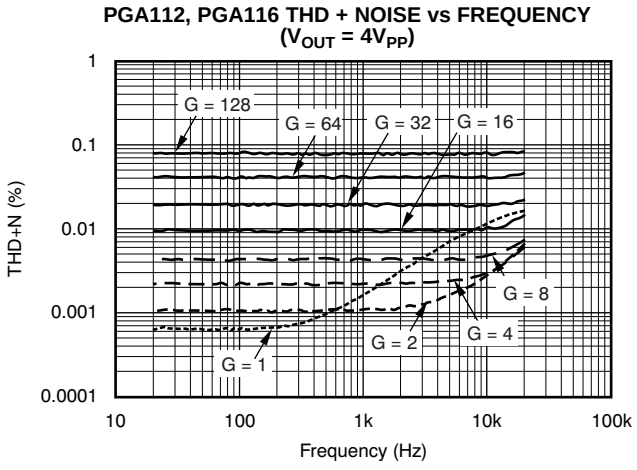


Figure 28.

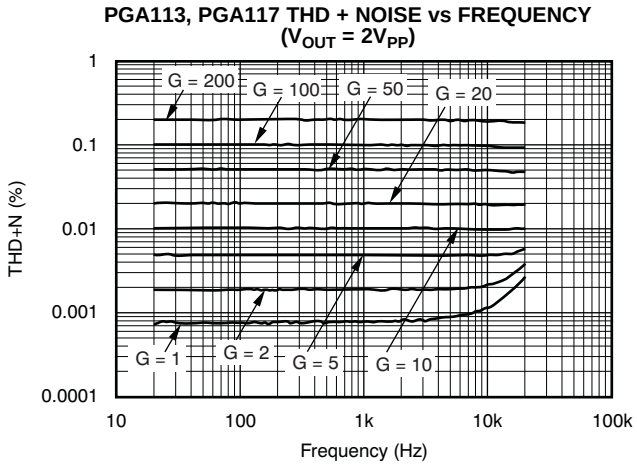


Figure 29.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

PGA113, PGA117 THD + NOISE vs FREQUENCY (V_{OUT} = 4V_{PP})

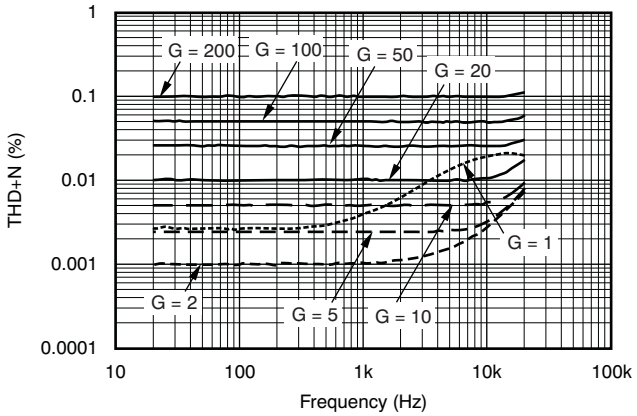


Figure 30.

QUIESCENT CURRENT vs TEMPERATURE

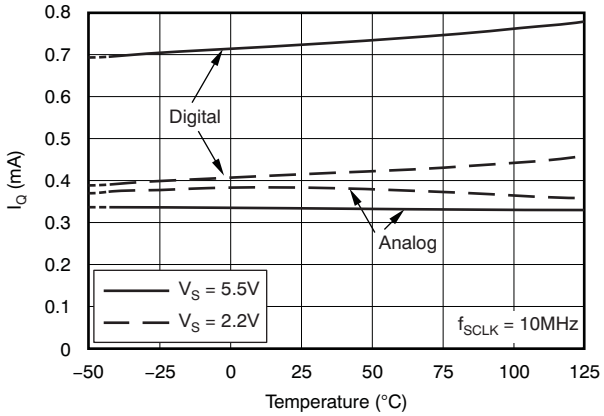


Figure 31.

TOTAL QUIESCENT CURRENT vs SUPPLY VOLTAGE

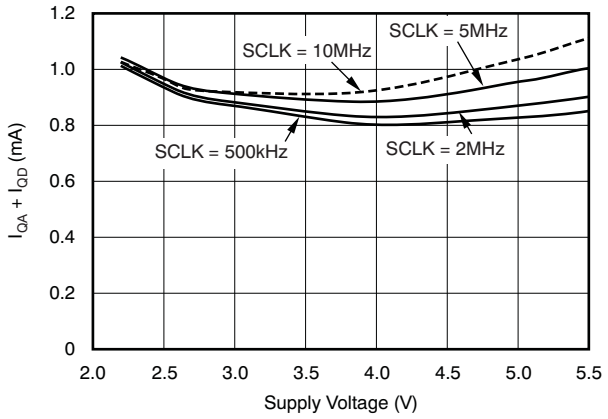


Figure 32.

SHUTDOWN QUIESCENT CURRENT vs TEMPERATURE

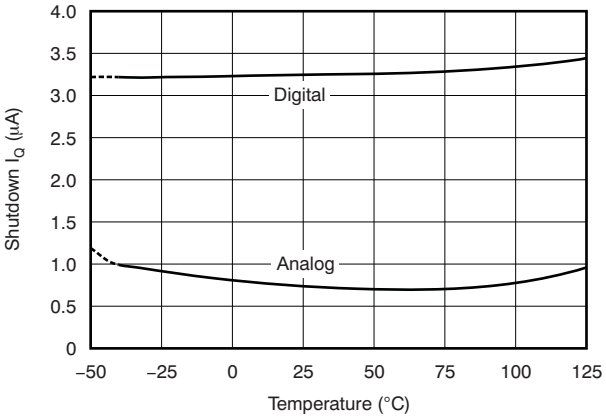


Figure 33.

OUTPUT VOLTAGE vs OUTPUT CURRENT

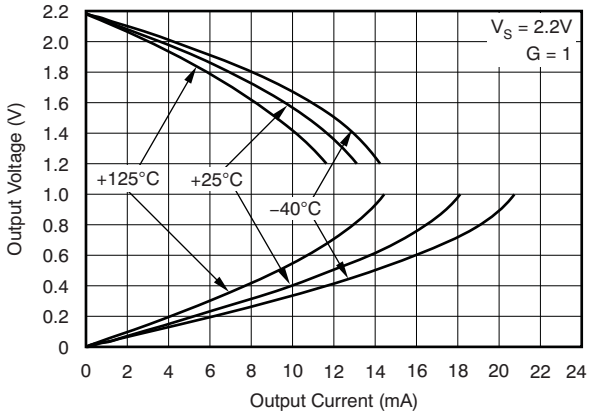


Figure 34.

OUTPUT VOLTAGE vs OUTPUT CURRENT

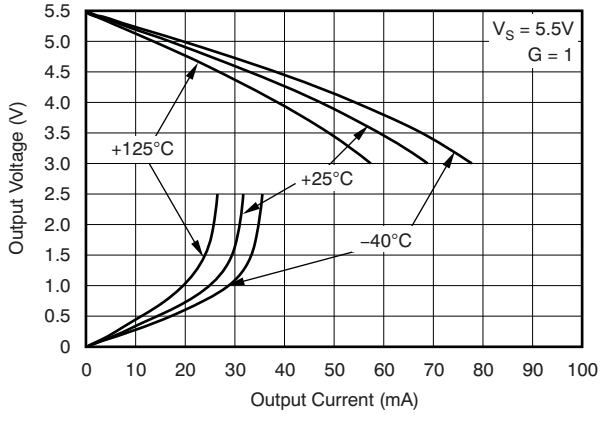


Figure 35.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

PGA112, PGA116 OUTPUT VOLTAGE SWING vs FREQUENCY

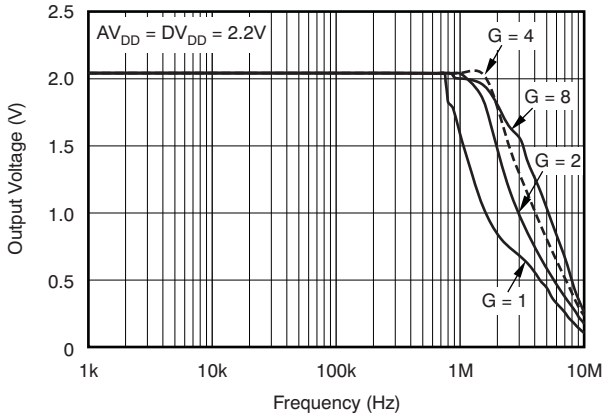


Figure 36.

PGA112, PGA116 OUTPUT VOLTAGE SWING vs FREQUENCY

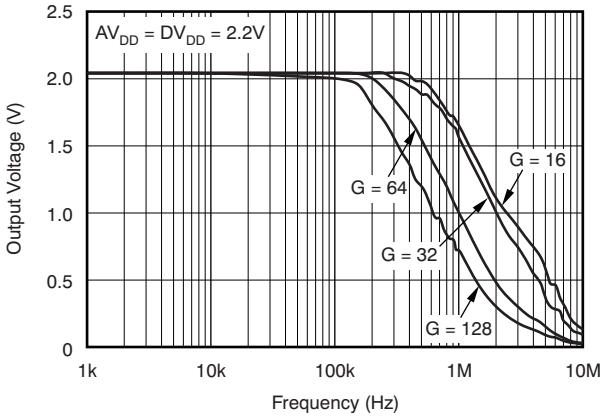


Figure 37.

PGA112, PGA116 OUTPUT VOLTAGE SWING vs FREQUENCY

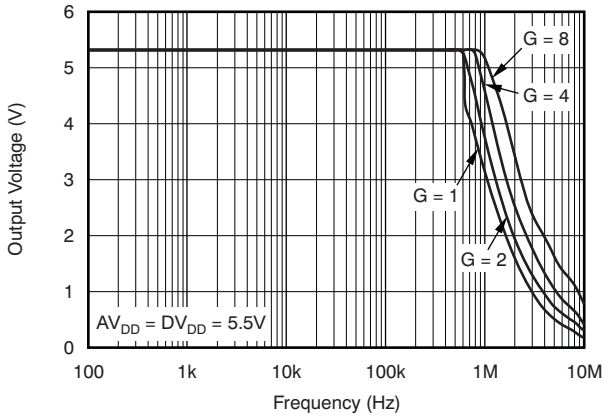


Figure 38.

PGA112, PGA116 OUTPUT VOLTAGE SWING vs FREQUENCY

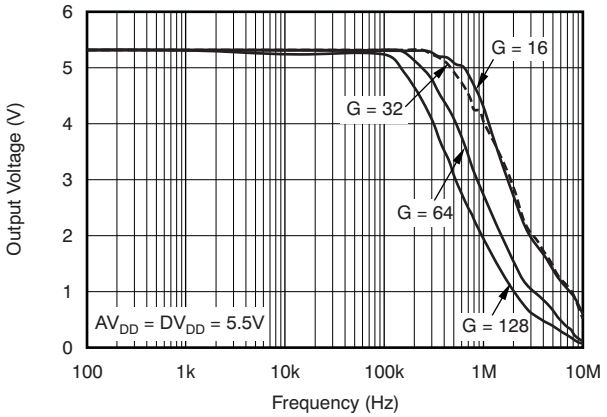


Figure 39.

PGA113, PGA117 OUTPUT VOLTAGE SWING vs FREQUENCY

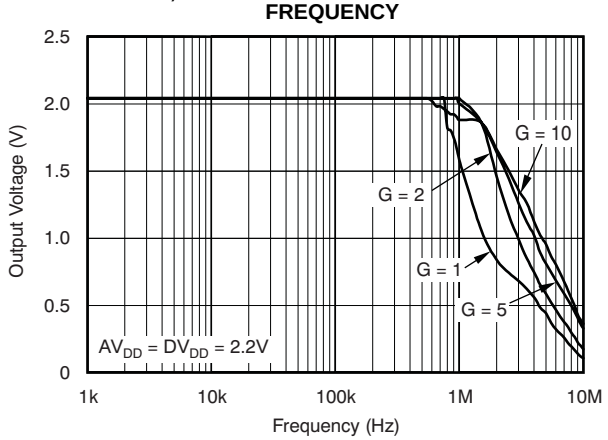


Figure 40.

PGA113, PGA117 OUTPUT VOLTAGE SWING vs FREQUENCY

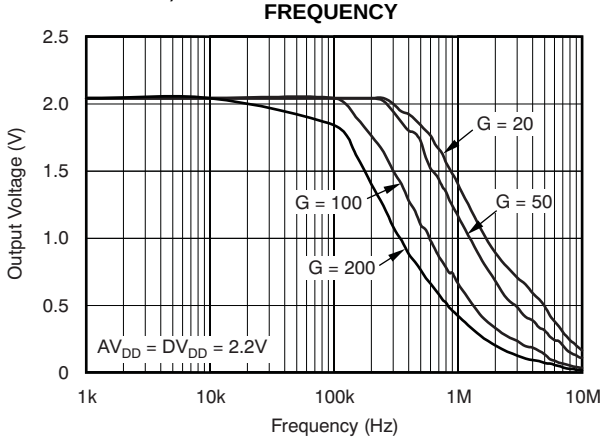


Figure 41.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

PGA113, PGA117 OUTPUT VOLTAGE SWING vs FREQUENCY

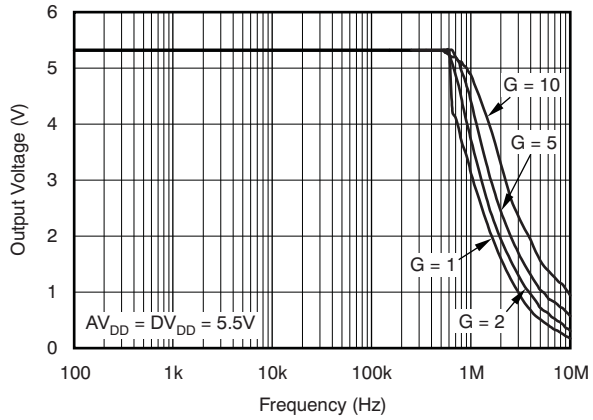


Figure 42.

PGA113, PGA117 OUTPUT VOLTAGE SWING vs FREQUENCY

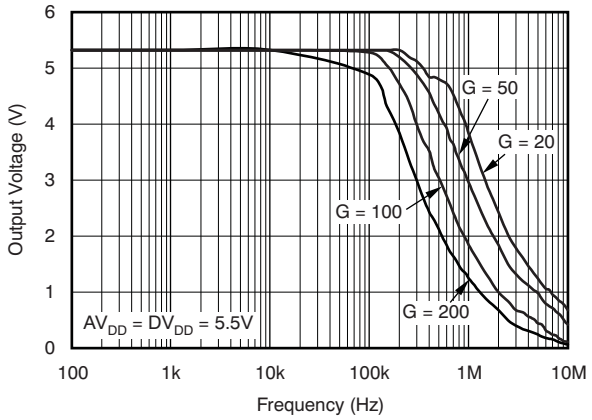


Figure 43.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

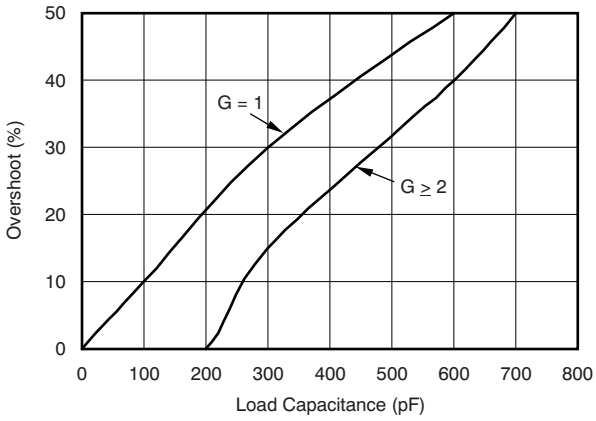


Figure 44.

GAIN vs SETTLING TIME

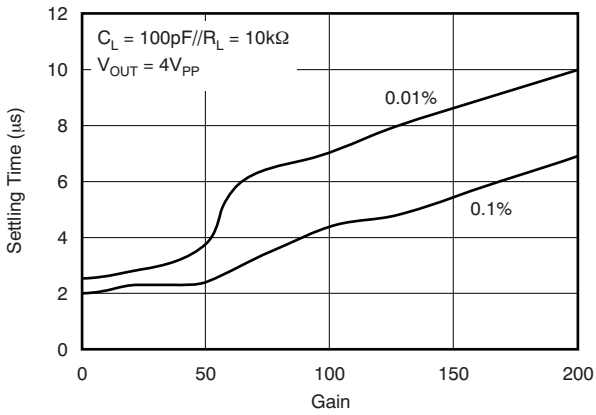


Figure 45.

INPUT ON-CHANNEL CURRENT vs TEMPERATURE

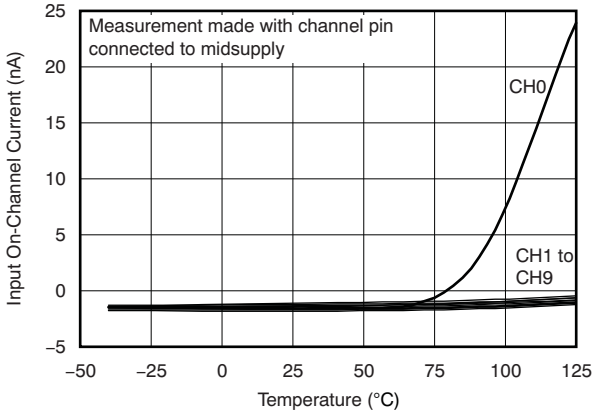


Figure 46.

INPUT OFF-CHANNEL LEAKAGE CURRENT vs TEMPERATURE

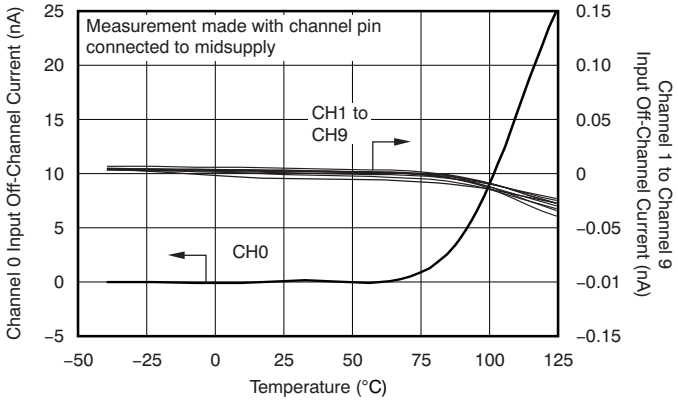


Figure 47.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to $DV_{DD}/2$, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

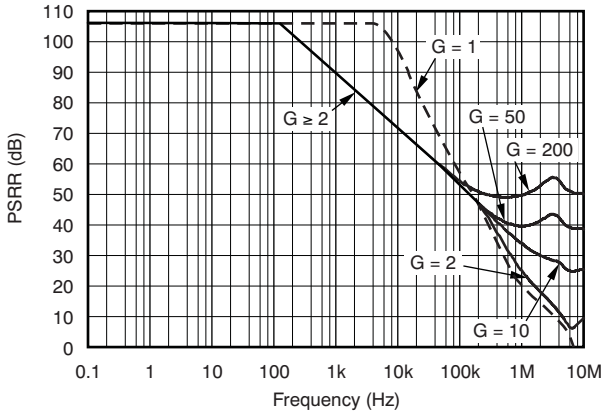


Figure 48.

CROSSTALK vs FREQUENCY

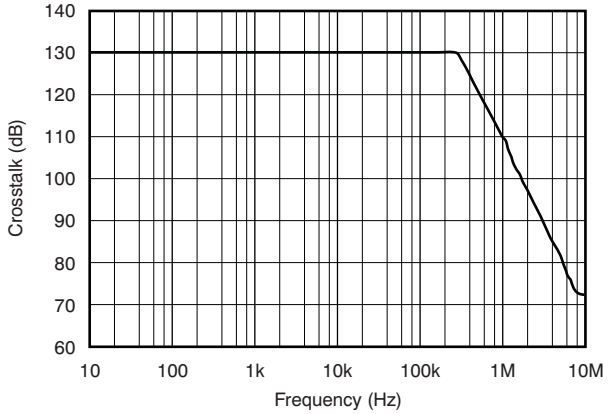


Figure 49.

SMALL-SIGNAL PULSE RESPONSE

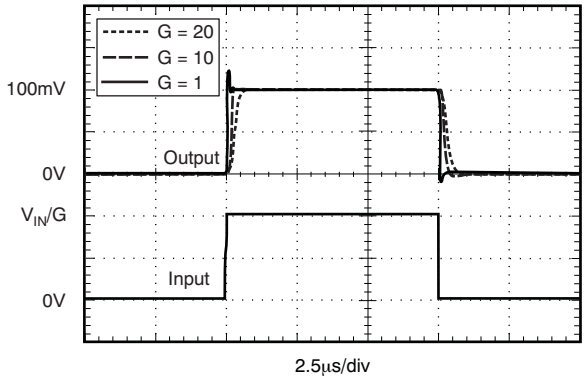


Figure 50.

SMALL-SIGNAL PULSE RESPONSE

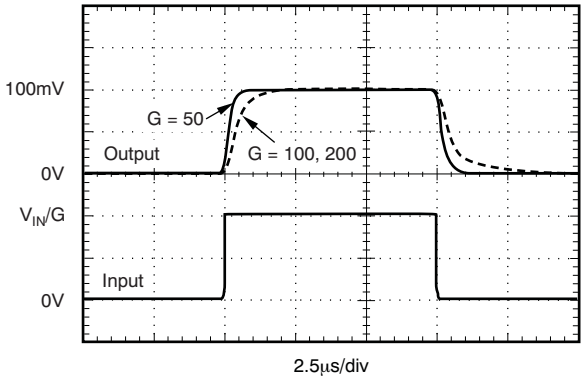


Figure 51.

LARGE-SIGNAL PULSE RESPONSE

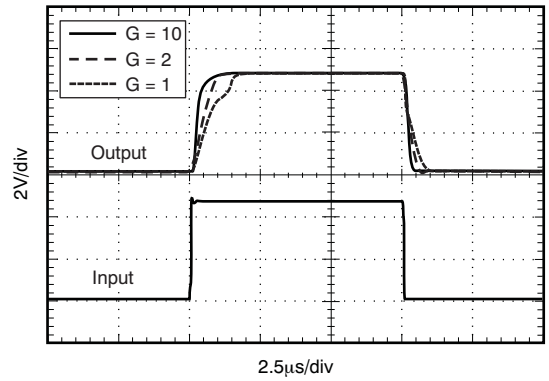


Figure 52.

LARGE-SIGNAL PULSE RESPONSE

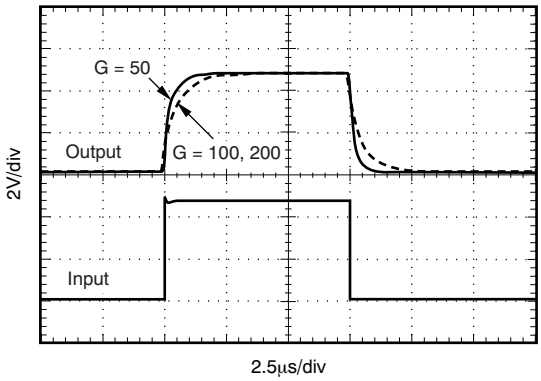


Figure 53.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AV_{DD} = DV_{DD} = 5V, R_L = 10kΩ connected to DV_{DD}/2, V_{REF} = GND, and C_L = 100pF, unless otherwise noted.

POWER-UP/POWER-DOWN TIMING

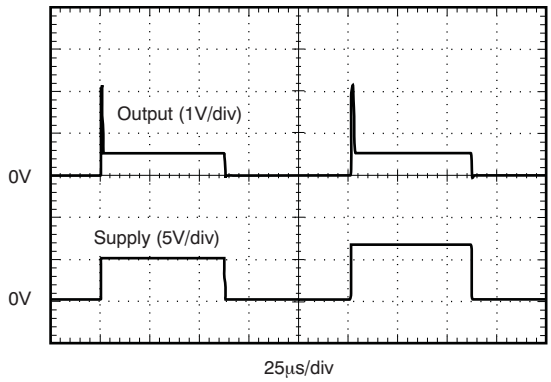


Figure 54.

OUTPUT OVERDRIVE PERFORMANCE

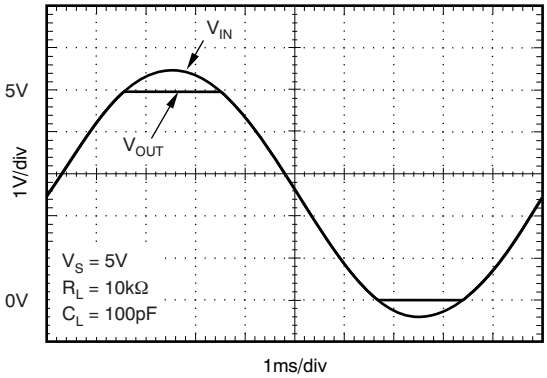


Figure 55.

OUTPUT VOLTAGE vs SHUTDOWN MODE

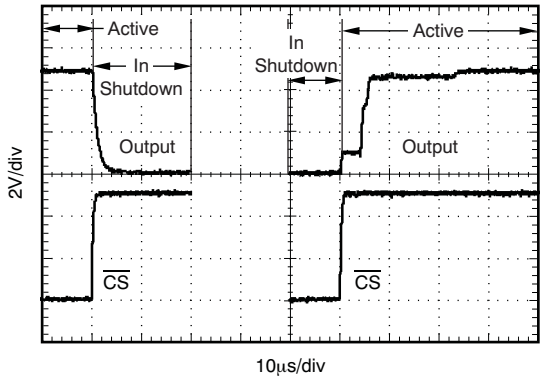


Figure 56.

PGA116, PGA117 HARDWARE SHUTDOWN MODE

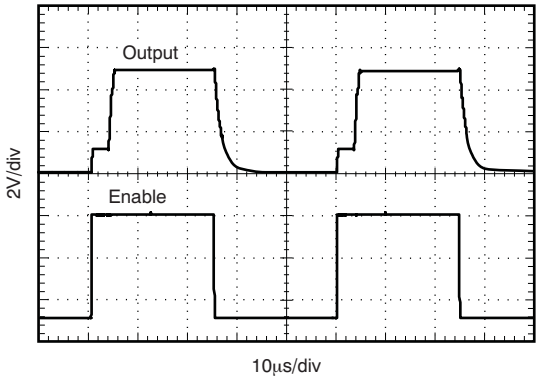


Figure 57.

SERIAL INTERFACE INFORMATION

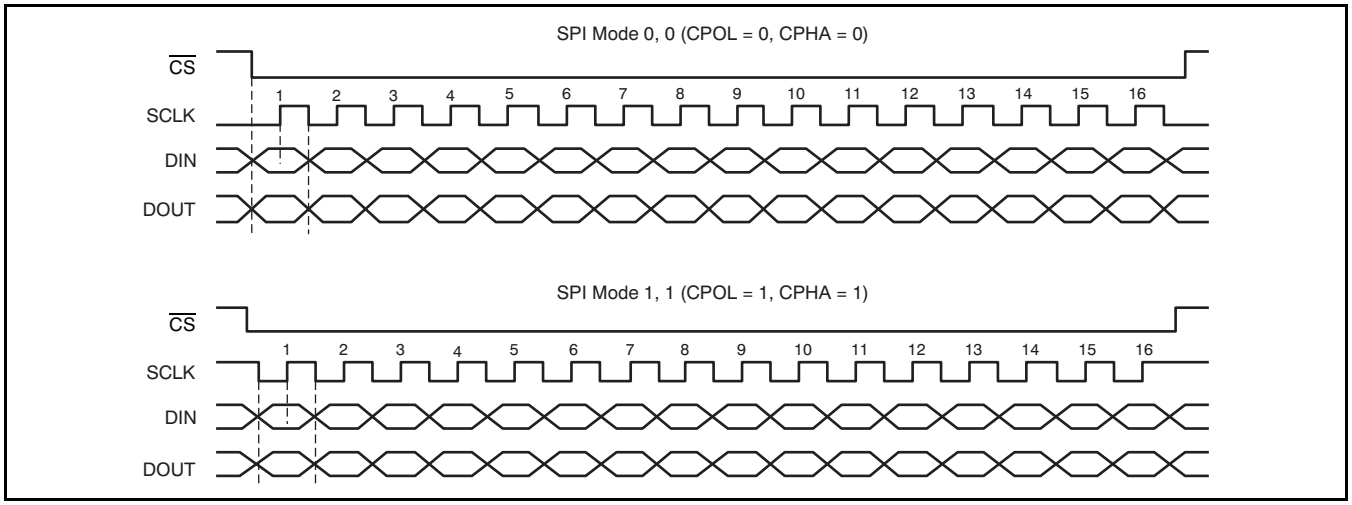


Figure 58. SPI Mode 0,0 and Mode 1,1

Table 2. SPI Mode Setting Description

MODE	CPOL	CPHA	CPOL DESCRIPTION	CPHA DESCRIPTION
0, 0	0	0(1)	Clock idles low	Data are read on the rising edge of clock. Data change on the falling edge of clock.
1, 1	1	1(2)	Clock idles high	Data are read on the rising edge of clock. Data change on the falling edge of clock.

(1) CPHA = 0 means sample on first clock edge (rising or falling) after a valid $\overline{CS}$.
(2) CPHA = 1 means sample on second clock edge (rising or falling) after a valid $\overline{CS}$.

SERIAL DIGITAL INTERFACE: SPI MODES

The PGA uses a standard serial peripheral interface (SPI). Both SPI Mode 0,0 and Mode 1,1 are supported, as shown in Figure 58 and described in Table 2.

If there are not even-numbered increments of 16 clocks (that is, 16, 32, 64, and so forth) between $\overline{CS}$ going low (falling edge) and $\overline{CS}$ going high (rising edge), the device takes no action. This condition provides reliable serial communication. Furthermore, this condition also provides a way to quickly reset the SPI interface to a known starting condition for data synchronization. Transmitted data are latched internally on the rising edge of $\overline{CS}$.

On the PGA116/PGA117, $\overline{CS}$, DIN, and SCLK are Schmitt-triggered CMOS logic inputs. DIN has a weak internal pull-down to support daisy-chain communications on the PGA116/PGA117. DOUT is a CMOS logic output. When $\overline{CS}$ is high, the state of DOUT is high-impedance. When $\overline{CS}$ is low, DOUT is driven as illustrated in Figure 59.

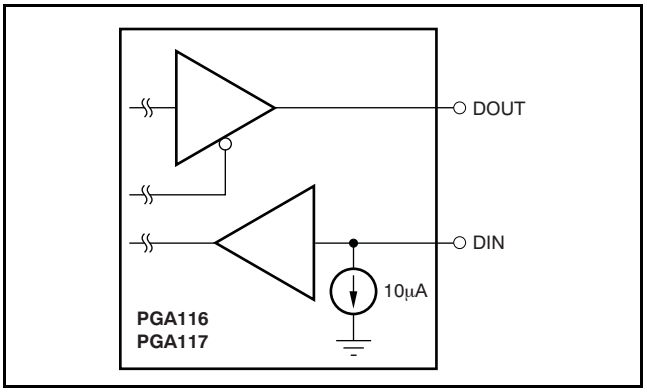


Figure 59. Digital I/O Structure—PGA116/PGA117

On the PGA112/PGA113, there are digital output and digital input gates both internally connected to the DIO pin. DIN is an input-only gate and DOUT is a digital output that can give a 3-state output. The DIO pin has a weak 10μA pull-down current source to prevent the pin from floating in systems with a high-impedance SPI DOUT line. When $\overline{CS}$ is high, the state of the internal DOUT gate is high-impedance. When $\overline{CS}$ is low, the state of DIO depends on the previous valid SPI communication; either DIO becomes an output to clock out data or it remains an input to receive data. This structure is shown in Figure 60.

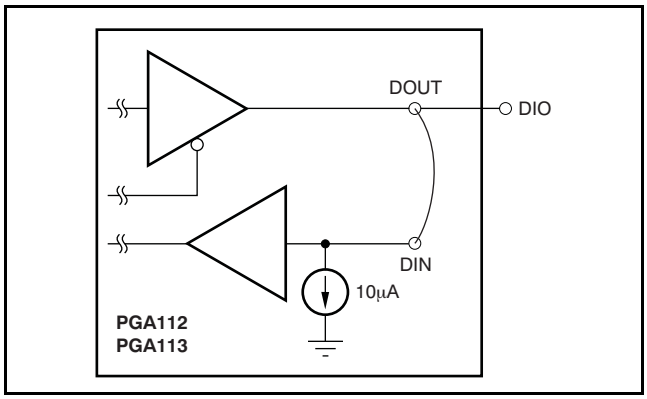


Figure 60. Digital I/O Structure—PGA112/PGA113

SERIAL DIGITAL INTERFACE: SPI DAISY-CHAIN COMMUNICATIONS

To reduce the number of I/O port pins used on a microcontroller, the PGA116/PGA117 support SPI daisy-chain communications with full read/write capability. A two-device daisy-chain configuration is shown in Figure 61, although any number of devices can be daisy-chained. The SPI daisy-chain communication uses a common SCLK and $\overline{CS}$ line for all devices in the daisy chain, rather than each device requiring a separate $\overline{CS}$ line. The daisy-chain mode of communication routes data serially through each device in the chain by using its respective DIN and DOUT pins as shown. Special commands are used (see Table 4) to ensure that data are written or read in the proper sequence. There is a special daisy-chain NOP command (No OPeration) which, when presented to the desired device in the daisy-chain, causes no changes in that respective device. Detailed timing diagrams for daisy-chain operation are shown in Figure 65 through Figure 67.

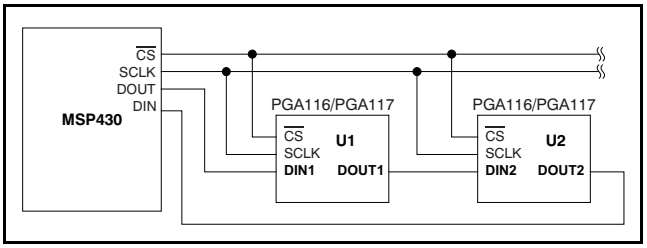


Figure 61. Daisy-Chain Read/Write Configuration

The PGA112/PGA113 can be used as the last device in a daisy-chain as shown in Figure 62 if *write-only* communication is acceptable, because the PGA112/PGA113 have no separate DOUT pin to connect back to the microcontroller DIN pin in order to read back data in this configuration.

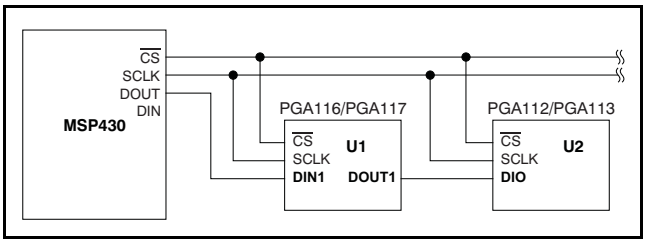


Figure 62. Daisy-Chain Write-Only Configuration

The maximum SCLK frequency that can be used in daisy-chain operation is directly related to SCLK rise/fall times, DIN setup time, and DOUT propagation delay. Any number of two or more devices have the same limitations because it is the timing considerations between adjacent devices that limit the clock speed.

Figure 63 analyzes the maximum SCLK frequency for daisy-chain mode based on the circuit of Figure 61. A clock rise and fall time of 10ns is assumed to allow for extra bus capacitance that could occur as a result of multiple devices in the daisy-chain.

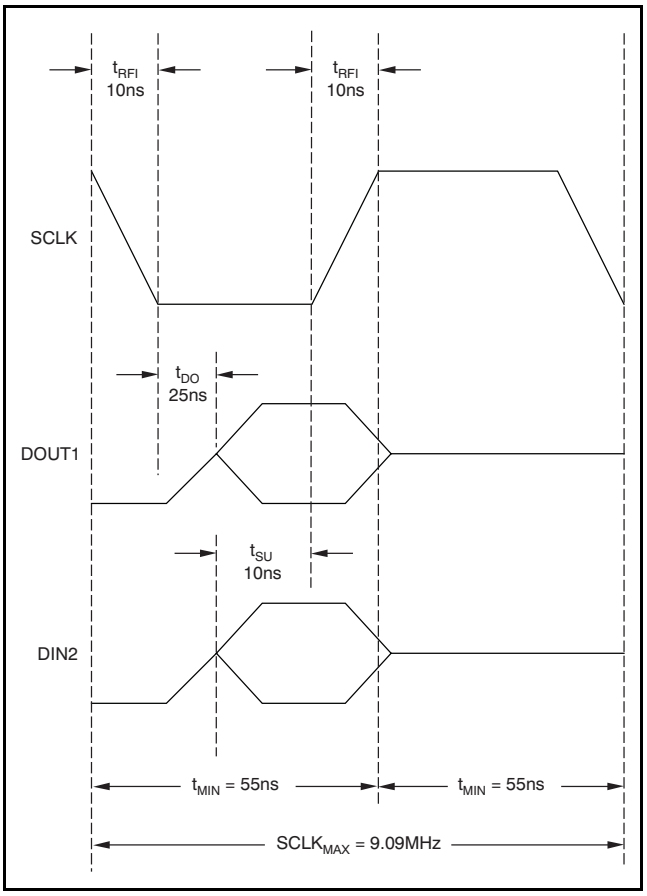


Figure 63. Daisy-Chain Maximum SCLK Frequency

SPI SERIAL INTERFACE

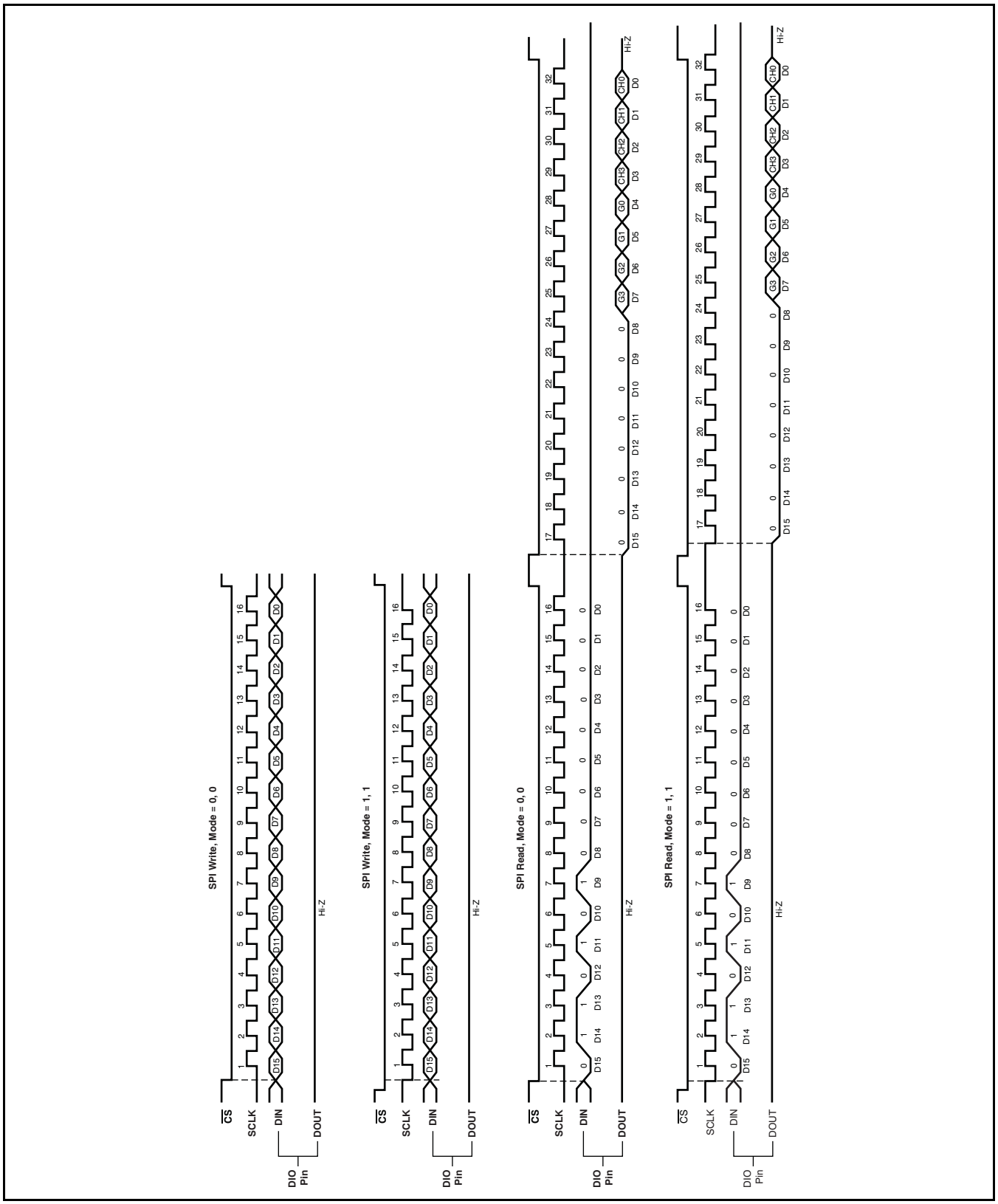


Figure 64. SPI Serial Interface Timing Diagrams

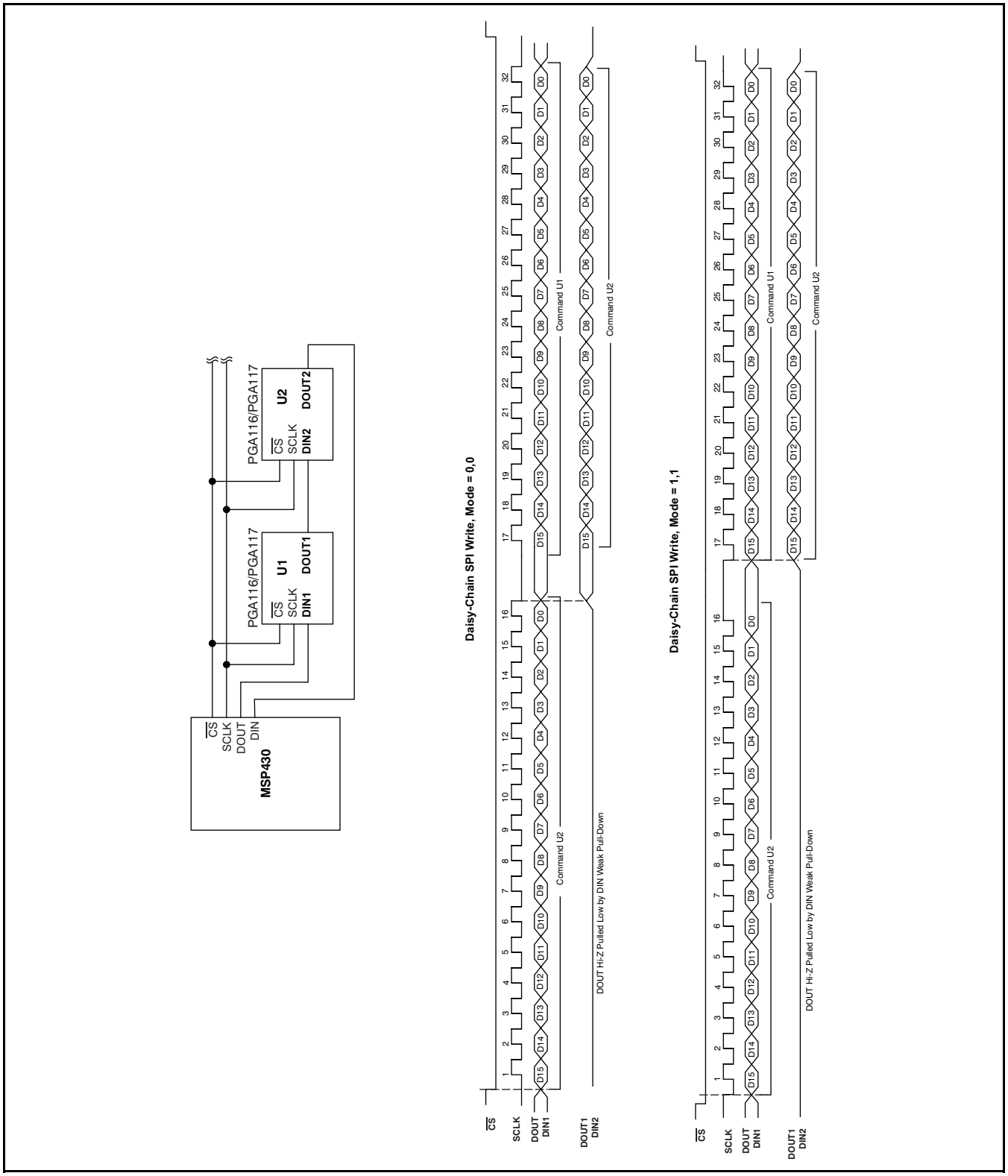


Figure 65. SPI Daisy-Chain Write Timing Diagrams

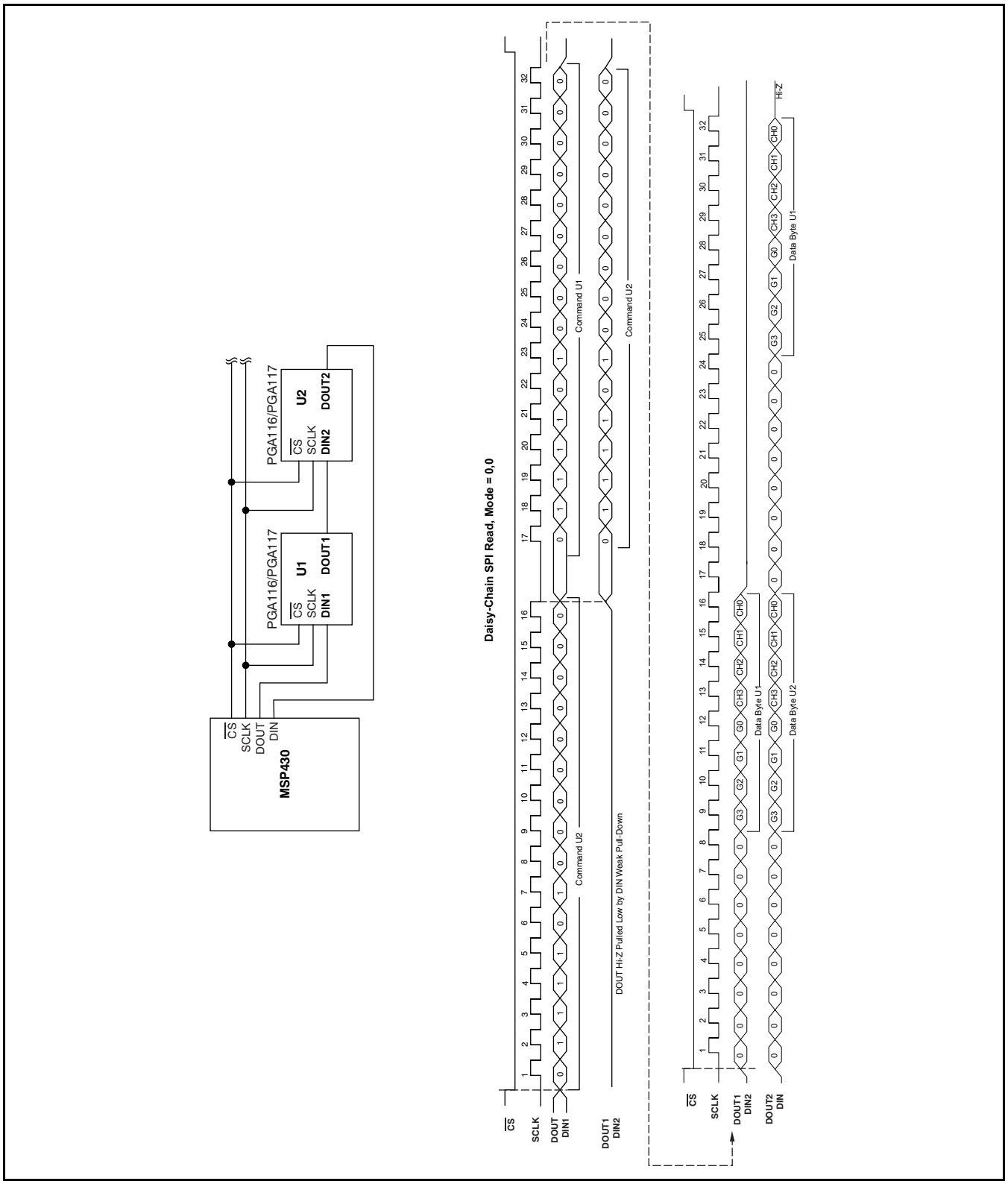


Figure 66. SPI Daisy-Chain Read Timing Diagram (Mode 0,0)

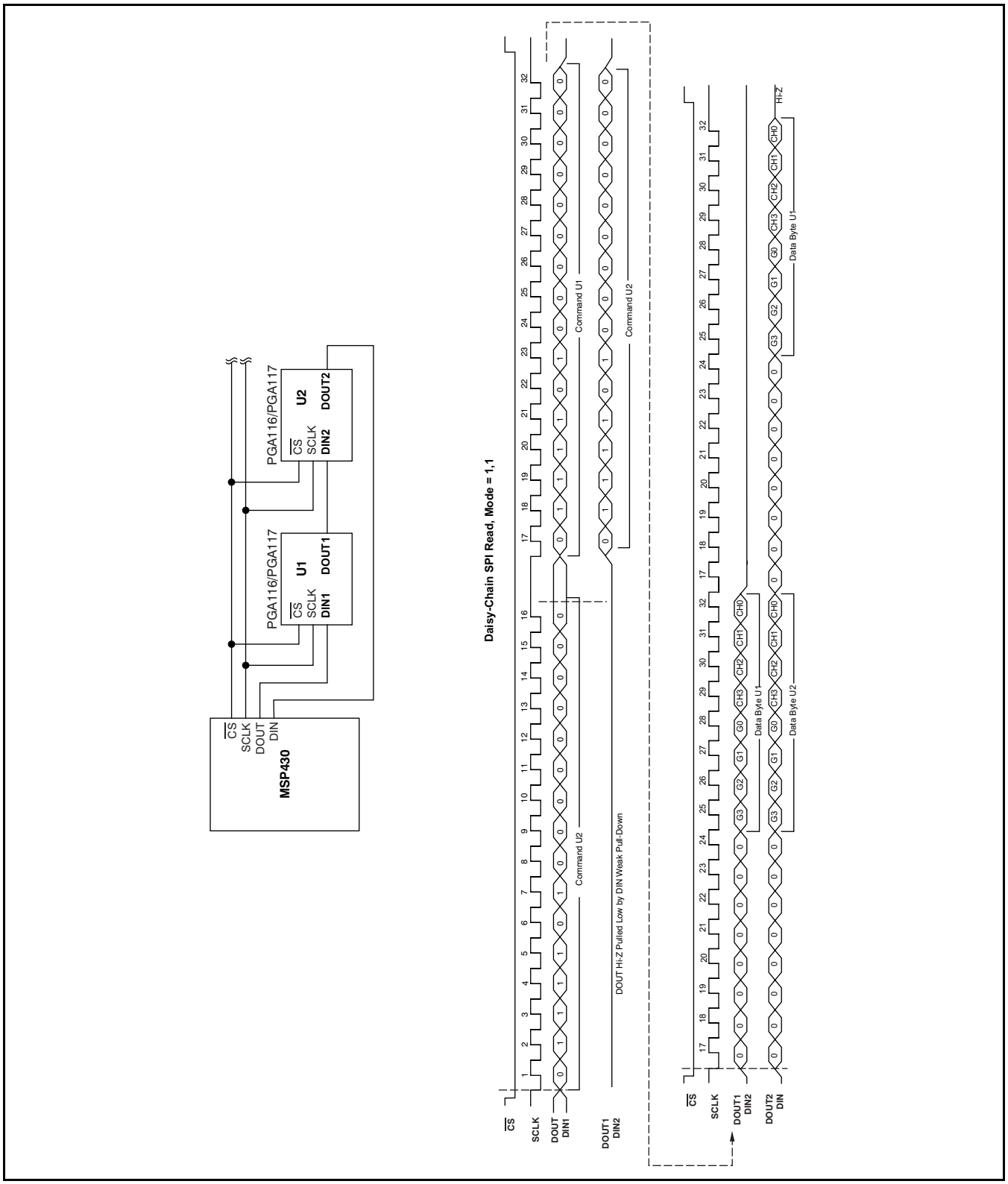


Figure 67. SPI Daisy-Chain Read Timing Diagram (Mode 1,1)

SPI COMMANDS

Table 3. SPI Commands (PGA112/PGA113)(1)(2)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	THREE-WIRE SPI COMMAND
0	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	READ
0	0	1	0	1	0	1	0	G3	G2	G1	G0	CH3	CH2	CH1	CH0	WRITE
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NOP WRITE
1	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	SDN_DIS WRITE
1	1	1	0	0	0	0	1	1	1	1	1	0	0	0	1	SDN_EN WRITE

(1) SDN = Shutdown mode. Enter Shutdown mode by issuing an SDN_EN command. Shutdown mode is cleared (returned to the last valid write configuration) by a SDN_DIS command or by any valid Write command.
(2) POR (Power-on-Reset) value of internal Gain/Channel Select Register is all 0s; this value sets Gain = 1, and Channel = V_{CAL}/CH0.

Table 4. SPI Daisy-Chain Commands(1)(2)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DAISY-CHAIN COMMAND
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	NOP
1	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	SDN_DIS
1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1	SDN_EN
0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	READ
0	0	1	1	1	0	1	0	G3	G2	G1	G0	CH3	CH2	CH1	CH0	WRITE

(1) SDN = Shutdown Mode. Shutdown Mode is entered by an SDN_EN command. Shutdown Mode is cleared (returned to the last valid write configuration) by a SDN_DIS command or by any valid Write command.
(2) POR (Power-on-Reset) value of internal Gain/Channel Register is all 0s; this value sets Gain = 1, V_{CAL}/CH0 selected.

Table 5. Gain Selection Bits (PGA112/PGA113)

G3	G2	G1	G0	BINARY GAIN	SCOPE GAIN
0	0	0	0	1	1
0	0	0	1	2	2
0	0	1	0	4	5
0	0	1	1	8	10
0	1	0	0	16	20
0	1	0	1	32	50
0	1	1	0	64	100
0	1	1	1	128	200

Table 6. Mux Channel Selection Bits

CH3	CH2	CH1	CH0	PGA112, PGA113	PGA116, PGA117
0	0	0	0	VCAL/CH0	VCAL/CH0
0	0	0	1	CH1	CH1
0	0	1	0	X(1)	CH2
0	0	1	1	X	CH3
0	1	0	0	X	CH4
0	1	0	1	X	CH5
0	1	1	0	X	CH6
0	1	1	1	X	CH7
1	0	0	0	X	CH8
1	0	0	1	X	CH9
1	0	1	0	X	X(1)
1	0	1	1	Factory Reserved	Factory Reserved
1	1	0	0	CAL1(2)	CAL1(2)
1	1	0	1	CAL2(3)	CAL2(3)
1	1	1	0	CAL3(4)	CAL3(4)
1	1	1	1	CAL4(5)	CAL4(5)

(1) X = channel is not used.
(2) CAL1: connects to GND.
(3) CAL2: connects to $0.9V_{CAL}$.
(4) CAL3: connects to $0.1V_{CAL}$.
(5) CAL4: connects to V_{REF}.

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The PGA112/PGA113 and PGA116/PGA117 are single-ended input, single-supply, programmable gain amplifiers (PGAs) with an input multiplexer. Multiplexer channel selection and gain selection are done through a standard SPI interface. The PGA112/PGA113 have a two-channel input MUX and the PGA116/PGA117 have a 10-channel input MUX. The PGA112 and PGA116 provide binary gain selections (1, 2, 4, 8, 16, 32, 64, 128) and the PGA113 and PGA117 provide scope gain selections (1, 2, 5, 10, 20, 50, 100, 200). All models use a split-supply architecture with an analog supply, AV_{DD}, and a digital supply, DV_{DD}. This split-supply architecture allows for ease of interface to analog-to-digital converters (ADCs) and microcontrollers in mixed-supply voltage systems, such as where the analog supply is +5V and the digital supply is +3V. Four internal calibration channels are provided for system-level calibration. The channels are tied to GND, $0.9V_{CAL}$, $0.1V_{CAL}$, and V_{REF}, respectively. V_{CAL}, an external voltage connected to V_{CAL}/CH0, acts as the system calibration reference. If V_{CAL} is the system ADC reference, then gain and offset calibration on the ADC are easily accomplished through the PGA using only one MUX input. If calibration is not used, then V_{CAL}/CH0 can be used as a standard MUX input. All four versions provide a V_{REF} pin that can be tied to ground or, for ease of scaling, to midsupply in single-supply systems where midsupply is used as a virtual ground. The PGA112/PGA113 offer a software-controlled shutdown feature for low standby power. The PGA116/PGA117 offer both hardware- and software-controlled shutdown for low standby power. The PGA112/PGA113 have a three-wire SPI digital interface; the PGA116/PGA117 have a four-wire SPI digital interface. The PGA116/117 also have daisy-chain capability.

OP AMP: INPUT STAGE

The PGA op amp is a rail-to-rail input and output (RRIO) single-supply op amp. The input topology uses two separate input stages in parallel to achieve rail-to-rail input. As Figure 68 shows, there is a PMOS transistor on each input for operation down to ground; there is also an NMOS transistor on each input in parallel for operation to the positive supply rail. When the common-mode input voltage (that is, the single-ended input, because this PGA is configured internally for noninverting gain) crosses a level that is typically about 1.5V below the positive supply, there is a transition between the NMOS and PMOS transistors. The result of this transition appears as a small input offset voltage transition that is reflected to the output by the selected PGA gain. This transition may be either increasing or decreasing, and differs from part to part as described in Figure 69 and Figure 70. These figures illustrate possible differences in input offset voltage between two different devices when used with AV_{DD} = +5V. Because the exact transition region varies from device to device, the Electrical Characteristics table specifies an input offset voltage above and below this input transition region.

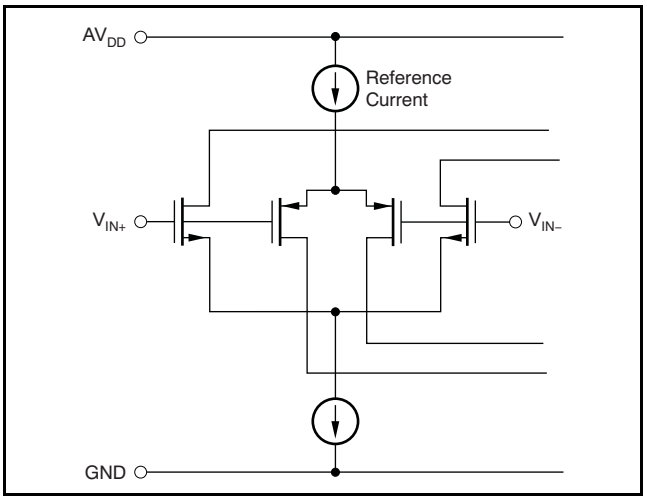


Figure 68. PGA Rail-to-Rail Input Stage

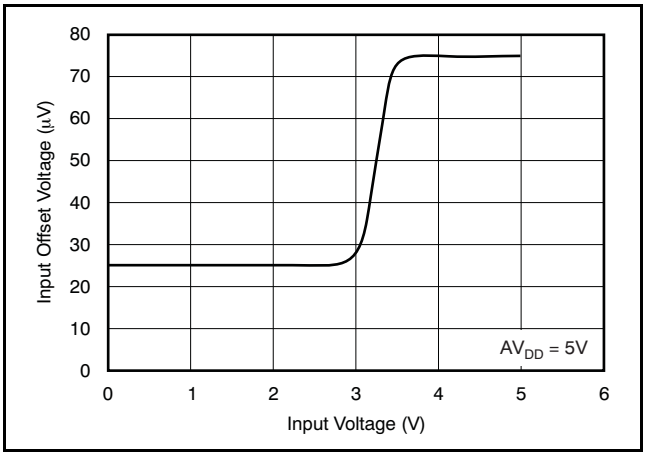


Figure 69. V_{OS} versus Input Voltage—Case 1

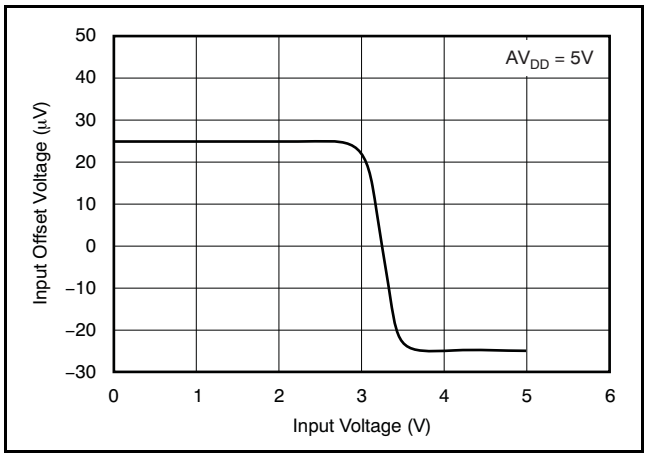


Figure 70. V_{OS} versus Input Voltage—Case 2

OP AMP: GENERAL GAIN EQUATIONS

Figure 71 shows the basic configuration for using the PGA as a gain block. V_{OUT}/V_{IN} is the selected noninverting gain, depending on the model selected, for either binary or scope gains.

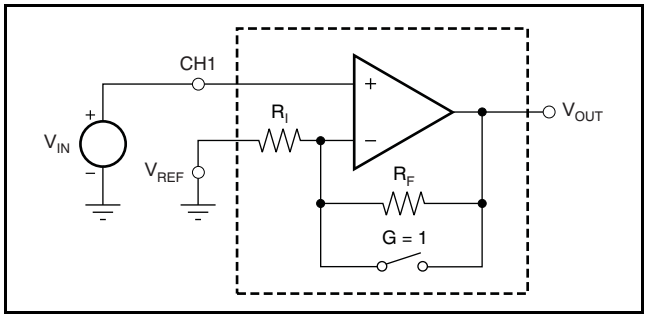


Figure 71. PGA Used as a Gain Block

$$V_{OUT} = G \times V_{IN} \quad (1)$$

Where:

G = 1, 2, 4, 8, 16, 32, 64, and 128 (binary gains)

G = 1, 2, 5, 10, 20, 50, 100, and 200 (scope gains)

Figure 72 shows the PGA configuration and gain equations for $V_{REF} = AV_{DD}/2$. V_{OUT0} is V_{OUT} when CH0 is selected and V_{OUT1} is V_{OUT} when CH1 is selected. Notice the V_{REF} pin has no effect for G = 1 because the internal feedback resistor, R_F, is shorted out. This configuration allows for positive and negative voltage excursions around a midsupply virtual ground.

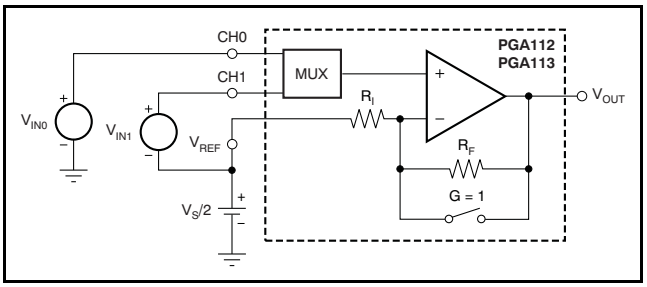


Figure 72. PGA112/PGA113 Configuration for Positive and Negative Excursions Around Midsupply Virtual Ground

$$V_{OUT0} = G \times V_{IN0} - AV_{DD}/2 \times (G - 1) \quad (2)$$

When: G = 1

Then: $V_{OUT0} = G \times V_{IN0}$

$$V_{OUT1} = G \times (V_{IN1} + AV_{DD}/2) - AV_{DD}/2 \times (G - 1)$$
$$V_{OUT1} = G \times V_{IN1} + AV_{DD}/2, \text{ where: } -AV_{DD}/2 < G \times V_{IN1} < +AV_{DD}/2 \quad (3)$$

Where:

G = 1, 2, 4, 8, 16, 32, 64, and 128 (binary gains)

G = 1, 2, 5, 10, 20, 50, 100, and 200 (scope gains)

Table 7 details the internal typical values for the op amp internal feedback resistor (R_F) and op amp internal input resistor (R_I) for both binary and scope gains.

Table 7. Typical R_F and R_I versus Gain

Binary Gain (V/V)	R_F (Ω)	R_I (Ω)	Scope Gain (V/V)	R_F (Ω)	R_I (Ω)
1	0	3.25k	1	0	3.25k
2	3.25k	3.25k	2	3.25k	3.25k
4	9.75k	3.25k	5	13k	3.25k
8	22.75k	3.25k	10	29.25k	3.25k
16	48.75k	3.25k	20	61.75k	3.25k
32	100.75k	3.25k	50	159.25k	3.25k
64	204.75k	3.25k	100	321.75k	3.25k
128	412.75k	3.25k	200	646.75k	3.25k

OP AMP: FREQUENCY RESPONSE VERSUS GAIN

Table 8 documents how small-signal bandwidth and slew rate change correspond to changes in PGA gain.

Full power bandwidth (that is, the highest frequency that a sine wave can pass through the PGA for a given gain) is related to slew rate by Equation 4:

$$SR\ (V/\mu s) = 2\pi f \times V_{OP}\ (1 \times 10^{-6}) \quad (4)$$

Where:

SR = Slew rate in V/µs

f = Frequency in Hz

V_{OP} = Output peak voltage in volts

Example:

For G = 8, then SR = 10.6V/µs (slew rate rise is minimum slew rate).

For a 5V system, choose 0.1V < V_{OUT} < 4.9V or V_{OUTPP} = 4.8V or V_{OUTP} = 2.4V.

SR (V/µs) = $2\pi f \times V_{OP}\ (1 \times 10^{-6})$.

$10.6 = 2\pi f\ (2.4)\ (1 \times 10^{-6}) \rightarrow f = 702.9kHz$

This example shows that a G = 8 configuration can produce a $4.8V_{PP}$ sine wave with frequency up to 702.9kHz. This computation only shows the theoretical upper limit of frequency for this example, but does not indicate the distortion of the sine wave. The acceptable distortion depends on the specific application. As a general guideline, maintain two to three times the calculated slew rate to minimize distortion on the sine wave. For this example, the application should only use G = 8, $4.8V_{PP}$, up to a frequency range of 234kHz to 351kHz, depending upon the acceptable distortion. For a given gain and slew rate requirement, check for adequate small-signal bandwidth (typical –3dB frequency) in order to assure that the frequency of the signal can be passed without attenuation.

ANALOG MUX

The analog input MUX provides two input channels for the PGA112/PGA113 and 10 input channels for the PGA116/PGA117. The MUX switches are designed to be break-before-make and thereby eliminate any concerns about shorting the two input signal sources together.

Four internal MUX CAL channels are included in the analog MUX for ease of system calibration. These CAL channels allow ADC gain and offset errors to be calibrated out. This calibration does not remove the offset and gain errors of the PGA for gains greater than 1, but most systems should see a significant increase in the ADC accuracy. In addition, these CAL channels can be used by the ADC to read the minimum and maximum possible voltages from the PGA. With these minimum and maximum levels known, the system architecture can be designed to indicate an out-of-range condition on the measured analog input signals if these levels are ever measured.

To use the CAL channels, V_{CAL}/CH0 must be permanently connected to the system ADC reference. There is a typical 100kΩ load from V_{CAL}/CH0 to ground. Table 9 illustrates how to use the CAL channels with V_{REF} = ground. Table 10 describes how to use the CAL channels with V_{REF} = AV_{DD}/2. The V_{REF} pin must be connected to a source that is low-impedance for both dc and ac in order to maintain gain and nonlinearity accuracy. Worst-case current demand on the V_{REF} pin occurs when G = 1 because there is a 3.25kΩ resistor between V_{OUT} and V_{REF}. For a 5V system with AV_{DD}/2 = 2.5V, the V_{REF} pin buffer must source and sink 2.5V/3.25kΩ = 0.7mA minimum for a V_{OUT} that can swing from ground to +5V.

Table 8. Frequency Response versus Gain (C_L = 100pF, R_L= 10kΩ)

BINARY GAIN (V/V)	TYPICAL –3dB FREQUENCY (MHz)	SLEW RATE-FALL (V/µs)	SLEW RATE-RISE (V/µs)	0.1% SETTLING TIME: $4V_{PP}$ (µs)	0.01% SETTLING TIME: $4V_{PP}$ (µs)	SCOPE GAIN (V/V)	TYPICAL –3dB FREQUENCY (MHz)	SLEW RATE-FALL (V/µs)	SLEW RATE-RISE (V/µs)	0.1% SETTLING TIME: $4V_{PP}$ (µs)	0.01% SETTLING TIME: $4V_{PP}$ (µs)
1	10	8	3	2	2.55	1	10	8	3	2	2.55
2	3.8	9	6.4	2	2.6	2	3.8	9	6.4	2	2.6
4	2	12.8	10.6	2	2.6	5	1.8	12.8	10.6	2	2.6
8	1.8	12.8	10.6	2	2.6	10	1.8	12.8	10.6	2.2	2.6
16	1.6	12.8	12.8	2.3	2.6	20	1.3	12.8	9.1	2.3	2.8
32	1.8	12.8	13.3	2.3	3	50	0.9	9.1	7.1	2.4	3.8
64	0.6	4	3.5	3	6	100	0.38	4	3.5	4.4	7
128	0.35	2.5	2.5	4.8	8	200	0.23	2.3	2	6.9	10

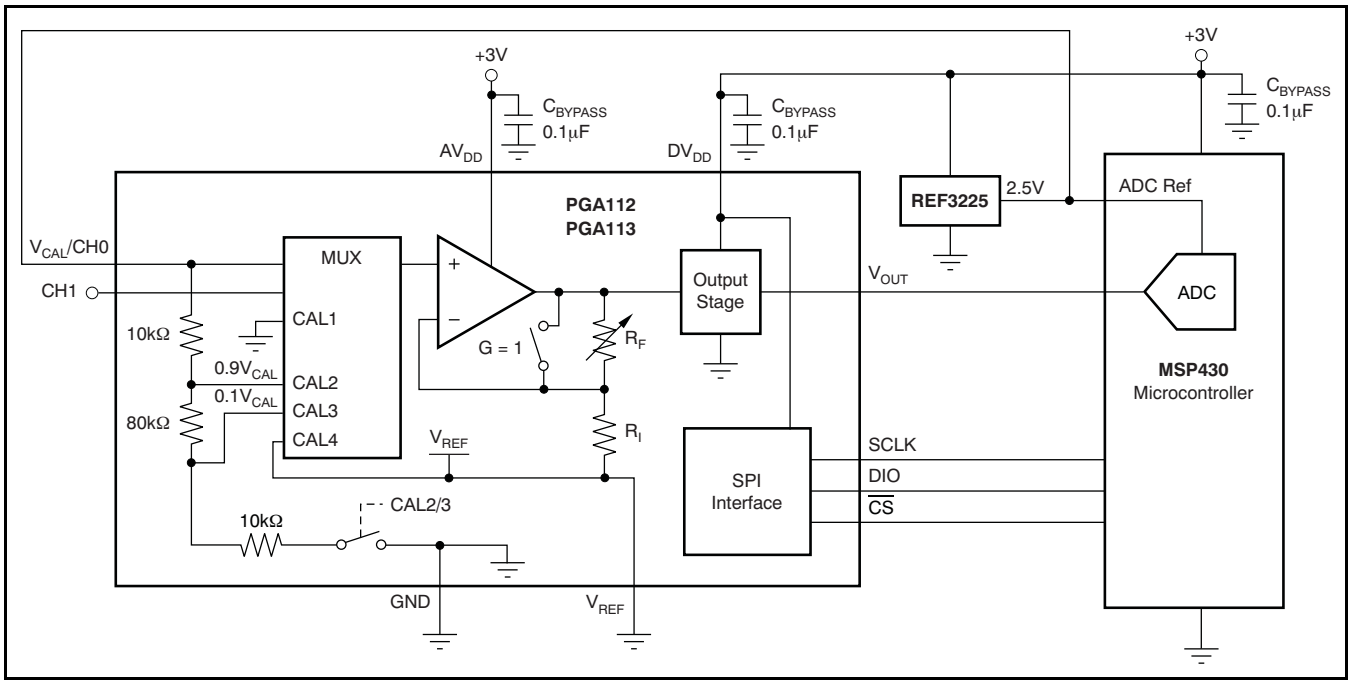


Figure 73. Using CAL Channels with V_{REF} = Ground

Table 9. Using the MUX CAL Channels with V_{REF} = GND (AV_{DD} = 3V, DV_{DD} = 3V, ADC Ref = 2.5V, and V_{REF} = GND)

FUNCTION	MUX SELECT	GAIN SELECT	MUX INPUT	OP AMP (+In)	OP AMP (V_{OUT})	DESCRIPTION
Minimum Signal	CAL1	1	GND	GND	50mV	Minimum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by negative saturation.
Gain Calibration	CAL2	1	0.9 × (V_{CAL}/CH0)	2.25V	2.25V	90% ADC Ref for system full-scale or gain calibration of the ADC.
Maximum Signal	CAL2	2	0.9 × (V_{CAL}/CH0)	2.25V	2.95V	Maximum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by positive saturation. System is limited by ADC max input of 2.5V (ADC Ref = 2.5V).
Offset Calibration	CAL3	1	0.1 × (V_{CAL}/CH0)	0.25V	0.25V	10% ADC Ref for system offset calibration of the ADC.
Minimum Signal	CAL4	1	V_{REF}	GND	50mV	Minimum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by negative saturation.

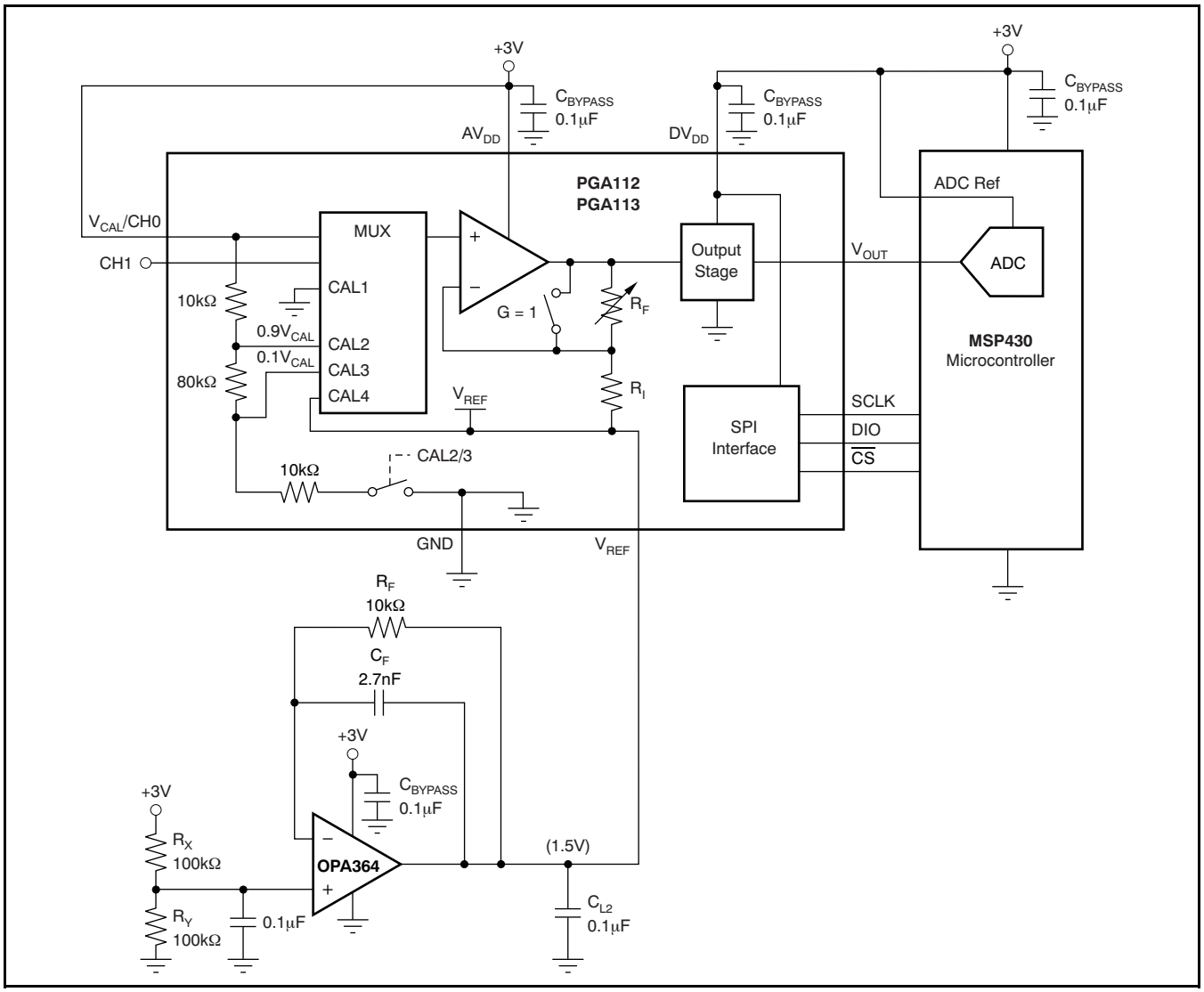


Figure 74. Using CAL Channels with V_{REF} = AV_{DD}/2

Table 10. Using the MUX CAL Channels with V_{REF} = AV_{DD}/2 (AV_{DD} = 3V, DV_{DD} = 3V, ADC Ref = 3V, and V_{REF} = 1.5V)

FUNCTION	MUX SELECT	GAIN SELECT	MUX INPUT	OP AMP (+In)	OP AMP (V_{OUT})	DESCRIPTION
Minimum Signal	CAL1	1	GND	GND	50mV	Minimum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by negative saturation.
Gain Calibration	CAL2	1	0.9 × (V_{CAL}/CH0)	2.7V	2.7V	90% ADC Ref for system full-scale or gain calibration of the ADC.
Maximum Signal	CAL2	4 or 5	0.9 × (V_{CAL}/CH0)	2.25V	2.95V	Maximum signal level that the MUX, op amp, and ADC can read. Op amp V_{OUT} is limited by positive saturation.
Offset Calibration	CAL3	1	0.1 × (V_{CAL}/CH0)	0.3V	0.3V	10% ADC Ref for system offset calibration of the ADC.
V_{REF} Check	CAL4	1	V_{REF}	1.5V	1.5V	Midsupply voltage used as V_{REF}.

SYSTEM CALIBRATION USING THE PGA

Analog-to-digital converters (ADCs) contain two major errors that can be easily removed by calibration at a system level. These errors are gain error and offset error, as shown in Figure 75. Figure 75 shows a typical transfer function for a 12-bit ADC. The analog input is on the x-axis with a range from 0V to (V_{REF_ADC} – 1LSB), where V_{REF_ADC} is the ADC reference voltage. The y-axis is the hexadecimal equivalent of the digital codes that result from ADC conversions. The dotted red line represents an ideal transfer function with *0000h* representing 0V analog input and *0FFFh* representing an analog input of (V_{REF_ADC} – 1LSB). The solid blue line illustrates the offset error. Although the solid blue line includes both offset error and gain error, at an analog input of 0V the offset error voltage, V_{Z_ACTUAL}, can be measured. The dashed black line represents the transfer function with gain error. The dashed black line is equivalent to the solid blue line without the offset error, and can be measured and computed using V_{Z_ACTUAL} and V_{Z_IDEAL}. The difference between the dashed black line and the dotted red line is the gain error. Gain and offset error can be computed by taking zero input and full-scale input readings. Using these error calculations, compute a calibrated ADC reading to remove the ADC gain and offset error.

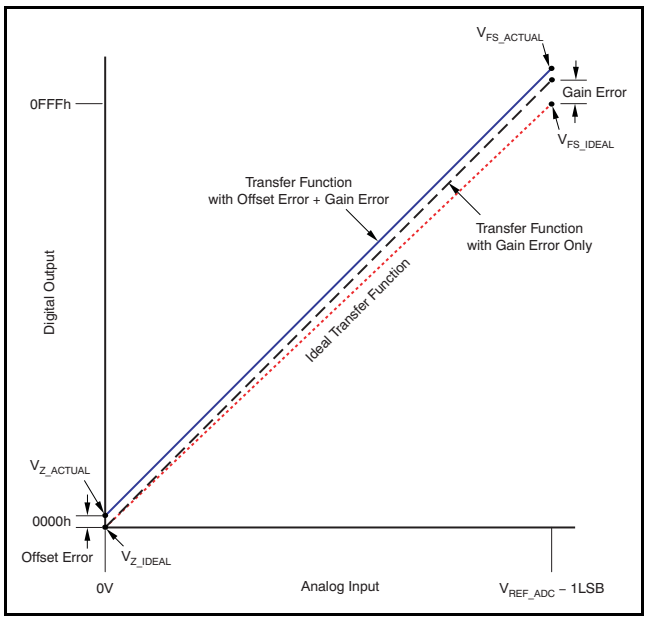


Figure 75. ADC Offset and Gain Error

In practice, the zero input (0V) or full-scale input (V_{REF_ADC} – 1LSB) of ADCs cannot always be measured because of internal offset error and gain error. However, if measurements are made very close to the full-scale input and the zero input, both zero and full-scale can be calibrated very accurately with the assumption of linearity from the calibration points to the desired end points of the ADC ideal transfer function. For the zero calibration, choose $10\%V_{REF\_ADC}$; this value should be above the internal offset error and sufficiently out of the noise floor range of the ADC. For the gain calibration, choose $90\%V_{REF\_ADC}$; this value should be less than the internal gain error and sufficiently below the tolerance of V_{REF}. These key points can be summarized in this way:

For zero calibration:

- The ADC cannot read the ideal zero because of offset error
- Must be far enough above ground to be above noise floor and ADC offset error
- Therefore, choose $10\%V_{REF\_ADC}$ for zero calibration

For gain calibration:

- The ADC cannot read the ideal full-scale because of gain error
- Must be far enough below full-scale to be below the V_{REF} tolerance and ADC gain error
- Therefore, choose $90\%V_{REF\_ADC}$ for gain calibration

The 12-bit ADC example in Figure 76 illustrates the technique for calibrating an ADC using a $10\%V_{REF\_ADC}$ and $90\%V_{REF\_ADC}$ reading where V_{REF_ADC} is the ADC reference voltage. Note that the $10\%V_{REF}$ reading also contains a gain error because it is not a V_{IN} = 0 calibration point. First, use the $90\%V_{REF}$ and $10\%V_{REF}$ points to compute the measured gain error. The measured gain error is then used to remove the gain error from the $10\%V_{REF}$ reading, giving a measured $10\%V_{REF}$ number. The measured $10\%V_{REF}$ number is used to compute the measured offset error.

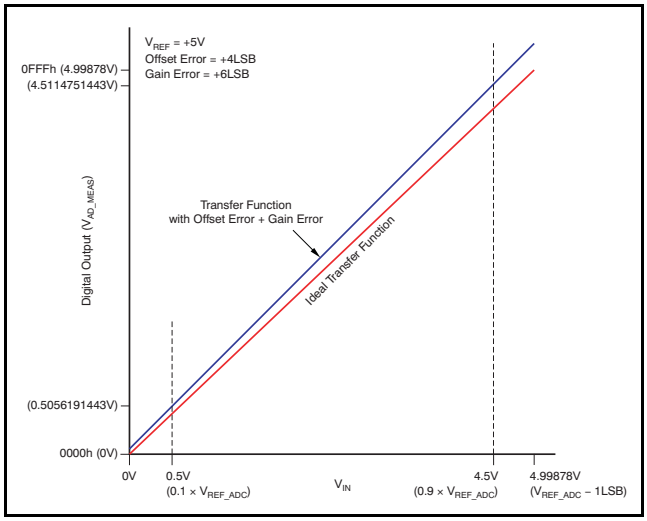


Figure 76. 12-Bit Example of ADC Calibration for Gain and Offset Error

The gain error and offset error in ADC readings can be calibrated by using $10\%V_{REF\_ADC}$ and $90\%V_{REF\_ADC}$ calibration points. Because the calibration is ratiometric to V_{REF_ADC}, the exact value of V_{REF_ADC} does not need to be known in the end application.

Follow these steps to compute a calibrated ADC reading:

1. Take the ADC reading at $V_{IN} = 90\% \times V_{REF}$ and $V_{IN} = 10\% \times V_{REF}$. The ADC readings for $10\%V_{REF}$ and $90\%V_{REF}$ are taken.

$$V_{REF}90 = 0.9(V_{REF\_ADC}) \quad (5)$$

$$V_{REF}10 = 0.1(V_{REF\_ADC}) \quad (6)$$

$$V_{MEAS}90 = ADC_{MEASUREMENT} \text{ at } V_{REF}90 \quad (7)$$

$$V_{MEAS}10 = ADC_{MEASUREMENT} \text{ at } V_{REF}10 \quad (8)$$

2. Compute the ADC measured gain. The slope of the curve connecting the measured $10\%V_{REF}$ and measured $90\%V_{REF}$ point is computed and compared to the slope between the ideal $10\%V_{REF}$ and ideal $90\%V_{REF}$. This result is the measured gain.

$$G_{MEAS} = \frac{V_{MEAS}90 - V_{MEAS}10}{V_{REF}90 - V_{REF}10} \quad (9)$$

3. Compute the ADC measured offset. The measured offset is computed by taking the difference between the measured $10\%V_{REF}$ and the (ideal $10\%V_{REF}$) × (measured gain).

$$O_{MEAS} = V_{MEAS}10 - (V_{REF}10 \times G_{MEAS}) \quad (10)$$

4. Compute the calibrated ADC readings.

$$V_{AD\_MEAS} = \text{Any } V_{IN}\ ADC_{MEASUREMENT} \quad (11)$$

$$V_{ADC\_CAL} = \frac{V_{AD\_MEAS} - O_{MEAS}}{G_{MEAS}} \quad (12)$$

Any ADC reading can therefore be calibrated by removing the gain error and offset error. The measured offset is subtracted from the ADC reading and then divided by the measured gain to give a corrected reading. If this calibration is performed on a timed basis, relative to the specific application, gain and offset error over temperature are also removed from the ADC reading by calibration.

For example; given:

- 12-Bit ADC
- ADC Gain Error = +6LSB
- ADC Offset Error = +4LSB
- ADC Reference (V_{REF_ADC}) = +5V
- Temperature = +25°C

Table 11 shows the resulting system accuracy.

Table 11. Bits of System Accuracy(1) (to 0.5LSB)

V_{IN}	ADC ACCURACY WITHOUT CALIBRATION	ADC ACCURACY WITH PGA112 CALIBRATION
$10\%V_{REF\_ADC}$	8.80 Bits	12.80 Bits
$90\%V_{REF\_ADC}$	7.77 Bits	11.06 Bits

(1) Difference in maximum input offset voltage for $V_{IN} = 10\%V_{REF\_ADC}$ and $V_{IN} = 90\%V_{REF\_ADC}$ is the reason for different accuracies.

APPLICATIONS: GENERAL-PURPOSE INPUT SCALING

Figure 77 is an example application that demonstrates the flexibility of the PGA for general-purpose input scaling. V_{IN0} is a ±100mV input that is ac-coupled into CH0. The PGA112/PGA113 is powered from a +5V supply voltage, V_S, and configured with the V_{REF} pin connected to $V_S/2$ (+2.5V). V_{CH0} is the ±100mV input, level-shifted and centered on $V_S/2$ (+2.5V). A gain of 20 is applied to CH0, and because of the PGA113 configuration, the output voltage at V_{OUT} is ±2V centered on $V_S/2$ (+2.5V).

CH1 is set to G = 1; through a resistive divider and scalar network, we can read ±5V or 0V. This setting provides bipolar to single-ended input scaling.

Table 12 summarizes the scaling resistor values for R_A, R_X, and R_B for different ADC Ref voltages. V_{REF_ADC} is the reference voltage used for the ADC connected to the PGA112/PGA113 output. It is assumed the ADC input range is 0V to V_{REF_ADC}. The *Bipolar Input to Single-Supply Scaling* section gives the algorithm to compute resistor values for references not listed in Table 12. As a general guideline, R_B should be chosen such that the input on-channel current multiplied by R_B is less than or equal to the input offset voltage. This value ensures that the scaling network contributes no more error than the input offset voltage. Individual applications may require other design trade-offs.

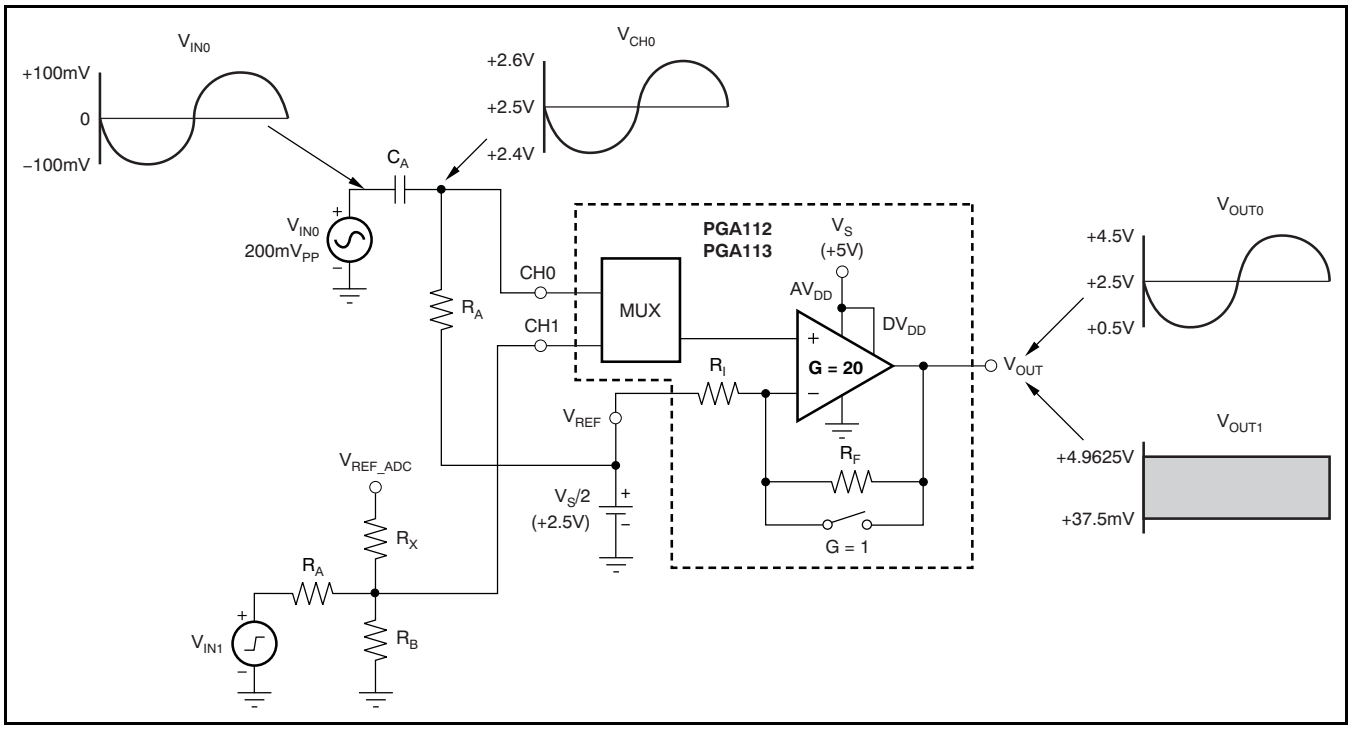


Figure 77. General-Purpose Input Scaling

Table 12. Bipolar to Single-Ended Input Scaling(1)(2)

V_{REF_ADC} (V)	V_{IN1} (V)	CH1 INPUT	R_A (kΩ)	R_X (Ω)	R_B (kΩ)
2.5	–5	0.047613	9.2	4.81k	10
	0	1.247613			
	5	2.447613			
2.5	–10	0.050317	3.16	2.4k	10
	0	1.250317			
	10	2.450317			
3	–5	0.058003	13.5	5.76k	10
	0	1.498003			
	5	2.938003			
3	–10	0.059303	4.02	2.87k	10
	0	1.499303			
	10	2.939303			
4.096	–5	0.082224	37	7.87k	10
	0	2.048304			
	5	4.014384			
4.096	–10	0.086018	6.49	3.92k	10
	0	2.052098			
	10	4.018178			
5	–5	0.093506	24	965	10
	0	2.493506			
	5	4.893506			
5	–10	0.095227	9.2	4.81k	10
	0	2.495227			
	10	4.895227			

(1) Scaling is based on 0.02(V_{REF_ADC}) to 0.98(V_{REF_ADC}), using standard 0.1% resistor values.
(2) Assumes symmetrical V_{IN} and symmetrical scaling for CH1 input minimum and maximum.

Bipolar Input to Single-Supply Scaling

Note that this process assumes a symmetrical V_{IN1} and that symmetrical scaling is used for CH1 input minimum and maximum values. The following steps give the algorithm to compute resistor values for references not listed in Table 12.

Step 1: Choose the following:

a. V_{REF_ADC} = 2.5V (ADC reference voltage)

b. $|V_{IN1}| = 5$

(magnitude of V_{IN}, assuming scaling is for $\pm V_{IN1}$)

c. Choose R_B as a standard resistor value. The input on-channel current multiplied by R_B should be less than the input offset voltage, such that R_B is not a major source of inaccuracy.

R_B = 10kΩ (select as a starting value for resistors)

d. For the most negative V_{IN1}, choose the percentage (in decimal format) of V_{REF_ADC} desired at the ADC input.

k_{VO-} = 0.02

(CH1 input = $k_{VO-} \times V_{REF\_ADC}$ when $V_{IN1} = -V_{IN1}$)

e. For the most positive V_{IN1}, choose the percentage (in decimal format) of V_{REF_ADC} desired at the ADC input. Since this scaling is based on symmetry, k_{VO+} must be the same percentage away from V_{REF_ADC} at the upper limit as at the lower limit where k_{VO-} is computed.

$k_{VO+} = 1 - k_{VO-}$

$k_{VO+} = 1 - 0.02 = 0.98$

(CH1 input = $k_{VO+} \times V_{REF\_ADC}$ when $V_{IN1} = +V_{IN1}$)

Step 2: Compute the following:

a. To simplify analysis, create one constant called k_{VO}.

$k_{VO} = k_{VO+} - k_{VO-}$

$0.96 = 0.98 - 0.02$

b. A constant, g, is created to simplify resistor value computations.

$$g = \frac{k_{VO} \times V_{REF\_ADC}}{2 \times |V_{IN1}| - k_{VO} \times V_{REF\_ADC}}$$

$$0.315789474 = \frac{0.96 \times 2.5}{2 \times 5 - 0.96 \times 2.5}$$

c. R_A is now selected from the starting value of R_B and the g constant.

$$R_A = \frac{2 \times R_B \times g}{1 - g}$$

$$9.23077k\Omega = \frac{2 \times 10k\Omega \times 0.315789474}{1 - 0.315789474}$$

d. R_X can now be computed from the starting value of R_B and the computed value for R_A.

$$R_X = \frac{R_B \times R_A}{R_B + R_A}$$

$$4.81k\Omega = \frac{10k\Omega \times 9.23077k\Omega}{10k\Omega + 9.23077k\Omega}$$

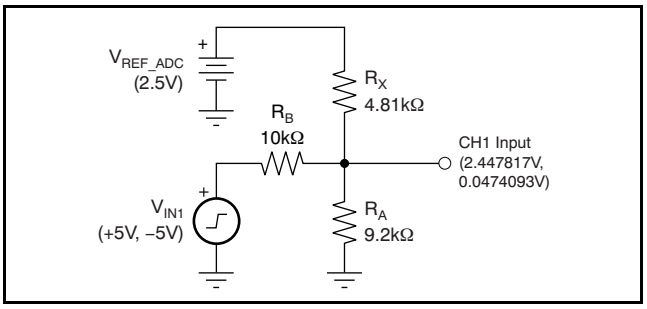


Figure 78. Bipolar to Single-Ended Input Algorithm

APPLICATIONS: HIGH GAIN/WIDE BANDWIDTH CONSIDERATIONS

As a result of the combination of wide bandwidth and high gain capability of the PGA112/PGA113 and PGA116/PGA117, there are several printed circuit board (PCB) design and system recommendations to consider for optimum application performance.

1. **Power-supply bypass.** Bypass each power-supply pin separately. Use a ceramic capacitor connected directly from the power-supply pin to the ground pin of the IC on the same PCB plane. Vias can then be used to connect to ground and voltage planes. This configuration keeps parasitic inductive paths out of the local bypass for the PGA. Good analog design practice dictates the use of a large value tantalum bypass capacitor on the PCB for each respective voltage.

2. **Signal trace routing.** Keep V_{OUT} and other low impedance traces away from MUX channel inputs that are high impedance. Poor signal routing can cause positive feedback, unwanted oscillations, or excessive overshoot and ringing on step-changing signals. If the input signals are particularly noisy, separate MUX input channels with guard traces on either side of the signal traces. Connect the guard traces to ground near the PGA and at the signal entry point into the PCB. On multilayer PCBs, ensure that there are no parallel traces near MUX input traces on adjacent layers; capacitive coupling from other layers can be a problem. Use ground planes to isolate MUX input signal traces from signal traces on other layers.

   Additionally, group and route the digital signals into the PGA as far away as possible from the analog MUX input signals. Most digital signals are fast rise/fall time signals with low-impedance drive capability that can easily couple into the high-impedance inputs of the input MUX channels. This coupling can create unwanted noise that gains up to V_{OUT}.
3. **Input MUX channels and source impedance.** Input MUX channels are high-impedance; when combined with high gain, the channels can pick up unwanted noise. Keep the input signal sources low-impedance (< 10kΩ). Also, consider bypassing input MUX channels with a ceramic bypass capacitor directly at the MUX input pin. Bypass capacitors greater than 100pF are recommended. Lower impedances and a bypass capacitor placed directly at the input MUX channels keep crosstalk between channels to a minimum as a result of parasitic capacitive coupling from adjacent PCB traces and pin-to-pin capacitance.

APPLICATIONS: DRIVING/INTERFACING TO ADCS

CDAC SAR ADCs contain an input sampling capacitor, C_{SH}, to sample the input signal during a sample period as shown in Figure 79. After the sample period, C_{SH} is removed from the input signal. Subsequent comparisons of the charge stored on C_{SH} are performed during the ADC conversion process. To achieve optimal op amp stability, input signal settling, and the demands for charge from the input signal conditioning circuitry, most ADC applications are optimized by the use of a resistor (R_{FILT}) and capacitor (C_{FILT}) filter placed between the op amp output and ADC input. For the PGA112/PGA113, or the PGA116/PGA117, setting C_{FILT} = 1nF and R_{FILT} = 100Ω yields optimum system performance for sampling converters operating at speeds up to 500kHz, depending upon the application settling time and accuracy requirements.

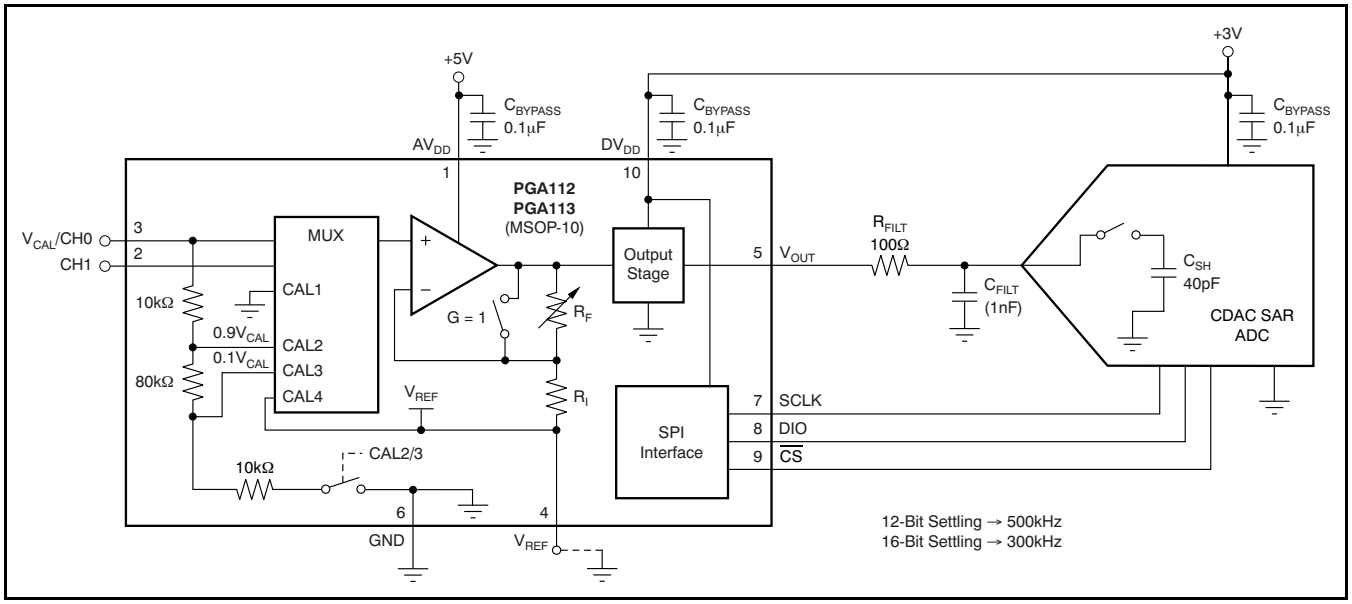


Figure 79. Driving/Interfacing to ADCs

POWER SUPPLIES

Figure 80 shows a typical mixed-supply voltage system where the analog supply, AV_{DD}, is +5V and the digital supply voltage, DV_{DD}, is +3V. The analog output stage of the PGA and the SPI interface digital circuitry are both powered from DV_{DD}. When considering the power required for DV_{DD}, use the Electrical Characteristics table and add any load current anticipated on V_{OUT}; this load current must be provided by DV_{DD}. This split-supply architecture ensures compatible logic levels with the microcontroller. It also ensures that the PGA output cannot run the input for the onboard ADC into an overvoltage condition; this condition could cause device latch-up and system lock-up, and require power-supply sequencing. Each supply pin should be individually bypassed with a 0.1µF ceramic capacitor directly at the device to ground. If there is only one power supply in the system, AV_{DD} and DV_{DD} can both be connected to the same supply; however, it is recommended to use individual bypass capacitors directly at each respective supply pin to a single point ground. V_{OUT} is diode-clamped to AV_{DD} (as shown in Figure 80); therefore, set DV_{DD} less than or equal to AV_{DD} + 0.3V. DV_{DD} and AV_{DD} must be within the operating voltage range of +2.2V to +5.5V.

At initial power-on, the state of the PGA is G = 1 and Channel 0 active. **CAUTION: For most applications, set $AV_{DD} \geq DV_{DD}$ to prevent V_{OUT} from driving current into AV_{DD} and raising the voltage level of AV_{DD}.**

SHUTDOWN AND POWER-ON-RESET (POR)

The PGA112/PGA113 have a software shutdown mode, and the PGA116/PGA117 offer both a hardware and software shutdown mode. When the PGA is shut down, it goes into a low-power standby mode. The Electrical Characteristics table details the current draw in shutdown mode with and without the SPI interface being clocked. In shutdown mode, R_F and R_I remain connected between V_{OUT} and V_{REF}.

When DV_{DD} is less than 1.6V, the digital interface is disabled and the channel and gain selections are held to the respective POR states of Gain = 1 and Channel = V_{CAL}/CH0. When DV_{DD} is above 1.8V, the digital interface is enabled and the POR gain and channel states remain unchanged until a valid SPI communication is received.

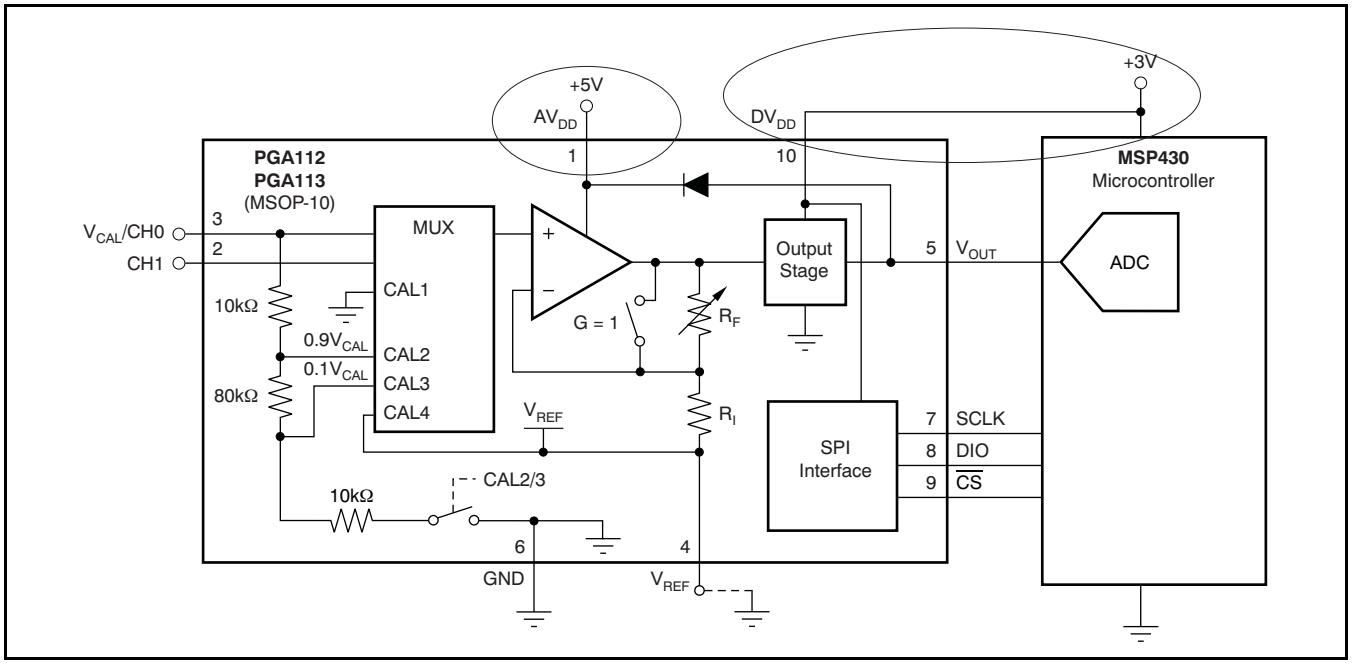


Figure 80. Split Power-Supply Architecture: $AV_{DD} \neq DV_{DD}$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
PGA112AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA112AIDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA112AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA112AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P112	Samples
PGA113AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA113AIDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA113AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA113AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	P113	Samples
PGA116AIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA116AIPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA116AIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA116AIPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA116	Samples
PGA117AIPW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA117	Samples
PGA117AIPWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA117	Samples
PGA117AIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA117	Samples
PGA117AIPWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PGA117	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

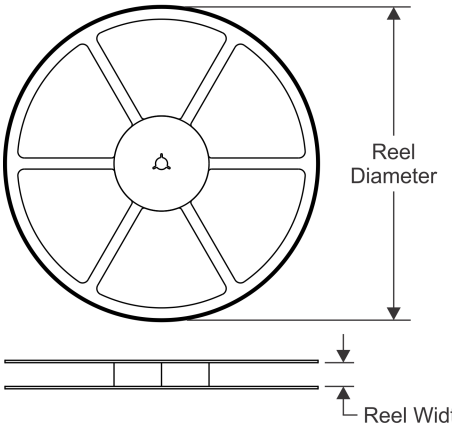
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

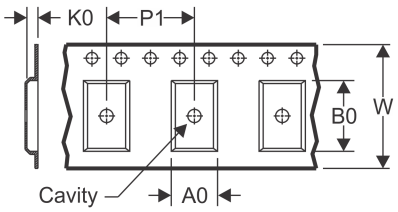
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

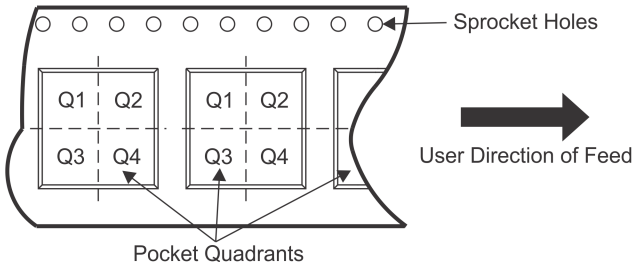


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

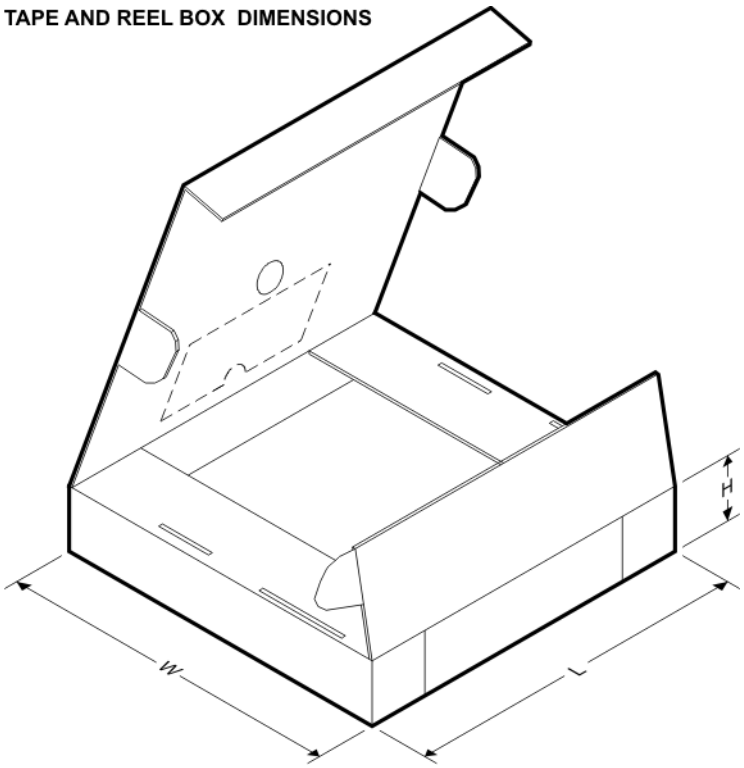
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA112AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA112AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PGA112AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA112AIDGST	VSSOP	DGS	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
PGA113AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA113AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
PGA116AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PGA117AIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

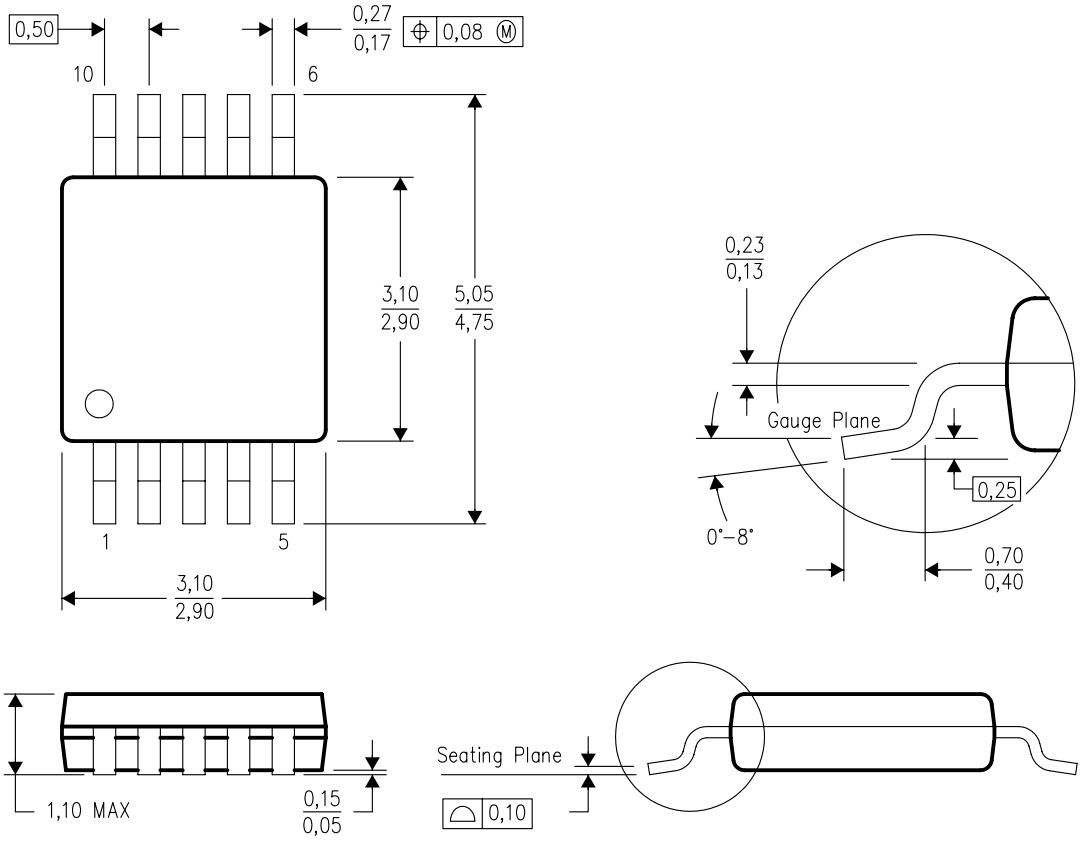
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA112AIDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
PGA112AIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
PGA112AIDGST	VSSOP	DGS	10	250	195.0	200.0	45.0
PGA112AIDGST	VSSOP	DGS	10	250	366.0	364.0	50.0
PGA113AIDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
PGA113AIDGST	VSSOP	DGS	10	250	195.0	200.0	45.0
PGA116AIPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
PGA117AIPWR	TSSOP	PW	20	2000	367.0	367.0	38.0

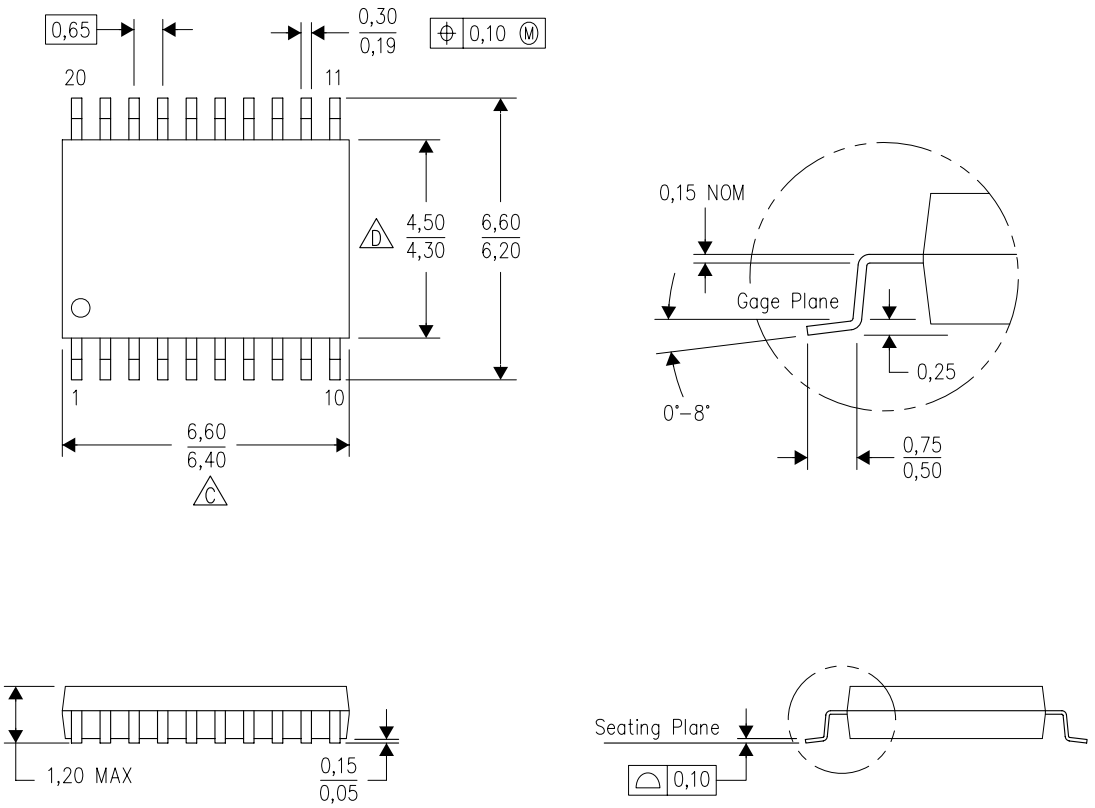
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

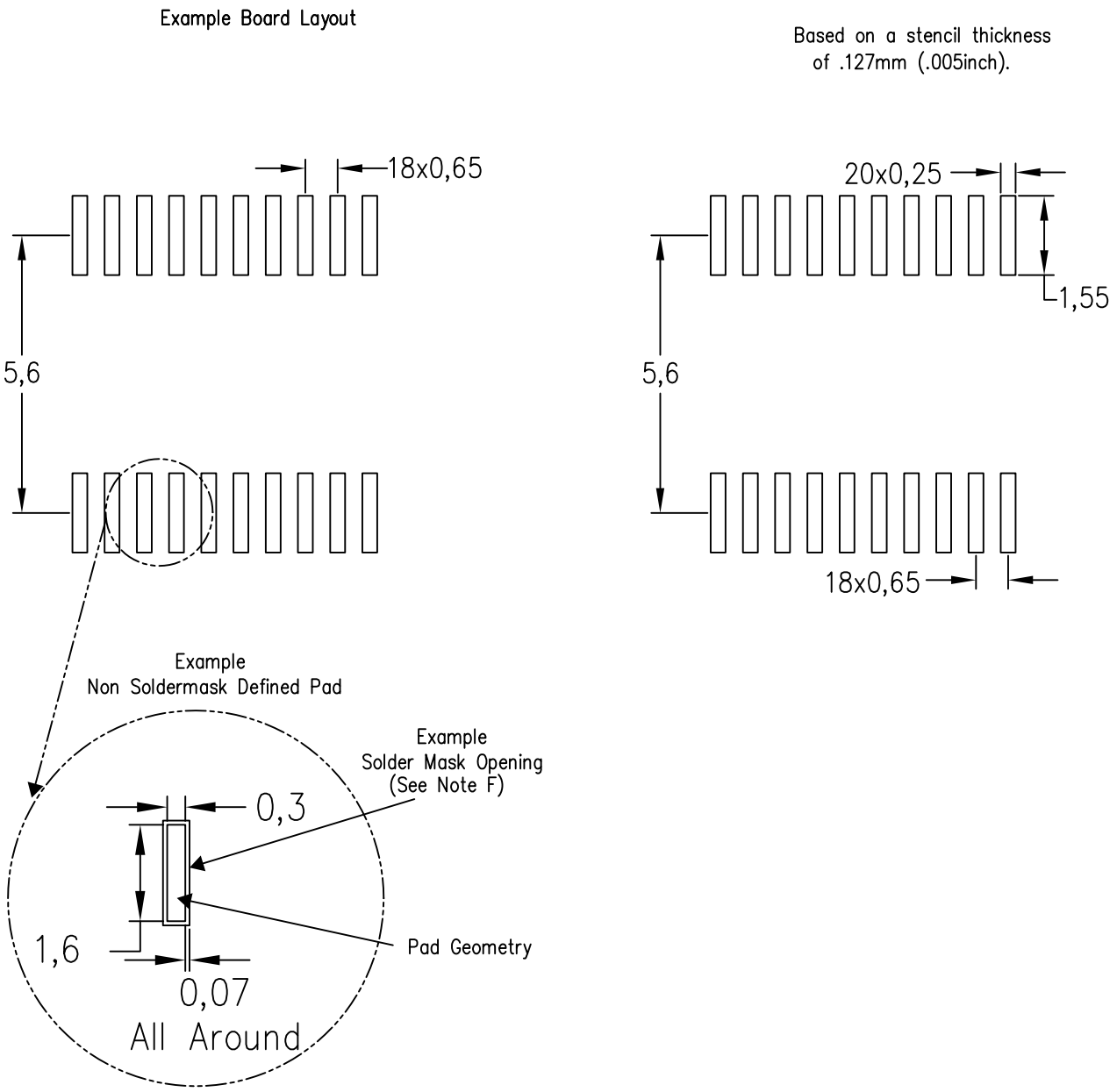
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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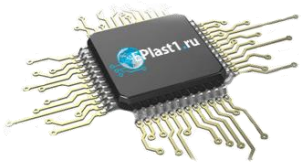

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