Automotive P-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY

V_{DS} (V)	- 100
$R_{DS(on)}$ (Ω) at V_{GS} = - 10 V	0.040
$R_{DS(on)}$ (Ω) at V_{GS} = - 4.5 V	0.048
I_D (A)	- 40
Configuration	Single

FEATURES

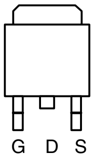
- TrenchFET® Power MOSFET
- Package with Low Thermal Resistance
- 100 % R_g and UIS Tested
- AEC-Q101 Qualified[d]
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

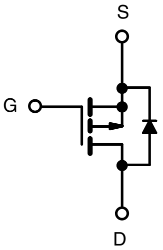
RoHS COMPLIANT

HALOGEN FREE

TO-263



Top View



P-Channel MOSFET

ORDERING INFORMATION

Package	TO-263
Lead (Pb)-free and Halogen-free	SQM40P10-40L-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	- 100	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25 °C	I_D	- 40	A
	T_C = 125 °C		- 23	
Continuous Source Current (Diode Conduction)[a]		I_S	- 60	
Pulsed Drain Current[b]		I_{DM}	- 160	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	- 45	
Single Pulse Avalanche Energy		E_{AS}	100	mJ
Maximum Power Dissipation[b]	T_C = 25 °C	P_D	150	W
	T_C = 125 °C		50	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount[c]	R_{thJA}	40	°C/W
Junction-to-Case (Drain)		R_{thJC}	1	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR-4 material).
d. Parametric verification ongoing.

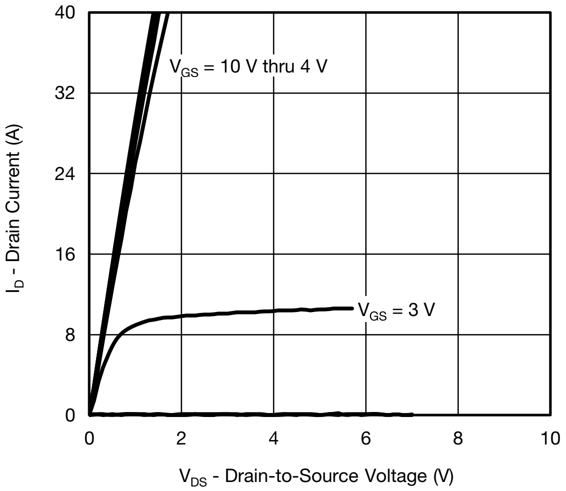
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = - 250 μA		- 100	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = - 250 μA		- 1.5	- 2.0	- 2.5	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = - 100 V	-	-	- 1	μA
		V_{GS} = 0 V	V_{DS} = - 100 V, T_J = 125 °C	-	-	- 50	
		V_{GS} = 0 V	V_{DS} = - 100 V, T_J = 175 °C	-	-	- 250	
On-State Drain Current[a]	$I_{D(on)}$	V_{GS} = - 10 V	V_{DS} ≤ - 5 V	- 30	-	-	A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 10 V	I_D = - 17 A	-	0.033	0.040	Ω
		V_{GS} = - 10 V	I_D = - 17 A, T_J = 125 °C	-	-	0.060	
		V_{GS} = - 10 V	I_D = - 17 A, T_J = 175 °C	-	-	0.099	
		V_{GS} = - 4.5 V	I_D = - 14 A	-	0.0367	0.0480	
Forward Transconductance[b]	g_{fs}	V_{DS} = - 15 V, I_D = - 17 A		-	47	-	S
Dynamic[b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = - 25 V, f = 1 MHz	-	4236	5295	pF
Output Capacitance	C_{oss}			-	314	395	
Reverse Transfer Capacitance	C_{rss}			-	216	270	
Total Gate Charge[c]	Q_g	V_{GS} = - 10 V	V_{DS} = - 50 V, I_D = - 40 A	-	89	134	nC
Gate-Source Charge[c]	Q_{gs}			-	11.6	-	
Gate-Drain Charge[c]	Q_{gd}			-	19.6	-	
Gate Resistance	R_g	f = 1 MHz		1.4	2.89	4.5	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = - 50 V, R_L = 1.25 Ω I_D ≅ - 40 A, V_{GEN} = - 10 V, R_g = 1 Ω		-	10	15	ns
Rise Time[c]	t_r			-	10	15	
Turn-Off Delay Time[c]	$t_{d(off)}$			-	63	95	
Fall Time[c]	t_f			-	20	30	
Source-Drain Diode Ratings and Characteristics[b]							
Pulsed Current[a]	I_{SM}			-	-	- 160	A
Forward Voltage	V_{SD}	I_F = - 30 A, V_{GS} = 0 V		-	- 0.9	- 1.5	V

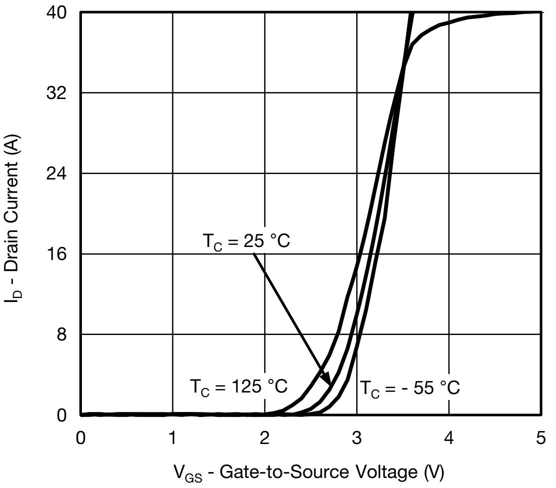
Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

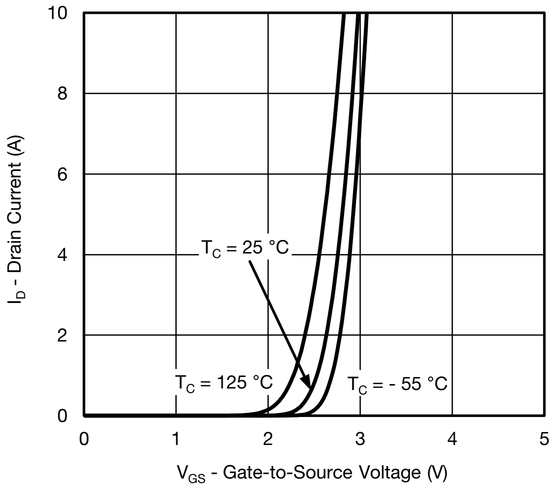
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



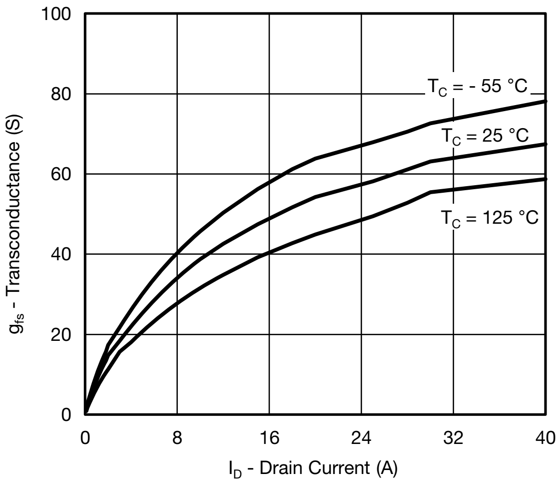
Output Characteristics



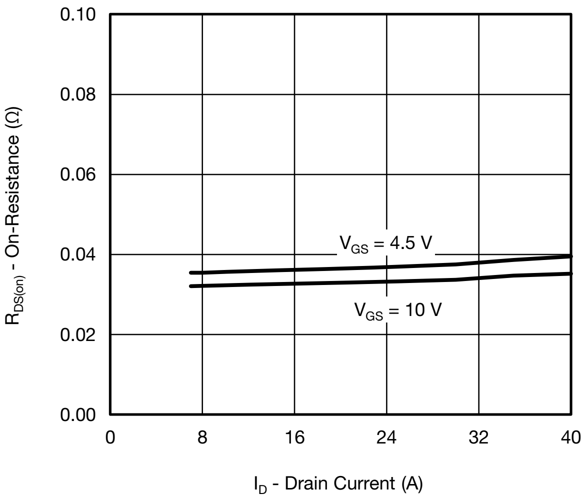
Transfer Characteristics



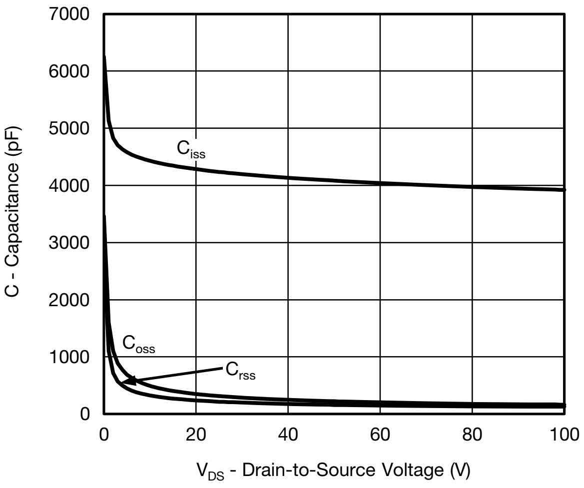
Transfer Characteristics



Transconductance

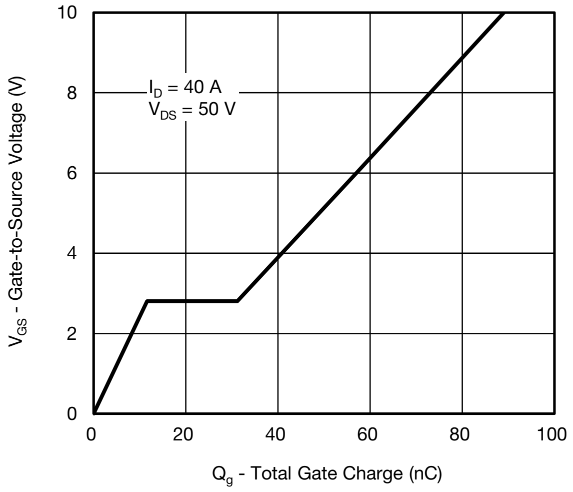


On-Resistance vs. Drain Current

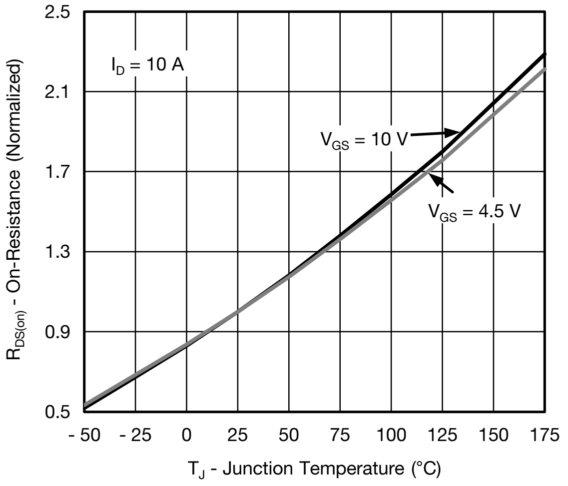


Capacitance

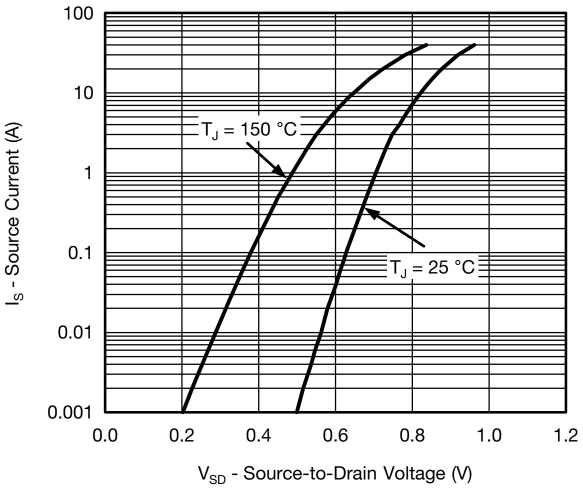
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



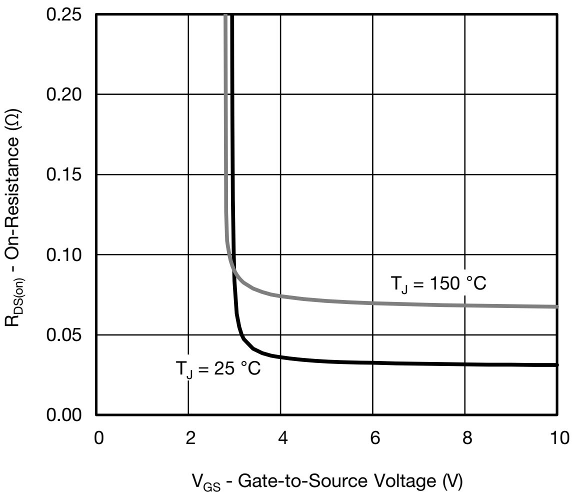
Gate Charge



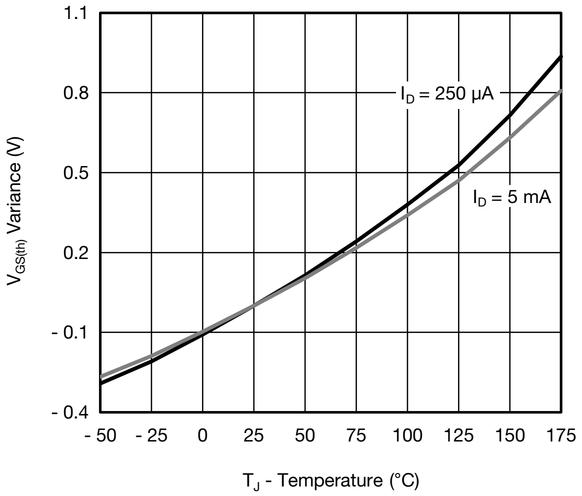
On-Resistance vs. Junction Temperature



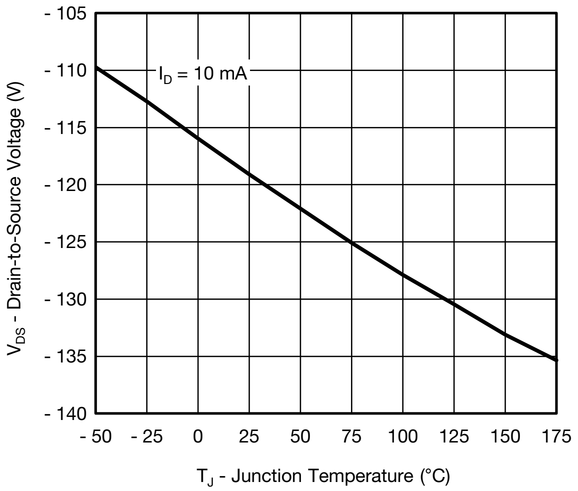
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

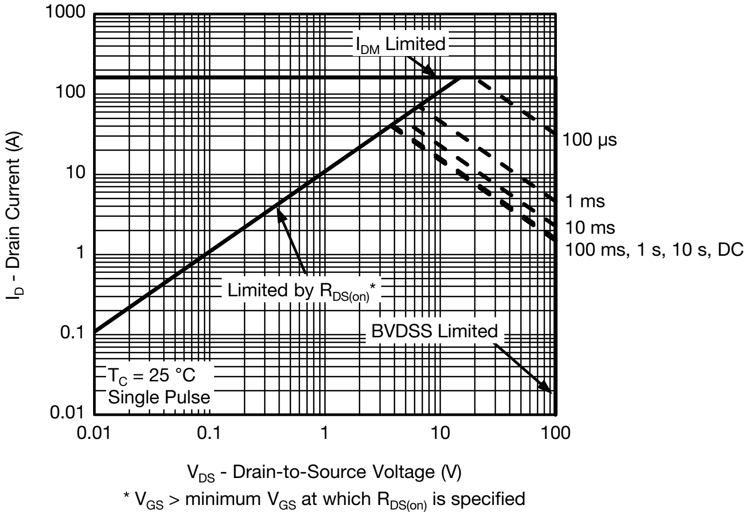


Threshold Voltage

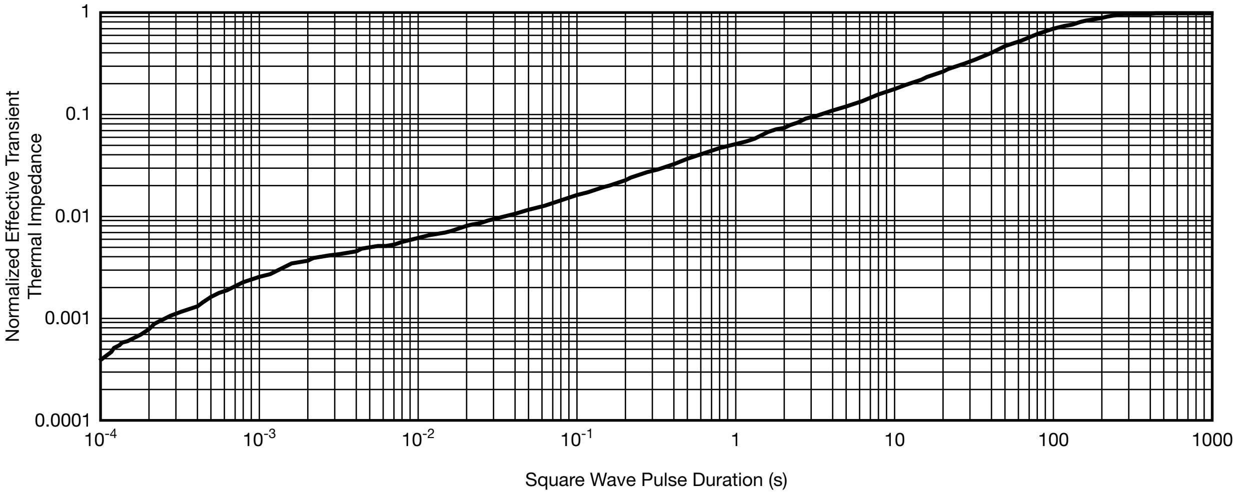


Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

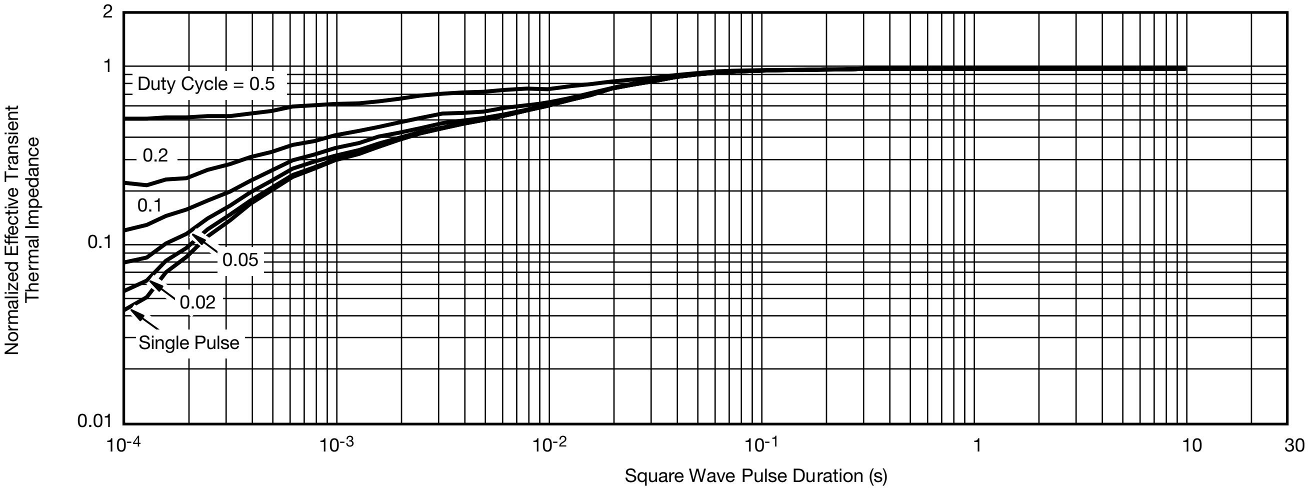


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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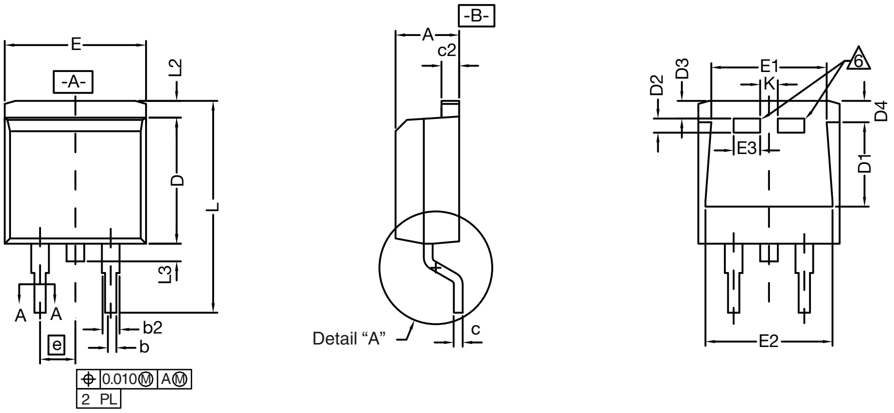
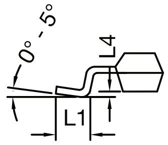
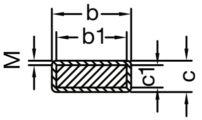
TO-263 (D^{2}PAK): 3-LEAD





DETAIL A (ROTATED 90°)



SECTION A-A

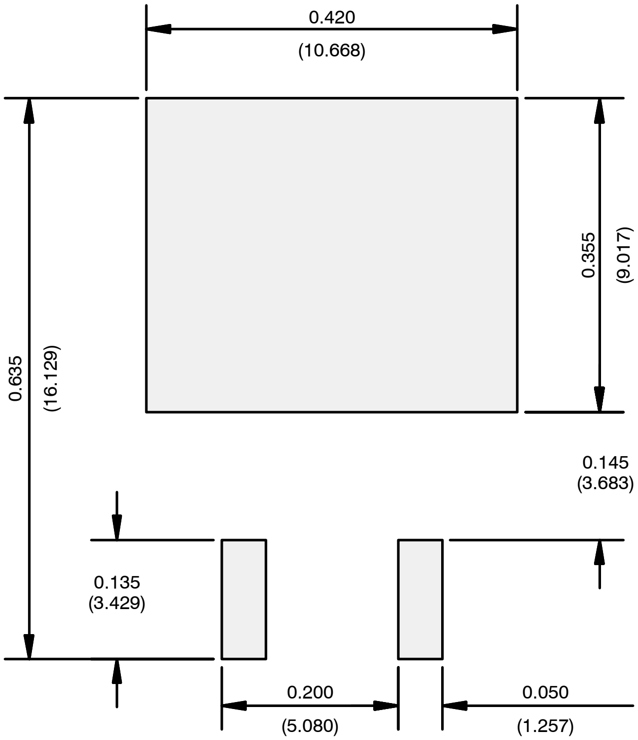
DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050

ECN: T13-0707-Rev. K, 30-Sep-13
DWG: 5843

Notes

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

RECOMMENDED MINIMUM PADS FOR D^{2}PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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