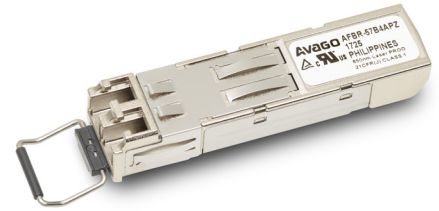


AFBR-57B4APZ

DC-50 MBaud 850 nm Multimode LC Duplex SFP Transceiver



Description

The SFP transceiver provides system designers the ability to implement DC-50 MBaud data transmission over 2 km with (62.5 μm /125 μm) multimode fibers. The transceiver supports LC duplex connector and is lead free, RoHS compliant. Using the 2-wire serial interface defined in the SFF-8472 MSA, the AFBR-57B4APZ provides real-time information on module temperature, transmitter supply voltage and receiver average input power.

Transmitter

The transmitter consists of 850 nm class 1 laser compliant VCSEL with an integrated driver IC. The VCSEL driver operates at 3.3V. It receives LVTTTL electrical input and converts it into a modulated current driving the VCSEL. The VCSEL is packaged in an optical subassembly.

The optimized lens system of the optical subassembly couples the emitted optical power very efficiently into multimode fibers.

Receiver

The receiver utilizes a fully integrated single-chip solution which provides excellent immunity to EMI and fast transient dV/dt rejection. The receiver directly converts optical signal to a digital LVTTTL/LVCMOS signal. Receiver operates at 3.3V.

Module Package

The transceiver package is compatible with the Small Form Pluggable (SFP) MSA with the LC duplex connector option. The hot-pluggable capability of the SFP package allows the module to be installed even when host is on-line and operating. The transceiver requires a 3.3V DC power supply for optimal performance.

Features

- Data rate support from DC to 50 MBaud
- Single 3.3V power supply
- Manufactured in an ISO 9001 certified facility
- 850 nm VCSEL transmitter
- Link Distance up to 2 km with 62.5 μm /125 μm multimode fiber
- Low current and low power dissipation
- Hot pluggable SFP connector
- Compatible with SFP MSA specification
- Class 1 FDA IEC60825-1 laser safety compliant
- Operating temperature -40°C to $+85^{\circ}\text{C}$
- Excellent EMI and EMC behavior
- Integrated 850 nm VCSEL and driver IC with LVTTTL input logic transmitter
- Integrated PIN diode and digitalizing IC with LVTTTL output logic receiver

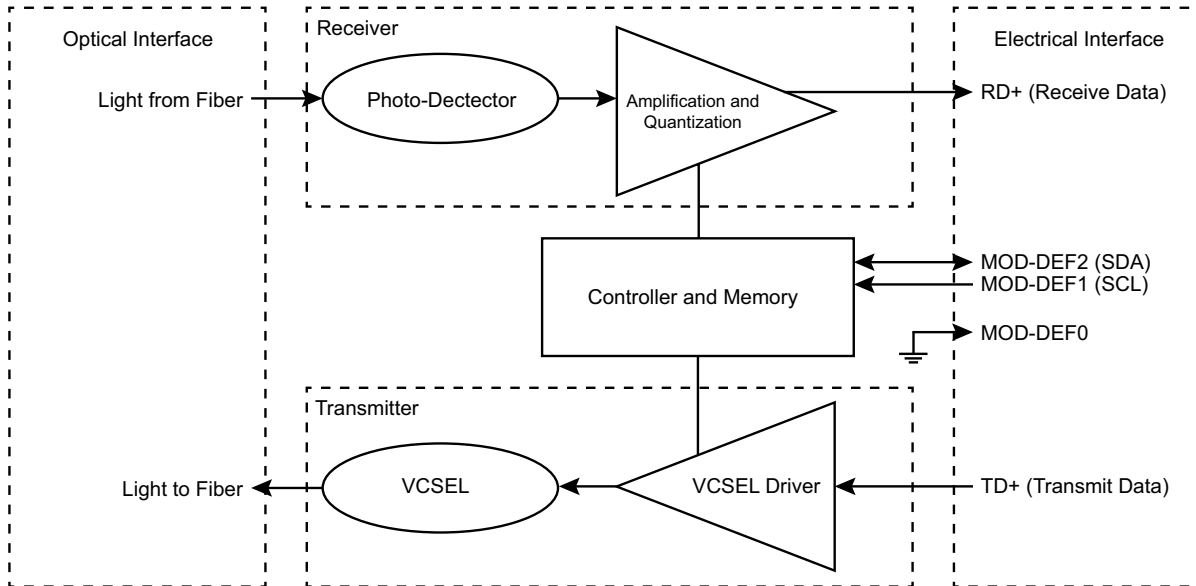
Applications

- Power substation automation
- HVDC
- Industrial networking over multimode fiber

Transceiver Functional Diagram

Figure 1 shows the major functional components of the transceiver.

Figure 1: Transceiver Functional Diagram



Data I/O

The transceiver is designed to accept industry-standard LVTTTL signals. The transceiver provides a DC-coupled data interface that is loaded with a current source of 15 μ A toward an internal reference voltage (1.2V).

Regulatory Compliance

See Table 1 for transceiver Regulatory Compliance performance. The overall equipment design will determine the certification level. The transceiver performance is offered as a figure of merit to assist the designer.

Electrostatic Discharge (ESD)

There are two conditions where immunity to ESD damage is important. Regulatory Compliance documents the transceiver's immunity to both of these conditions. The first condition is static discharge to the transceiver when handling; for example, when the transceiver is inserted into the transceiver port. To protect the transceiver, it is important to use normal ESD handling procedures. The ESD sensitivity of the transceiver is compatible with typical industry production environments. The second condition is static discharge to the exterior of the host equipment chassis after installation. To the extent at which the duplex LC optical interface is exposed to outer part of the host equipment chassis, transceiver may be subjected to system-level ESD events. The ESD performance of the transceiver exceeds typical industry standards.

Electromagnetic Interference (EMI)

Equipment designs utilizing these transceivers from Broadcom shall meet the requirements of CENELEC EN 55032:2012.

The metal housing and shielded design of the transceiver minimizes the EMI challenge faced by the host equipment designers. The transceivers provide superior EMI performance.

Eye Safety

These transceivers provide Class 1 eye safety by design. Broadcom has tested the transceiver design for compliance with the requirements listed in [Table 1](#) under normal operating conditions and under a single fault condition.

Flammability

The AFBR-57B4APZ transceiver housing is made of high strength, heat and chemical resistant metal and UL-94V-0 flame retardant plastic.

Regulatory Compliance

| Feature | Test Method | Performance |
|---|---|--|
| Electrostatic Discharge (ESD) to the electrical pins | JEDEC JESD22-A114 | Meets Class 2 (2000V to 3999V). Withstands up to 2000V applied between electrical pins. |
| Electrostatic Discharge (ESD) to the Duplex LC Receptacle | Variation of IEC 61000-4-2 | Typically withstands at least 9 kV without damage when the LC connector receptacle is contacted by a Human Body Model probe. Typically withstands 15 kV air discharge on LC-connector receptacle. |
| Electromagnetic Interference (EMI) | FCC Class B, CENELEC EN 55032:2012 (CISPR 32) Class B | System margins are dependent on customer board and chassis design. |
| Immunity | Variation of IEC 61000-4-3 Std C37.90.2-2004 | Typically shows no measurable effect from a 20 V/m field swept from 80 MHz to 1 GHz applied to the transceiver without a chassis enclosure. |
| Eye Safety | EN 60950-1 EN 60825-1 EN 60825-2 | Compliant per Broadcom, testing under single fault conditions. |
| RoHS Compliance | — | Reference to RoHS Directive 2011/65EU |

Digital Diagnostic Interface and Serial Identification

The 2-wire serial interface is based on ATMEL AT24C02C series EEPROM protocol. Conventional EEPROM memory (bytes 0–255 at memory address 0xA0) is organized in compliance with SFF-8074i. As an enhancement the transceiver is compatible to SFF-8472. This enhancement offers digital diagnostic information at bytes 0–255 at memory address 0xA2. In addition to monitoring of the VCSEL drive current and photodiode current, the interface also monitors the supply voltage and the module ambient temperature. The transmitter voltage supply must be provided for the digital diagnostic interface to operate.

Pin Description

Figure 2 shows top and bottom of PCB board.

Figure 2: PCB Pin Connection

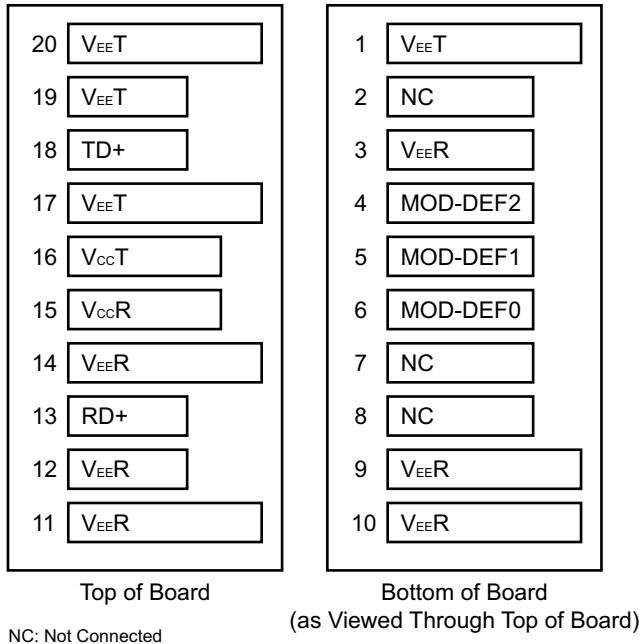


Table 1 lists the pins and their functions.

Table 1: PCB Pin Connections

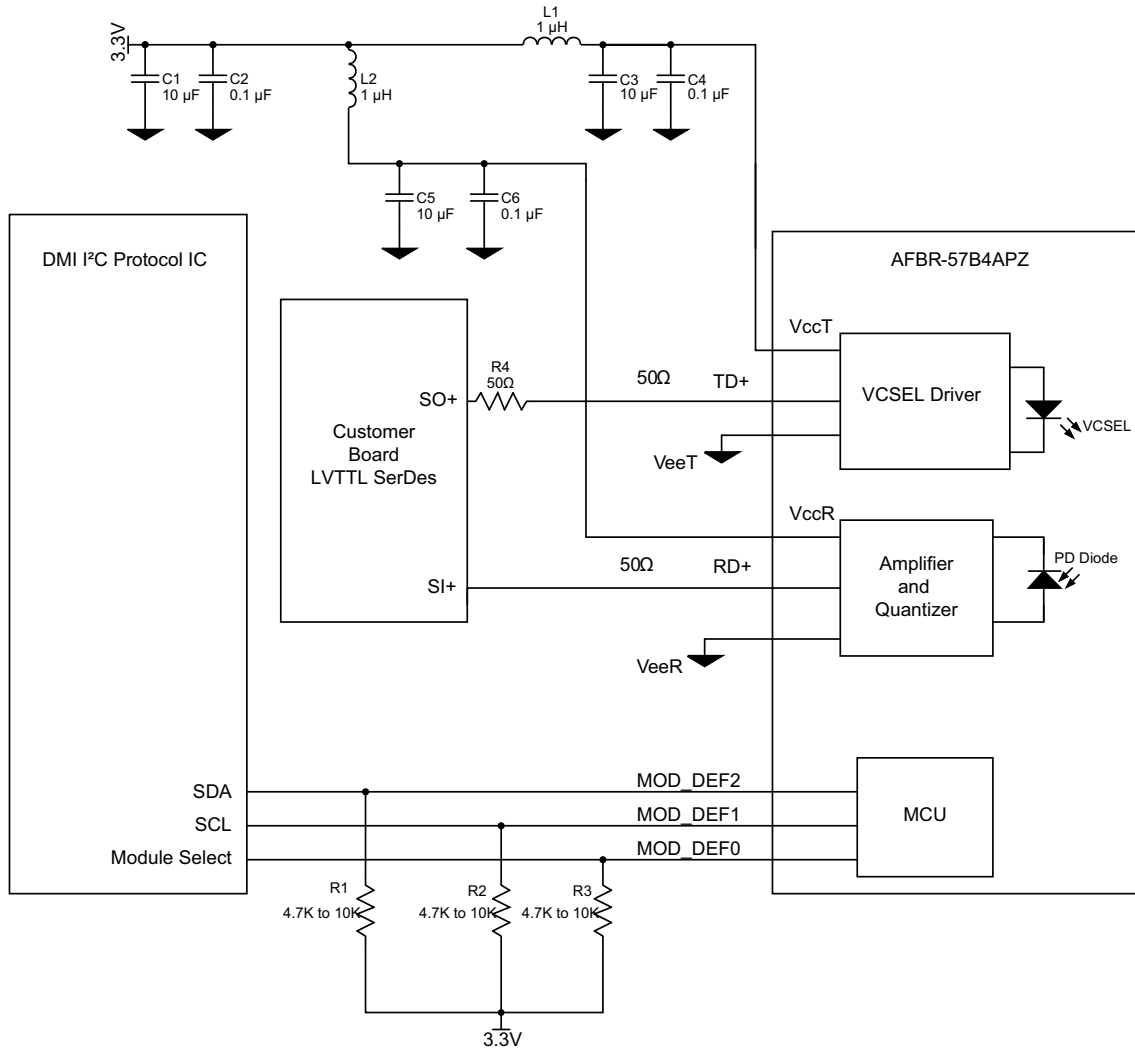
| Pin | Name | Function/Description | MSA Notes |
|-----|----------|---|-----------|
| 1 | VEET | Transmitter Ground | a |
| 2 | NC | Not Connected | — |
| 3 | VEER | Receiver Ground | — |
| 4 | MOD-DEF2 | Module Definition 2: 2-wire serial ID interface | b |
| 5 | MOD-DEF1 | Module Definition 1: Two wire serial ID interface | b |
| 6 | MOD-DEF0 | Module Definition 0: Grounded in module | b |
| 7 | NC | Not Connected | — |
| 8 | NC | Not Connected | — |
| 9 | VEER | Receiver Ground | a |
| 10 | VEER | Receiver Ground | a |
| 11 | VEER | Receiver Ground | a |
| 12 | VEER | Receiver Ground | — |
| 13 | RD+ | Received Data Out | c, d |
| 14 | VEER | Receiver Ground | a |
| 15 | VCCR | Receiver Power 3.3V | — |
| 16 | VCCT | Transmitter Power 3.3V | — |
| 17 | VEET | Transmitter Ground | a |

Table 1: PCB Pin Connections (Continued)

| Pin | Name | Function/Description | MSA Notes |
|-----|------|----------------------|-----------|
| 18 | TD+ | Transmitter Data In | d, e |
| 19 | VEET | Transmitter Ground | — |
| 20 | VEET | Transmitter Ground | a |

- a. Transmitter and Receiver grounds are connected together in the transceiver PCB.
- b. MOD-DEF 0, 1, 2 are the module definition pins. They should be pulled up with a 4.7 kΩ to 10 kΩ resistor on the host board to a supply less than VCCT + 0.3V or VCCR + 0.3V. In order to use this interface, supply 3.3V to VCCT.
 - MOD-DEF0 is grounded by the module to indicate that the module is present.
 - MOD-DEF1 is the clock line of the two-wire serial interface.
 - MOD-DEF2 is the data line of the two-wire serial interface.
- c. RD+: The receiver data output. The pin is LVTTTL output logic.
- d. Optical and electrical signal is non-inverted.
- e. TD+: The transmitter input. The pin is LVTTTL input logic.

Figure 3: Recommended Application Circuitry



Mechanical Dimensions and Module Drawings

Figure 4: Mechanical Dimensions

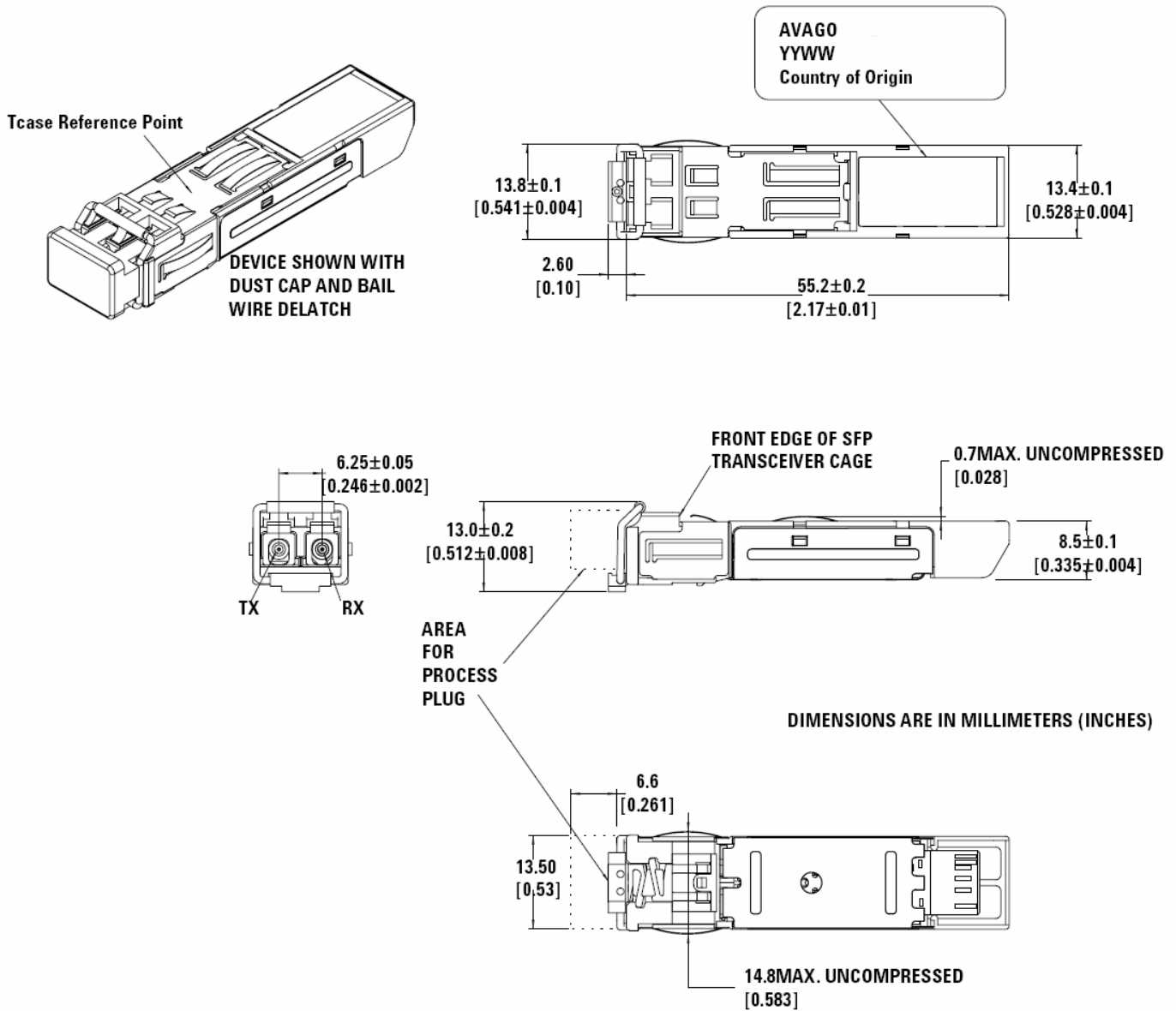
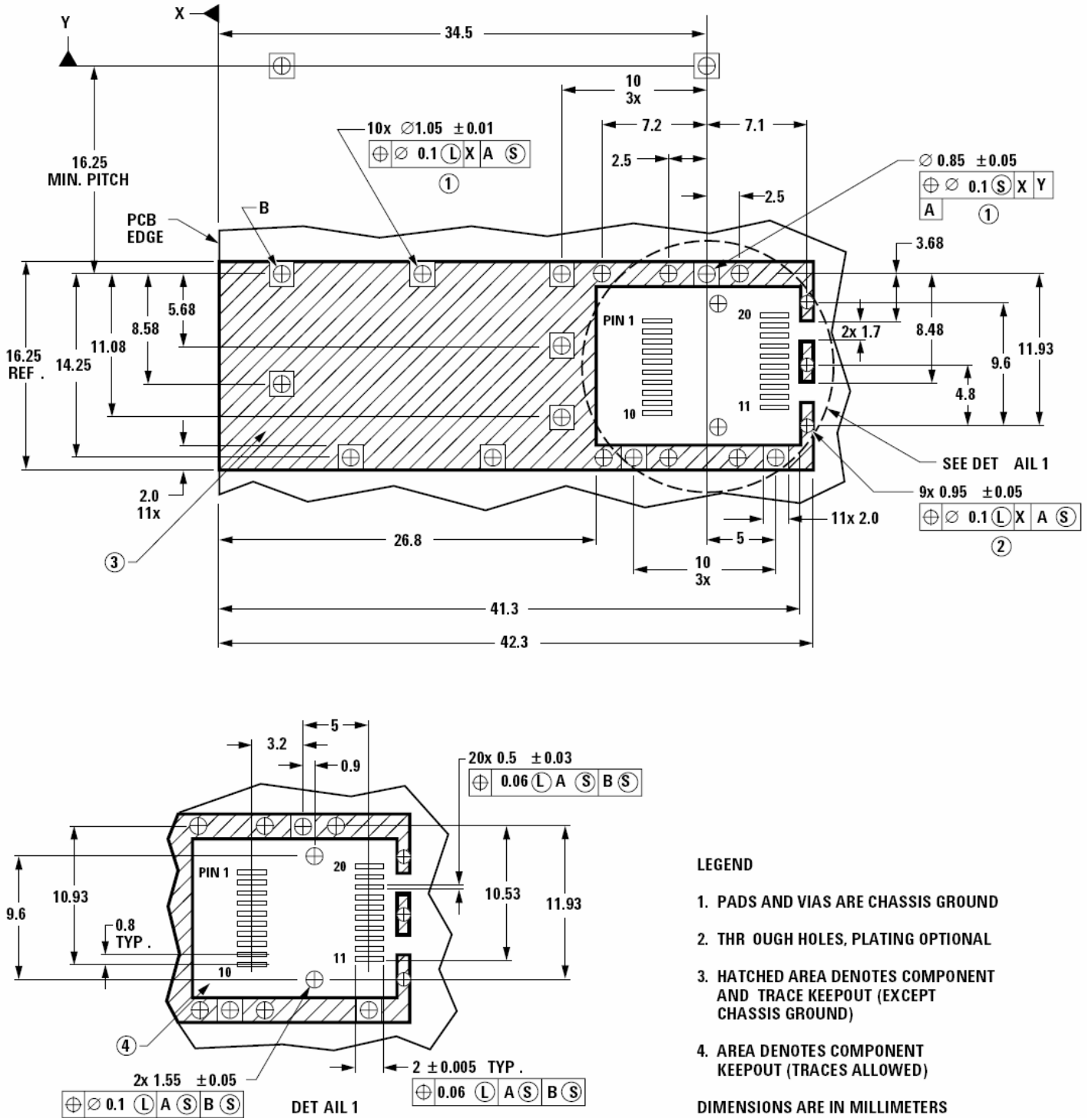


Figure 5: SFP Host Board Mechanical Layout

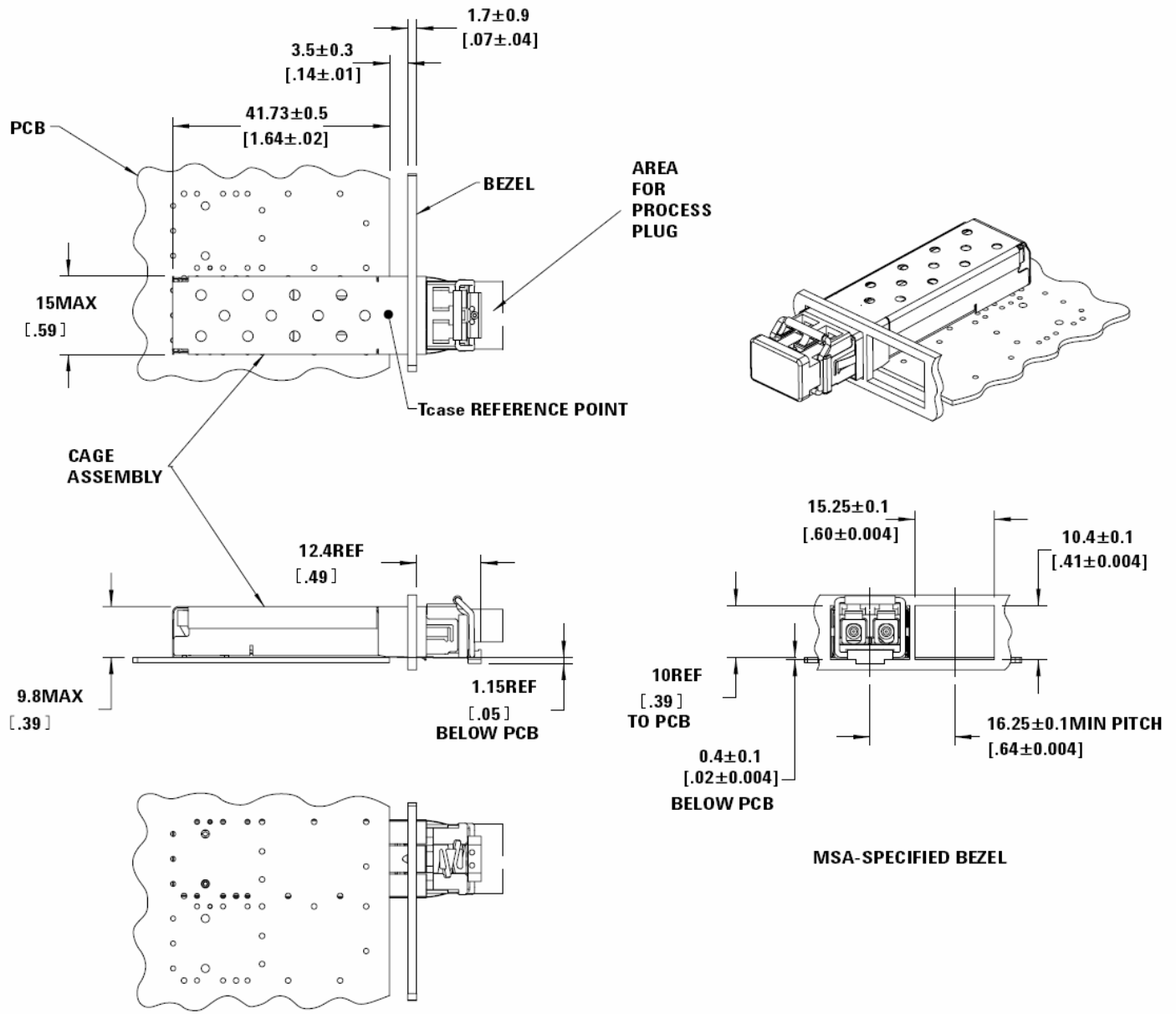


LEGEND

1. PADS AND VIAS ARE CHASSIS GROUND
2. THROUGH HOLES, PLATING OPTIONAL
3. HATCHED AREA DENOTES COMPONENT AND TRACE KEEPOUT (EXCEPT CHASSIS GROUND)
4. AREA DENOTES COMPONENT KEEPOUT (TRACES ALLOWED)

DIMENSIONS ARE IN MILLIMETERS

Figure 6: SFP Assemblies Drawing



DIMENSIONS ARE IN MILLIMETERS [INCHES].

Absolute Maximum Ratings

Exposure to the absolute maximum ratings for extended periods can adversely affect device reliability. It should not be assumed that limiting values of more than one parameter can be applied to the products at the same time.

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|-----------------------------|----------|------|----------|------|-------|
| Storage Temperature | T_s | -40 | +100 | °C | — |
| Supply Voltage | V_{cc} | -0.5 | 3.63 | V | — |
| Operating Relative Humidity | ϕ | — | 95 | % | a |
| Data Input Voltage | V_i | -0.5 | V_{cc} | V | — |
| Data output current | I_o | — | 10 | mA | — |

a. Normal operating humidity range is up to 85%. 95% humidity conditions at 70°C must not exceed 16 hours.

Recommended Operating Conditions

All the data in this specification refers to the operating conditions above and over lifetime unless otherwise stated.

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|-------------------------------|----------|------|------|------|-------|-------|
| Ambient Operating Temperature | T_c | -40 | — | +85 | °C | a |
| Supply Voltage | V_{cc} | 3.0 | 3.3 | 3.6 | V | — |
| Signaling rate | B | DC | — | 50 | MBaud | b |

a. Electrical and optical specifications of the product are guaranteed across recommended ambient operating temperature only.

b. Characterized with 50 MBaud, PRBS27-1 pattern.

Transmitter Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|------------------------|------------|------|------|----------|------------|-------|
| Supply Current | I_{cc} | — | 12 | 15 | mA | a |
| Power Dissipation | P_{diss} | — | 36 | 55 | mW | — |
| Input Voltage Low | V_{IL} | 0.0 | — | 0.8 | V | — |
| Input Voltage High | V_{IH} | 2.0 | — | V_{cc} | V | — |
| Data Input Capacitance | C_{in} | — | 5 | — | pF | — |
| Data Input Resistance | R_{in} | — | 80 | — | k Ω | — |
| Propagation Delay | T_{PD} | — | 6 | 15 | ns | — |

a. Typical values are for room temperature at 3.3V. The value is the combined current consumption of the transmitter, DMI block, and A0 memory.

Receiver Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--|------------|------|------|----------|------|------------|
| Supply Current | I_{CC} | — | 20 | 30 | mA | a |
| Power Dissipation | P_{diss} | — | 66 | 108 | mW | a |
| Data Output Rise Time (10% to 90%) | t_r | — | 1.7 | 5.0 | ns | a |
| Data Output Fall Time (10% to 90%) | t_f | — | 1.3 | 5.0 | ns | a |
| Data Output High | V_{OH} | 2.0 | — | V_{CC} | V | b |
| Data Output Low | V_{OL} | -0.3 | — | 0.8 | V | b |
| Pulse Width Distortion subsequent pulses | R_{PWDS} | -4 | — | +4 | ns | c, d, e, f |
| Pulse Width Distortion 1st to 3rd Pulse | R_{PWD1} | -8 | — | +8 | ns | e, f, g |
| Propagation Delay | R_{PD} | — | 8 | 30.0 | ns | — |

- Typical values are for room temperature at 3.3V.
- RD+ data is LVTTTL output logic.
- Optical input of 50 MBaud PRBS-7 pattern and 50% duty cycle.
- Pulse width is measured at 50% threshold using a rising edge trigger and PRBS-7 pattern.
- If data rate is below 1 MBaud, the pulse width distortion would be equal to the pulse width distortion of the 1st to 3rd pulses for higher data rates.
- Limits are valid for running the receiver with an ideal light input source.
- The threshold of the 1st pulse of a data sequence is difficult to adjust and therefore the pulse width distortion up to the 3rd pulse is higher than for all other pulses (worst case for the 1st pulse). This strongly depends on the quality of the rising and falling edge of the optical input. The faster the edges the smaller the pulse width variation. Furthermore lower data rates would result in the same issue as all the pulse become 1st pulses.

Transmitter Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--|-----------------|-------|-------|------|------|-------|
| Output Optical Power (Peak) 62.5 μ m/125 μ m NA = 0.275 Fiber | P_o | -14.0 | -11.0 | -8 | dBm | a |
| Extinction Ratio | ER | 10 | 20 | — | dB | — |
| Central Wavelength | λ_C | 805 | 845 | 865 | nm | — |
| Spectral width - FWHM | $\Delta\lambda$ | — | 0.5 | 5 | nm | — |
| Optical Rise Time (20% to 80%) | t_r | — | 0.5 | 4 | ns | b, c |
| Optical Fall Time (20% to 80%) | t_f | — | 0.3 | 3 | ns | b, c |
| Pulse width distortion first pulse | T_{PWD1} | -7 | — | +2 | ns | b, d |
| Pulse width distortion subsequent pulses | T_{PWDS} | -5 | — | +2 | ns | b, e |

- Optical values are measured over the specified operating voltage and temperature ranges. The peak power can be converted to an average value by subtracting 3 dB.
- Measured with 1.25 Gb/s optical to electrical converter.
- Measured with 20% to 80% markers to achieve stable results.
- First pulse width is measured with a long period of low pulses followed by a high pulse.
- Pulse width is measured at 50% threshold using a rising edge trigger tested with PRBS-7 pattern.

Receiver Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--------------------------------------|----------|-------|-------|------|------|-------|
| Input Optical Power (Peak) | P_{in} | -25.0 | — | -7.0 | dBm | a |
| Input Optical Power (Peak) Off State | P | — | -34.0 | — | dBm | — |
| Operating Wavelength | O | 800 | — | 870 | nm | — |

- a. This specification is intended to indicate the performance of the receiver section of the transceiver when Optical Input Power signal characteristics are present as per the following definitions:
- Over the specified operating temperature and voltage ranges
 - Bit Error Rate (BER) is better than or equal to 1×10^{-10}
 - Transmitter is operating to simulate any cross-talk present between the transmitter and receiver sections of the transceiver.
 - Fiber: 62.5 μm /125 μm , NA = 0.275;

Digital Diagnostics Monitoring Interface

The transceiver features an enhanced digital diagnostic interface, compliant to the *Digital Diagnostic Monitoring Interface for Optical Transceivers SFF-8472 Multi-source Agreement (MSA)*. Refer to the MSA document to access information on the range of options, both hardware and software, available to the host system for utilizing the available digital diagnostic features.

The enhanced digital interface allows real-time access to device operating parameters. In addition, it fully incorporates the functionality needed to implement digital alarms and warnings, as defined by the SFF-8472 MSA. With the digital diagnostic monitoring interface, the user has capability of performing component monitoring, fault isolation and failure prediction in their transceiver-based applications. The diagnostic monitoring interface (DMI) has two 256-byte memory maps in EEPROM which are accessible over a 2-wire interface: the serial ID memory map at address 1010000X (0xA0) and the digital diagnostic memory map at address 1010001X (0xA2).

The serial ID memory map contains a serial identification and vendor specific information. This information is read-only.

The digital diagnostic memory map contains device operating parameters as well as alarm and warning flags. The operating parameters are to be retrieved through a sequential read command ensuring that the MSB and LSB of each parameter is "coherent". MSB should be accessed before LSB. Furthermore, the memory map contains 120 bytes that can be written by the user as well as a writable soft control byte.

For applications requiring continuous updates to alarm and warning limits, it is recommended to use the available real-time monitor in combination with software algorithms. Continuous writing to alarm/warning registers should be avoided.

Transceiver Diagnostics Timing Characteristics

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|-----------------------------|----------------|------|------|------|-------|
| Time to Initialize | t_init | — | 300 | ms | a |
| Analog parameter Data Ready | t_data | — | 1000 | ms | b |
| Serial Hardware Ready | t_serial | — | 300 | ms | c |
| Write Cycle Time | t_write | — | 10 | ms | d |
| Serial ID Clock Rate | f_serial_clock | — | 400 | kHz | e |

- Time from power on to the transmitter and receiver being ready to send/receive data.
- From power on to the data ready bit asserted (A2h, byte 110, bit 0). Data ready indicates analog monitoring circuitry is functional.
- Time from power on until the module is ready for data transmission over the serial bus (reads or writes over A0h and A2h).
- Time from stop bit to the completion of a 1 to 8-byte write command.
- It is not recommended to continuously read the A2 digital diagnostic interface for more than 20 ms without a minimum time pause interval of 20 ms.

Transceiver Digital Diagnostic Monitor (Real Time Parameter Accuracy) Characteristics

| Parameter | Symbol | Max. | Unit | Notes |
|---|--------|------|------|--|
| Transceiver Internal Temperature Accuracy | TINT | ±5.0 | °C | Registers indicate case temperature, which is derived from the internally measured temperature. Valid from –40°C to +85°C case temperature. |
| Transceiver Internal Supply Voltage Accuracy | VINT | ±0.1 | V | Supply voltage is measured internal to the transceiver and can, with less accuracy, be correlated to voltage at the SFP V _{CC} pin. Valid over 3.3V ±10%. |
| Transmitter VCSEL DC Bias Current Accuracy | IBIAS | ±10 | % | By design, IBIAS is better than ±10% nominal value. The value is not monitored. |
| Transmitter Average Optical Power Accuracy | PT | ±3.0 | dB | By design, PRBS7 modulated PT is better than ±3.0 dB nominal value. The value is not monitored. |
| Received Average Optical Input Power Accuracy | PR | ±3.0 | dB | Coupled in a 62.5 μm/125 μm fiber. Averaging time constant is about 100 kHz. |

EEPROM Serial ID Memory Contents (Address A0h)

| Byte No. Decimal | Hex | ASCII | Description |
|------------------|-----|-------|-----------------|
| 0 | 03 | — | SFP transceiver |
| 1 | 04 | — | — |
| 2 | 07 | — | LC connector |
| 3 | 00 | — | — |
| 4 | 00 | — | — |
| 5 | 00 | — | — |
| 6 | 00 | — | — |
| 7 | 00 | — | — |
| 8 | 00 | — | — |
| 9 | 08 | — | — |
| 10 | 00 | — | — |
| 11 | 00 | — | — |
| 12 | 00 | — | — |
| 13 | 00 | — | — |
| 14 | 00 | — | — |
| 15 | 00 | — | — |
| 16 | 00 | — | — |
| 17 | C8 | — | — |
| 18 | 00 | — | — |
| 19 | 00 | — | — |
| 20 | 41 | A | — |
| 21 | 56 | V | — |
| 22 | 41 | A | — |
| 23 | 47 | G | — |
| 24 | 4F | O | — |
| 25 | 20 | — | — |
| 26 | 20 | — | — |
| 27 | 20 | — | — |
| 28 | 20 | — | — |
| 29 | 20 | — | — |
| 30 | 20 | — | — |
| 31 | 20 | — | — |
| 32 | 20 | — | — |
| 33 | 20 | — | — |
| 34 | 20 | — | — |
| 35 | 20 | — | — |
| 36 | 00 | — | — |
| 37 | 00 | — | — |
| 38 | 17 | — | — |
| 39 | 6A | — | — |
| 40 | 41 | A | — |
| 41 | 46 | F | — |

| Byte No. Decimal | Hex | ASCII | Description |
|------------------|-----|-------|--|
| 42 | 42 | B | — |
| 43 | 52 | R | — |
| 44 | 2D | — | — |
| 45 | 35 | 5 | — |
| 46 | 37 | 7 | — |
| 47 | 42 | B | — |
| 48 | 34 | 4 | — |
| 49 | 41 | A | — |
| 50 | 50 | P | — |
| 51 | 5A | Z | — |
| 52 | 20 | — | — |
| 53 | 20 | — | — |
| 54 | 20 | — | — |
| 55 | 00 | — | — |
| 56 | 30 | — | — |
| 57 | 30 | — | — |
| 58 | 30 | — | — |
| 59 | 30 | — | — |
| 60 | 03 | — | a |
| 61 | 52 | — | a |
| 62 | 00 | — | — |
| 63 | B7 | — | b |
| 64 | 00 | — | — |
| 65 | 00 | — | Tx disable not implemented. |
| 66 | 00 | — | — |
| 67 | 00 | — | — |
| 68–83 | — | — | c |
| 84–91 | — | — | d |
| 92 | 68 | — | Internally calibrated. Average RX Power. |
| 93 | 80 | — | Alarms, Warnings implemented. |
| 94 | 08 | — | Includes functionality described in Rev 12.2 of SFF-8472 |
| 95 | 64 | — | b |
| 96 - 127 | 00 | — | e |

- VCSEL wavelength is represented in 16 unsigned bits. The hex representation of 850 (nm) is 0x0352.
- Address 63 is the checksum for bytes 0-62 and address 95 is the checksum for bytes 64–94. They are calculated (per SFF-8472) and stored prior to product shipment.
- Addresses 68–83 specify a unique module serial number.

- d. Addresses 84–91 specify the date code.
e. Addresses 96–127 are vendor specific.

EEPROM Serial ID Memory Contents - Enhanced Features (Address A2h)

| Byte # Decimal | Notes |
|----------------|--|
| 0 | Temp H Alarm MSB ^a |
| 1 | Temp H Alarm LSB ^a |
| 2 | Temp L Alarm MSB ^a |
| 3 | Temp L Alarm LSB ^a |
| 4 | Temp H Warning MSB ^a |
| 5 | Temp H Warning LSB ^a |
| 6 | Temp L Warning MSB ^a |
| 7 | Temp L Warning LSB ^a |
| 8 | V _{cc} H Alarm MSB ^b |
| 9 | V _{cc} H Alarm LSB ^b |
| 10 | V _{cc} L Alarm MSB ^b |
| 11 | V _{cc} L Alarm LSB ^b |
| 12 | V _{cc} H Warning MSB ^b |
| 13 | V _{cc} H Warning LSB ^b |
| 14 | V _{cc} L Warning MSB ^b |
| 15 | V _{cc} L Warning LSB ^b |
| 16 | Tx Bias H Alarm MSB ^c |
| 17 | Tx Bias H Alarm LSB ^c |
| 18 | Tx Bias L Alarm MSB ^c |
| 19 | Tx Bias L Alarm LSB ^c |
| 20 | Tx Bias H Warning MSB ^c |
| 21 | Tx Bias H Warning LSB ^c |
| 22 | Tx Bias L Warning MSB ^c |
| 23 | Tx Bias L Warning LSB ^c |
| 24 | Tx Power H Alarm MSB ^d |
| 25 | Tx Power H Alarm LSB ^d |
| 26 | Tx Power L Alarm MSB ^d |
| 27 | Tx Power L Alarm LSB ^d |
| 28 | Tx Power H Warning MSB ^d |
| 29 | Tx Power H Warning LSB ^d |
| 30 | Tx Power L Warning MSB ^d |

| Byte # Decimal | Notes |
|----------------|--|
| 31 | Tx Power L Warning LSB ^d |
| 32 | Rx Power H Alarm MSB ^e |
| 33 | Rx Power H Alarm LSB ^e |
| 34 | Rx Power L Alarm MSB ^e |
| 35 | Rx Power L Alarm LSB ^e |
| 36 | Rx Power H Warning MSB ^e |
| 37 | Rx Power H Warning LSB ^e |
| 38 | Rx Power L Warning MSB ^e |
| 39 | Rx Power L Warning LSB ^e |
| 40–55 | Reserved |
| 56–94 | External Calibration Constants ^f |
| 95 | Checksum for Bytes 0 through 94 ^g |
| 96 | Real Time Temperature MSB ^a |
| 97 | Real Time Temperature LSB ^a |
| 98 | Real Time V _{cc} MSB ^b |
| 99 | Real Time V _{cc} LSB ^b |
| 100 | Real Time Tx Bias MSB ^c |
| 101 | Real Time Tx Bias LSB ^c |
| 102 | Real Time Tx Power MSB ^d |
| 103 | Real Time Tx Power LSB ^d |
| 104 | Real Time Rx Power MSB ^e |
| 105 | Real Time Rx Power LSB ^e |
| 106 | Reserved |
| 107 | Reserved |
| 108 | Reserved |
| 109 | Reserved |
| 110 | Status/Control |
| 111 | Reserved |
| 112 | Flag Bits |
| 113 | Flag Bits |
| 114 | Reserved |
| 115 | Reserved |
| 116 | Flag Bits |
| 117 | Flag Bits |

| Byte # Decimal | Notes |
|----------------|-------------------|
| 118–127 | Reserved |
| 128–247 | Customer Writable |
| 248–255 | Vendor Specific |

- a. Temperature (Temp) is decoded as a 16-bit signed two's complement integer in increments of $1/256^{\circ}\text{C}$.
- b. Supply Voltage (V_{CC}) is decoded as a 16-bit unsigned integer in increments of $100\ \mu\text{V}$.
- c. Tx bias current (Tx Bias) is decoded as a 16-bit unsigned integer in increments of $2\ \mu\text{A}$.
- d. Transmitted average optical power (Tx Pwr) is decoded as a 16-bit unsigned integer in increments of $0.1\ \mu\text{W}$.
- e. Received average optical power (Rx Pwr) is decoded as a 16-bit unsigned integer in increments of $0.1\ \mu\text{W}$.
- f. Bytes 56 through 94 are not intended for use with AFBR-57B4APZ, but have been set to default values per SFF-8472.
- g. Byte 95 is a checksum calculated (per SFF-8472) and stored prior to product shipment.

EEPROM Serial ID Memory Contents - Soft Commands (Address A2h, Byte 110)

| Bit | Status/Control Name | Description | Notes |
|-----|---------------------|---|-------|
| 7 | Reserved | — | — |
| 6 | Reserved | — | — |
| 5 | Reserved | — | — |
| 4 | Reserved | — | — |
| 3 | Reserved | — | — |
| 2 | Reserved | — | — |
| 1 | Reserved | — | — |
| 0 | Data Ready (Bar) | Indicates transceiver is powered and real time sense data is ready (0 = ready). | — |

EEPROM Serial ID Memory Contents - Alarms and Warnings (Address A2h, Bytes 112, 113, 116, 117)

| Byte | Bit | Flag Bit Name Description | Notes |
|------|-----|------------------------------|--|
| 112 | 7 | Temp High Alarm | Set when transceiver internal temperature exceeds high alarm threshold. |
| | 6 | Temp Low Alarm | Set when transceiver internal temperature exceeds low alarm threshold. |
| | 5 | V _{cc} High Alarm | Set when transceiver internal supply voltage exceeds high alarm threshold. |
| | 4 | V _{cc} Low Alarm | Set when transceiver internal supply voltage exceeds low alarm threshold. |
| | 3 | Tx Bias High Alarm | Set when transceiver VCSEL bias exceeds high alarm threshold. |
| | 2 | Tx Bias Low Alarm | Set when transceiver VCSEL bias exceeds low alarm threshold. |
| | 1 | Tx Power High Alarm | Set when transmitted average optical power exceeds high alarm threshold. |
| | 0 | Tx Power Low Alarm | Set when transmitted average optical power exceeds low alarm threshold. |
| 113 | 7 | Rx Power High Alarm | Set when received average optical power exceeds high alarm threshold. |
| | 6 | Rx Power Low Alarm | Set when received average optical power exceeds low alarm threshold. |
| | 0-5 | Reserved | — |
| 116 | 7 | Temp High Warning | Set when transceiver case temperature exceeds high warning threshold. |
| | 6 | Temp Low Warning | Set when transceiver case temperature exceeds low warning threshold. |
| | 5 | V _{cc} High Warning | Set when transceiver internal supply voltage exceeds high warning threshold. |
| | 4 | V _{cc} Low Warning | Set when transceiver internal supply voltage exceeds low warning threshold. |
| | 3 | Tx Bias High Warning | Set when transceiver VCSEL bias exceeds high warning threshold. |
| | 2 | Tx Bias Low Warning | Set when transceiver VCSEL bias exceeds low warning threshold. |
| | 1 | Tx Power High Warning | Set when transmitted average optical power exceeds high warning threshold. |
| | 0 | Tx Power Low Warning | Set when transmitted average optical power exceeds low warning threshold. |
| 117 | 7 | Rx Power High Warning | Set when received average optical power exceeds high warning threshold. |
| | 6 | Rx Power Low Warning | Set when received average optical power exceeds low warning threshold. |
| | 0-5 | Reserved | — |

Broadcom, the pulse logo, Connecting everything, Avago Technologies, Avago, and the A logo are among the trademarks of Broadcom and/or its affiliates in the United States, certain other countries and/or the EU.

Copyright © 2017 by Broadcom. All Rights Reserved.

The term “Broadcom” refers to Broadcom Limited and/or its subsidiaries. For more information, please visit www.broadcom.com.

Broadcom reserves the right to make changes without further notice to any products or data herein to improve reliability, function, or design. Information furnished by Broadcom is believed to be accurate and reliable. However, Broadcom does not assume any liability arising out of the application or use of this information, nor the application or use of any product or circuit described herein, neither does it convey any license under its patent rights nor the rights of others.





Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.