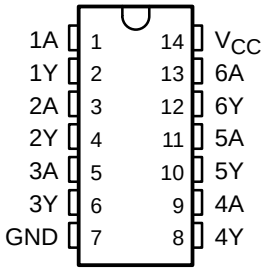
- **AC Types Feature 1.5-V to 5.5-V Operation and Balanced Noise Immunity at 30% of the Supply Voltage**
- **Speed of Bipolar F, AS, and S, With Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **±24-mA Output Drive Current**
  **– Fanout to 15 F Devices**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Exceeds 2-kV ESD Protection Per MIL-STD-883, Method 3015**

**CD54AC05 . . . F PACKAGE**
**CD74AC05 . . . E OR M PACKAGE**
**(TOP VIEW)**




## description

The ’AC05 devices contain six independent inverters. These devices perform the Boolean function $Y = \overline{A}$. The open-drain outputs require pullup resistors to perform correctly, and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

**ORDERING INFORMATION**

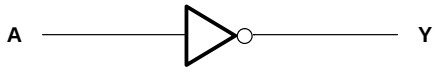
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –55°C to 125°C | PDIP – E | Tube | CD74AC05E | CD74AC05E |
| | SOIC – M | Tube | CD74AC05M | AC05M |
| | | Tape and reel | CD74AC05M96 | |
| | CDIP – F | Tube | CD54AC05F3A | CD54AC05F3A |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**
**(each inverter)**

| INPUT A | OUTPUT Y |
|---|---|
| H | L |
| L | Z |

## logic diagram, each inverter (positive logic)




Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6 V
Input clamp current, $I_{IK}$ ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O = 0$ to $V_{CC}$) . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package . . . . . 80°C/W
M package . . . . . 86°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

| | | | $T_A$ = 25°C | | –40°C TO 85°C | | –55°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 1.5 | 5.5 | 1.5 | 5.5 | 1.5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.5 V | 1.2 | | 1.2 | | 1.2 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.5 V | | 0.3 | | 0.3 | | 0.3 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 4.5 V to 5.5 V | | –24 | | –24 | | –24 | mA |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 4.5 V to 5.5 V | | 24 | | 24 | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 1.5 V to 3 V | | 50 | | 50 | | 50 | ns/V |
| | | $V_{CC}$ = 3.6 V to 5.5 V | | 20 | | 20 | | 20 | |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | $T_A$ = 25°C | | −40°C TO 85°C | | −55°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{OL}$ | $V_I$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 50 μA | 1.5 V | | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3 V | | 0.1 | | 0.1 | | 0.1 | |
| | | | 4.5 V | | 0.1 | | 0.1 | | 0.1 | |
| | | $I_{OL}$ = 12 mA | 3 V | | 0.36 | | 0.44 | | 0.5 | |
| | | $I_{OL}$ = 24 mA | 4.5 V | | 0.36 | | 0.44 | | 0.5 | |
| | | $I_{OL}$ = 50 mA† | 5.5 V | | | | | | 1.65 | |
| | | $I_{OL}$ = 75 mA† | 5.5 V | | | | 1.65 | | | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | | 5.5 V | | ±0.1 | | ±1 | | ±1 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, | $I_O$ = 0 | 5.5 V | | 4 | | 40 | | 80 | μA |
| $C_i$ | | | | | 10 | | 10 | | 10 | pF |

† Test one output at a time, not exceeding 1-second duration. Measurement is made by forcing indicated current and measuring voltage to minimize power dissipation. Test verifies a minimum 50-Ω transmission-line drive capability at 85°C and 75-Ω transmission-line drive capability at 125°C.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 1.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | −40°C TO 85°C | | −55°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLZ}$ | A | Y | | 94 | | 103 | ns |
| $t_{PZL}$ | | | | 74 | | 81 | |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | −40°C TO 85°C | | −55°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLZ}$ | A | Y | 3 | 10.4 | 2.9 | 11.5 | ns |
| $t_{PZL}$ | | | 2.3 | 8.3 | 2.3 | 9.1 | |

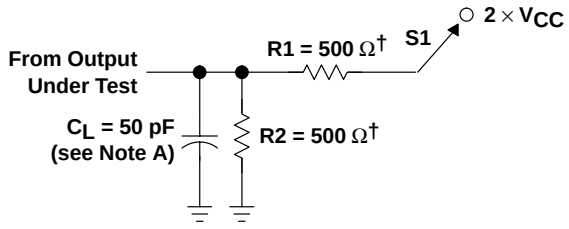
### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V, $C_L$ = 50 pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | −40°C TO 85°C | | −55°C TO 125°C | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_{PLZ}$ | A | Y | 2.2 | 7.5 | 2.1 | 8.2 | ns |
| $t_{PZL}$ | | | 1.7 | 5.9 | 1.6 | 6.5 | |

### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

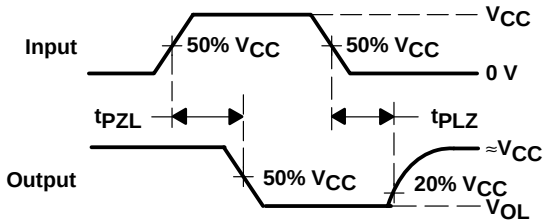
| PARAMETER | | TYP | UNIT |
|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | 105 | pF |

## PARAMETER MEASUREMENT INFORMATION




† When $V_{CC}$ = 1.5 V, R1 = R2 = 1 kΩ

**LOAD CIRCUIT**




**VOLTAGE WAVEFORMS**
**PROPAGATION DELAY TIMES**

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54AC05F3A | ACTIVE | CDIP | J | 14 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | CD54AC05F3A | Samples |
| CD74AC05E | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC05E | Samples |
| CD74AC05EE4 | ACTIVE | PDIP | N | 14 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC05E | Samples |
| CD74AC05M | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC05M | Samples |
| CD74AC05M96 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC05M | Samples |
| CD74AC05M96E4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC05M | Samples |
| CD74AC05M96G4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC05M | Samples |
| CD74AC05ME4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC05M | Samples |
| CD74AC05MG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC05M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.



**OTHER QUALIFIED VERSIONS OF CD54AC05, CD74AC05 :**

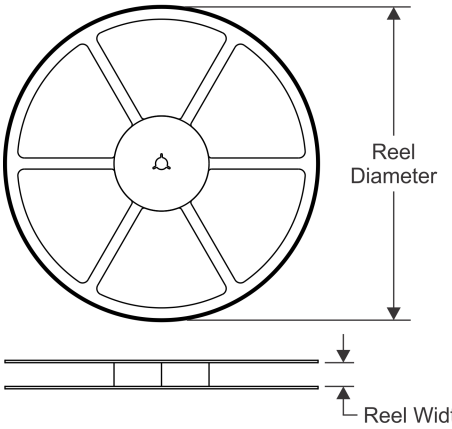
- Catalog: CD74AC05
- Military: CD54AC05

NOTE: Qualified Version Definitions:

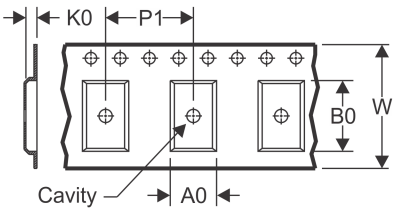
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

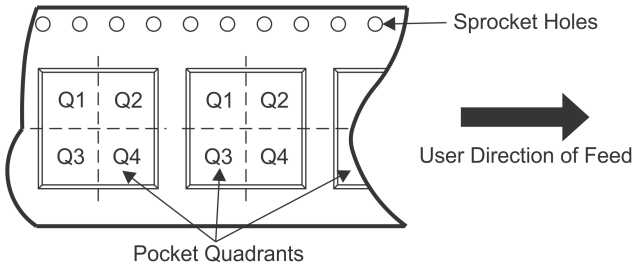



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

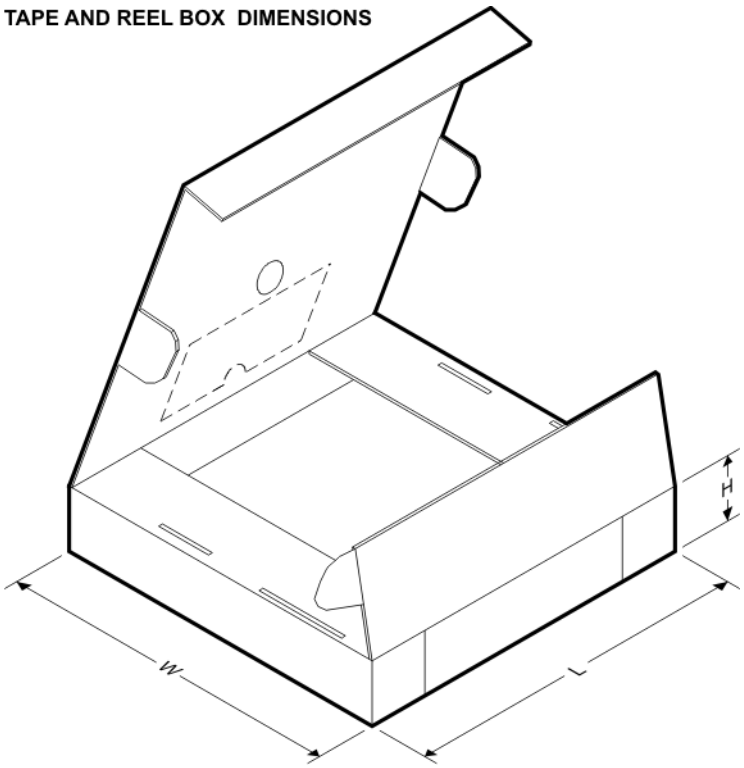
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC05M96 | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



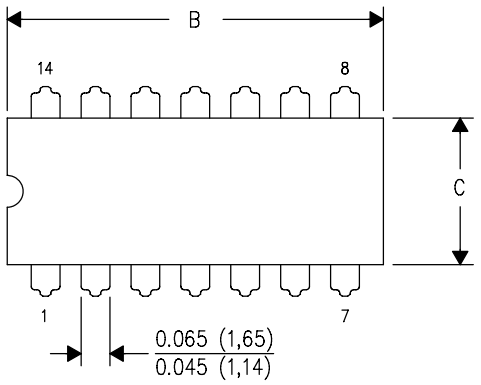

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC05M96 | SOIC | D | 14 | 2500 | 367.0 | 367.0 | 38.0 |

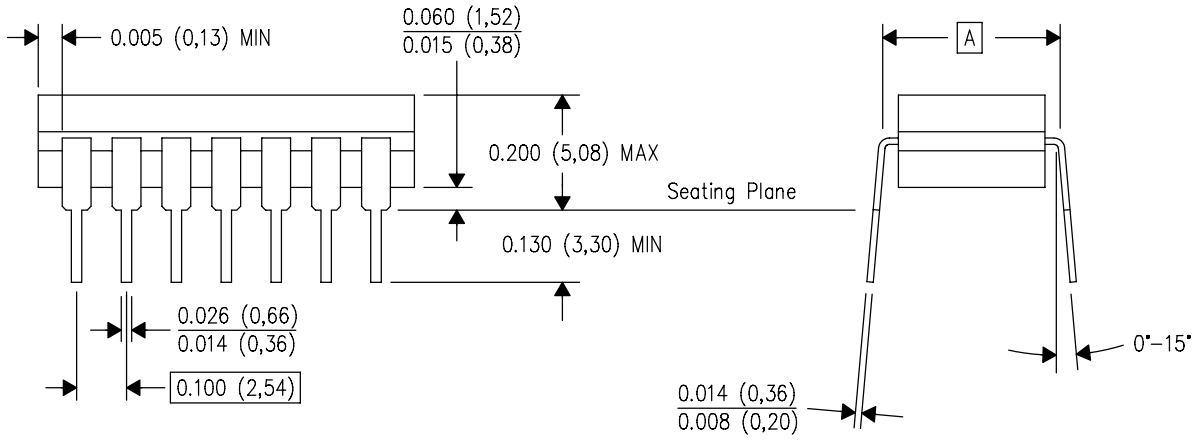
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



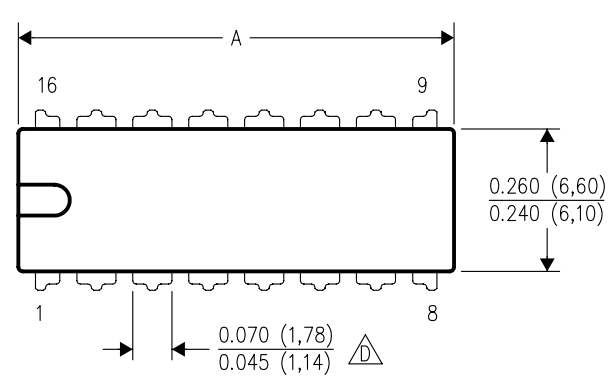

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

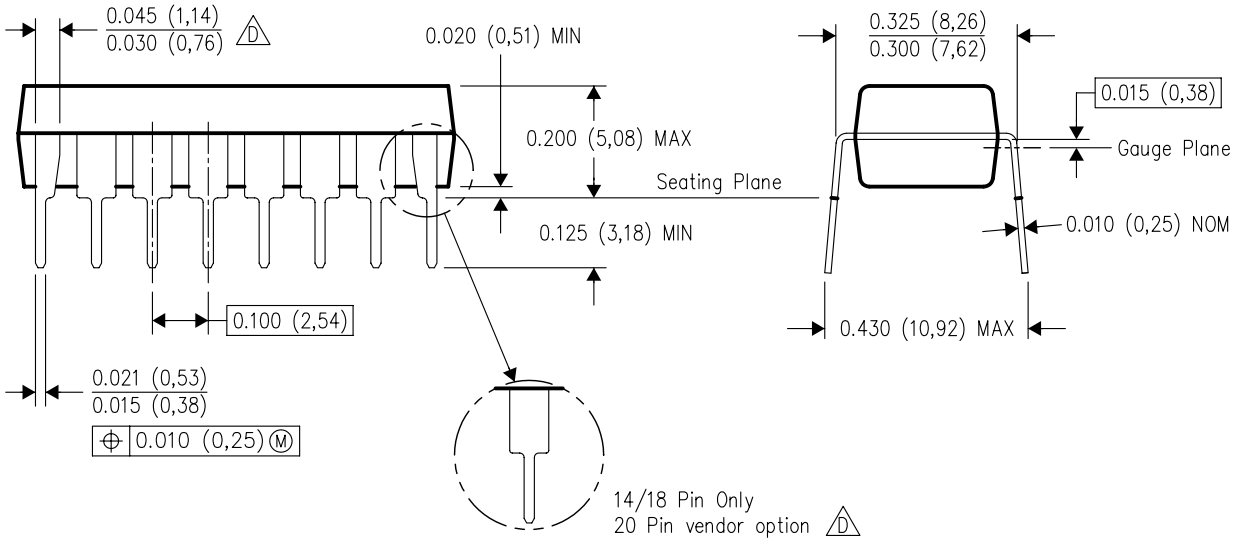
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



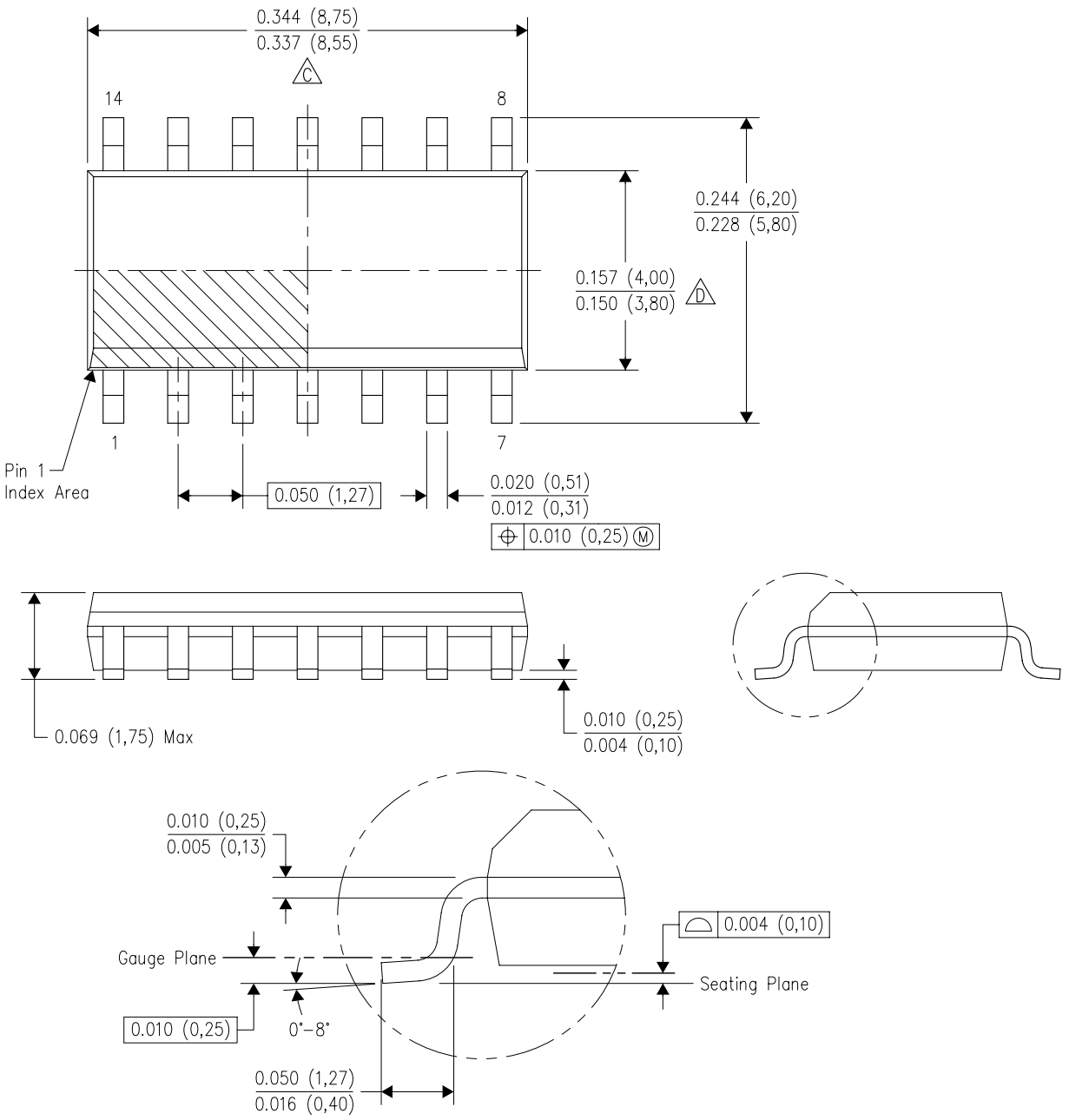

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

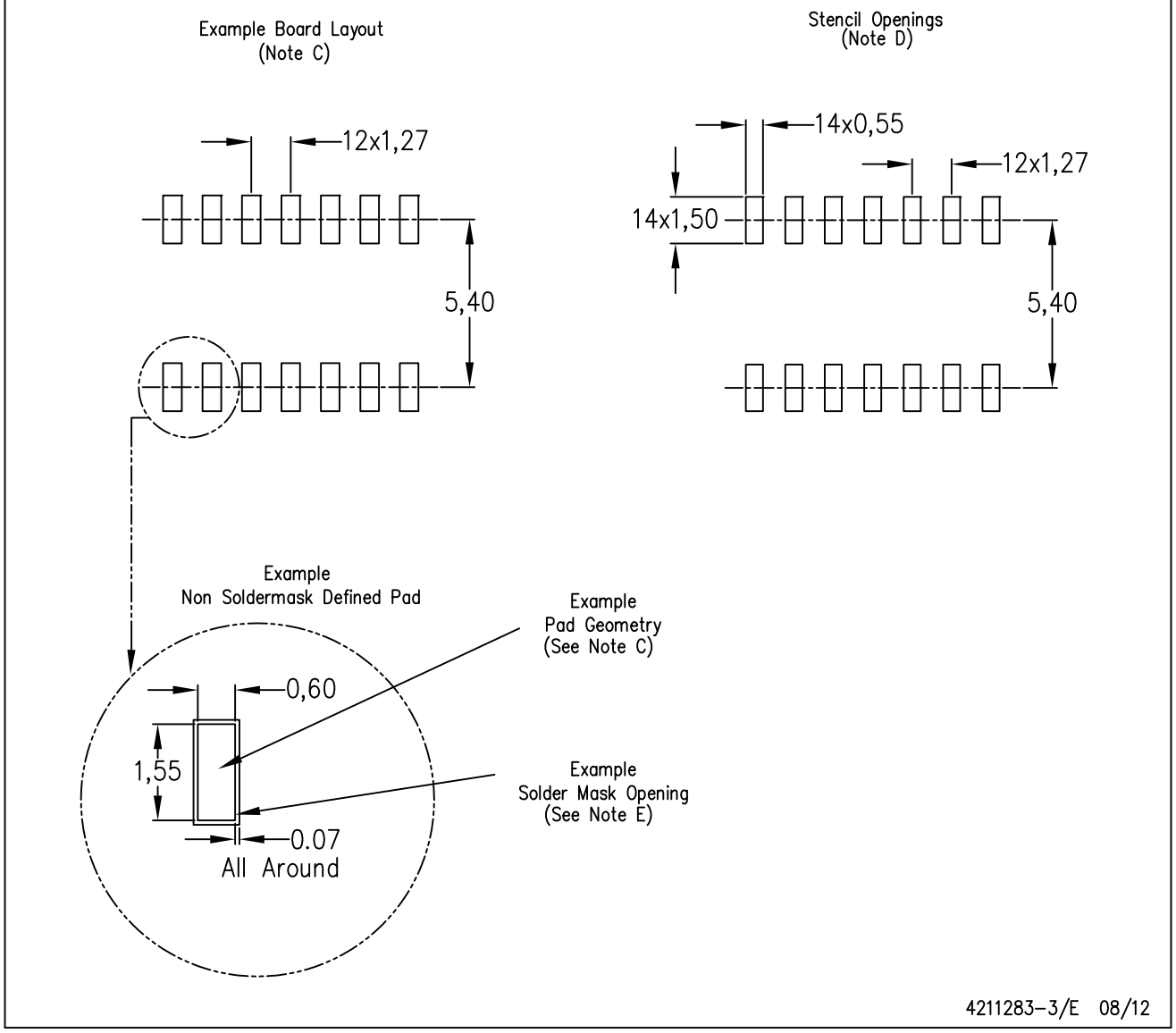
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

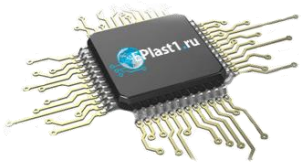
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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